# Balancing Design Challenges in Portable Products

Design With Freescale Low Power Seminars

www.freescale.com/lowpowerseminars

### Low Power Product Design Seminars

A new approach to low power training





# What will I learn?

# Your Goal:

• To develop a scalable handheld battery operated product

# **Our Objectives:**

- To provide you with an understanding of Freescale's low power solutions
- To educate you on the benefits of designing products based on Freescale devices
- To provide you with the techniques required to design a low power, scaleable handheld product with a rich human-machine interface



# Seminar Agenda

32-bit ColdFire

- Defining low power
- Defining your power management strategy
- Selecting your low power MCU
- Other Low Power solutions from Freescale
- Introduction to CodeWarrior & Processor Expert
- Digital Multi-Meter Design



v 8-bit S08

• Low Power Resources & Wrap-up

After the seminar each attendee will be <u>sent an email voucher with instructions on</u> <u>how to get their free development tool</u>.



## **Defining low power**





# The Importance of Low Power

Longer battery life	Reduced operating costs / end product differentiation	
Reduced heat dissipation	Removes cost of heat sinks / fans	<b>E</b>
Reduced system complexity	Faster development / time-to-market	
Ability to meet more low power standards	Larger target market	
Increased reliability for battery back-up critical applications	End product differentiation	C
Increased board density	Increased system performance	



### Low Power Market Overview - SAM







### Freescale's Low Power Strategy

•Develop industry leading low power technology that delivers enhanced battery life performance for embedded applications

•Embed low power IP across the 8-bit S08, 16-bit Digital Signal Controller, & 32-bit ColdFire architectures offering performance & price scalability for low power applications



•Provide an extensive development ecosystem including reference designs, application notes, and training resources (like this seminar!) to promote the awareness of low power design techniques and reduce product time to market





## **Defining Low Power**

How semiconductor manufacturers specify low power?

Measured in Run Current (mA or mA/MHz)

Does high Run Current mean high power consumption?

Measured in Lowest Sleep Current (nA or uA)

Low Power is Defined as Lowest Power Mode. Is it practical? Is it useful in real applications?

Measured in performance per Watt (MIPS/Watt)

Does it make more sense?



## **Defining Low Power**

How customers ask for low power?

Measured in Battery Life (Years)

Customer preferred method

Measured in Average Power (Watt/Hour)

Influences battery life. See the figure on following slide

Measured in Peak Current? (mA)



### **Battery Life vs. Average Current**









# **Defining Low Power**

Low Power means different things for different applications

Every low power design is different and will have its own interesting set of problems to solve. You have to think through every element of the design, not only hardware but software if you want to operate at very low power levels.



### Defining your power management strategy





# Factors affecting power consumption

- MCU Low Power modes
- ► MCU Speed
- MCU Peripheral Power Consumption
- ► Low Power I/O
- ► Periodic Wake-Up from Low Power mode



### **Low Power Modes**

#### How many MCU operating modes are there and what are they?

Does the MCU have one of more low power modes?

#### What are the features of each operating mode?

- > What is the maximum speed?
- What is the regulator status?

Is the Low Power mode practical for your application?

- > How long will the MCU take to recover from the Low power mode? Too long for the application?
- What functions can be supported by the MCU in the Low-Power mode? How to wake up the MCU from the Low-Power mode?



# **MCU Speed**

#### Speed kills !

- Power consumed by modern CMOS devices is almost always dominated by how fast the device is being clocked.
- > As a general rule, if you double the speed, you double the power consumption.
- > We often forget, if you double the bus width, you may also double the power consumption.
- Try to architect your system to run as slowly as practical.

#### Can the clock speed be changed on the fly?

Allow the processor to dynamically change the speed of operation based on instantaneous demand for computing power

#### Run at the full speed across the whole voltage range?

- How fast can the part run at lower voltages?
- Typically Low Power Competitors Have 1MHz Bus Speed



### **Peripheral Power Consumption**

#### Do the peripherals consume power when unused?

> Try to reduce the power consumption of the peripherals unused

#### Is it pratical to turn off all functions in the Low Power mode?

The functions may be critical to your application in the LP mode. For example, the low power mode won't do much good if it turns off the on-chip UART and you have to wake up based on receiving characters on the serial port.

Are the peripherals fully functional when the voltage is low?

- Can the flash be programmed at lower voltages? Typically Low Power Competitors need > 2V
- Can the ADC work at lower voltages?



### Low-power I/O

#### What pull-up values are really needed?

- > The days of using 4.7K pull-up resistors are gone.
- Start thinking of pull-ups with values in the 1MW range.

#### Are all of the pull-up resistors required all of the time?

Consider removing power from pull-ups.

#### Should you use a pull-down instead?

Look at the state you expect an input to be in most of the time. If it will be reliably low most of the time, consider using a pull-down resistor rather than a pull-up.

#### Do not float the I/O unused!

- Current is consumed at the point where the transistor switches.
- Applying a mid-rail voltage and allowing an input pin to float will cause a current to flow from VDD to VSS.
- Ensure that input voltages are held to VDD or VSS.



# **Periodic Wake-Up**

Reducing the power consumption by sleeping and waking up periodically provided your applif your application can

Many embedded applications spend most of their time waiting for something to happen: receiving data on a serial port, watching an I/O pin change state, or waiting for a time delay to expire. If the processor is still running at full speed when it is just waiting for something to happen, we are burning up battery life while accomplishing little.

#### **Example:**

Need to wake every second and read sensor. Every 5 seconds, process data.

Which approach uses less power?

- 1. Run MCU in low-power run the entire time
- 2. Use MCU's RTC with a crystal to provide accurate clock during Stop3 mode
- 3. Use MCU's RTC with internal LPO reference during Stop2 mode



Example



### **Battery Life vs. Average Current**







# **The Product: Digital Multi-Meter**

- ► In the following labs you will design a portable Digital Multi-Meter (DMM)
- ► Why was a Digital Multi-meter chosen?
  - The DMM was selected as the end product for reasons of design simplicity. The low power design principles used in this seminar can be applied to <u>any</u> <u>portable battery-operated product</u>
- ► Typical DMM application requirements
  - Easy development to provide shorter time to market
  - Time keeping in low power mode
  - Ability to turn peripherals on and off in order to reduce power consumption
  - Ability to change System clock speeds
  - Flash programming at low voltages
    - Data capture and display
  - Operation across Battery voltage range 1.8V-3.6V
  - Scalability for a Family of Multi Meter devices
    - Low end DMM to Oscilloscope DMM with Data logger

► In the next section we will map product requirements to MCU device features





# **Selecting your Low Power MCU**





### **Freescale Battery Life Calculator**

#### www.freescale.com/lowpower

•Determines the average current the MCU is consuming and estimate the resulting battery life

•Based on application system variables: V, Hz, °C, % of time in in MCU modes (run, wait, stop3, stop2 and stop1), periodic wakeup interval

•User can select from a variety of standard battery sizes and types or enter battery characteristics directly



Device Panel MCF51QE128  Invironment Settings Run/Wait Mode CPU Frequency (Hz) 50,000,000 PRun/LPWait Mode CPU Frequency (H 32,768 Vvg VDD (V) 3.0 Vvg Operating Temperature (C) 50	Battery Information         Alkaline 9V         10       Battery Self         10       Discharge (uA)         Duty Cycle         1       wake up interval (sec)         0.00       Run %         0.00       Wait %         20.00       LPRun %         50.00       Stop3 %         0.00       Stop2 %	System Options Number of ADC conversions/cycles 5 ACMP on in Stop No LVD on in Stop No TC on in Stop Yes TC Clock Src XTAL	How Many Active Modules? TPM's (0-3) SCI's (0-2) 0 SPI's (0-2) 1 IIC (0-2) ACMP (0-2) 2
Imean Battery Life	Current (uA)	Current Adders (uA)	Boost

•Devices currently supported: S08QE128/96/64, MCF51QE128/64/32, S08QE8

•Additional devices will be added as they are introduced to market



### **Freescale 3V MCU Solutions**









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### **Flexis<sup>™</sup> QE Device Overview**

	S08	ColdFire V1				
CPU Mode	Only one mode	User Mode/Supervisor Mode				
Program Model	A(8-bit), HX(16-bit), SP(16-bit), PC(16-bit), CCR(8-bit)	User Mode D0-7(32-bit), A0-7(32-bit), PC(32-bit), CCR(32-b Supervisor Mode OTHER_A7, VBR, CPUCR, SR(16-bit)				
Bus	8-bit Data bus, 16-bit Address bus	32-bit Data bus, 24-bit Address bus				
Instruction	HC08 instruction set with added BGND, CALL, RTC instructions	ColdFire Instruction Set Revision C (ISA_C)				
Memory Map	64K-byte Memory Map, Memory Management unit (MMU) for S08, 16K paging window for addressing memory beyond 64K, Linear address pointer for addressing data across entire memory,	16M-byte Memory Map, entire memory map addressed directly				
Exception/Interrupt	Support up to 32 interrupt/reset vectors, priorities are fixed, One level interrupt grouping, No hardware support for nesting	Support up to 32 interrupt/exception vectors, interrupt/exception priorities are fixed except two interrupts can be remapped, seven levels interrupt grouping, hardware support for nesting				
Reset	One vector for reset sources	Vectors for up to 64 reset sources				





## **Flexis™ QE Device Overview (Continued)**

	MC9S08QE128	MCF51QE128						
Development Support	Single-wire background debug interface, Same hardware/BDM cable for both devices, One version of CodeWarrior IDE and debugger support both devices,							
Operation Range	Up to 50MHz CPU from 3.6V ~ 2.1V, 20MHz CPU from 2.1V ~ 1.8V, across temperature range -40C ~ 85C							
On-chip memory	8K-byte RAM, 128K-byte Flash							
Operation Made	Run, Low Power Run, Wait, Low Power Wait, STOP3, STOP2							
Operation mode	-	STOP4						
Peripherals	24-ch 12-bit ADC, 2 TPM (3-ch) 1 TPM (6-ch), 2 SPI, 2 SCI, 2 IIC, 16-ch KBI, RTC, GPIC							
	-	Interrupt controller, Rapid GPIO,						
Deskages	Pin to pin compatible in 80	-pin LQFP and 64-pin LQFP						
гаскаges	48-pin QFN, 44-pin QFP, 32-pin LQFP	-						

# **QE Low Power Family Device Overview**

	QE8	QE32	S08QE128	51QE128						
CPU	S08 Up to 20 MHz	S08 Up to 50MHz	S08 Up to 50 MHz	ColdFire V1 Up to 50 MHz						
FLASH	8K Bytes	32K Bytes	128K Bytes	128K Bytes						
RAM	512 Bytes	2K Bytes	8K Bytes	8K Bytes						
ADC	10-ch 12-bit ADC	10-ch 12-bit ADC	24-ch 12-bit ADC	24-ch 12-bit ADC						
ТРМ	2 TPM (3-ch)	2 TPM (3-ch) 1 TPM (6-ch)	2 TPM (3-ch) 1 TPM (6-ch)	2 TPM (3-ch) 1 TPM (6-ch)						
SPI	1 SPI	1 SPI	2 SPI	2 SPI						
SCI	1 SCI	2 SCI	2 SCI	2 SCI						
IIC	1 IIC	1 IIC	2 IIC	2 IIC						
КВІ	8-ch KBI	16-ch KBI	16-ch KBI	16-ch KBI						
Rapid GPIO	NA	NA	NA	Yes						
Others	ICS, RTC, GPIO, BDM									



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## **Ultra-Low Power Overview**

- ► Ultra-low-power run and wait modes
- CPU and peripherals run with voltage regulator in low power mode
- Allows full functionality at reduced frequency for lower power operation

#### ► Clock gating

- Turn clocks off to unused peripherals
- Reduces overall run and wait mode current
- Ultra-low-power internal regulator & oscillator
- Fast Start Up from stop modes, typically 6-7 usec
- New low power external oscillator consumes less than 1 uA
- Ultra-low-power internal clock source & oscillator
- ► Eliminates need for external clock source
- Supports low frequency operations which lowers power in system
- Ultra-low-power real-time counter
- ► Use in run, wait and stop modes
- Use with low power oscillator, internal or external clock sources

	MCF51QE128	MC9S08QE128
Run Mode @ 2 MHz CPU / 1 MHz bus	2 mA	1 mA
Run Mode @ 50 MHz CPU / 25 MHz bus	27 mA	11 mA
Lower Power Run Mode @ 32 kHz CPU/16 kHz bus	50 uA	22 uA
Stop 2 – Lowest power mode; partial power down of circuits	370 nA	370 nA
Stop 3 - Int. circuits loosely regulated; clocks at low frequency	520nA	450 nA
Stop 3 - Wake Up Time	6 us	6 us

Preliminary typical measurements, Vdd = 3V, Temp = 25C



# High Performance and Low Power

- QE128 devices can run at 50 MHz CPU frequency down to 2.4V, 40MHz from 2.4V to 2.1V
  - Configure peripherals in microseconds
  - Copy/search large data tables rapidly
  - Perform complex calculations faster
- Below 2.1V, QE128's can still run at 20 MHz CPU frequency
  - Flexis devices are designed to run at high frequency across all voltages
- Flash programming at 1.8V while typical competitors' lowest is 2.2V
  - If working off batteries, with FSL part customer can re-program flash
  - Ability to update variables/constants and provides greater flexibility
    - Can save variables to flash before batteries die and are replaced
    - Can perform field s/w upgrades at any time, doesn't require fresh batteries





# **Internal Positioning**

	S08QE8	S08QE32	S08QE128	MCF51QE128
Stop2 @ 3V	750 nA	950 nA	2000 nA	11 uA
Stop2 @ 2V	600 nA	850 nA	1900 nA	10 uA
Stop3 @ 3V	1800 nA	2300 nA	4200 nA	18 uA
Stop3 @ 2V	1500 nA	2000 nA	3900 nA	16 uA

#### FSL spec max @70C



## **Freescale Product Specifications**





### **New Product Specifications: S08QE8 & S08QE32**

	S08QE8									S08QE3	2				
		V	typ	max		temp			V	typ	max		temp		
Ρ			0.3	0.65		-40 to 25 P	)		0.35	0.65		-40 to 25			
С		3	0.5	0.8	uA	70	С	С	3	0.8	1	uA	70		
Ρ	Stop 2		1	2.5		85	Р	Stop 2		2	4.5		85		
С			0.25	0.5		-40 to 25	С	С		;		0.25	0.5		-40 to 25
С		2	0.3	0.6	uA	IA 70 C 85 C	C C	2	0.75	0.85	uA	70			
С			0.7	2					1.5	3.5		85			
Ρ			0.4	0.8		-40 to 25	Ρ	Р	3	0.45	1		-40 to 25		
С		3	1	1.8	uA	70	С			1.5	2.3	uA	70		
Ρ	Stop 2		3	6		85	Ρ	Stop 2		4	8		85		
С	Stop 3		0.35	0.6		-40 to 25	С				0.35	0.7		-40 to 25	
С		2	0.8	1.5	uA	70	С		2	1	2	uA	70		
С			2.5	5.5		85	С	С		3.5	6		85		

•Changes have been made to the Flexis QE family product specifications to include power consumption ratings @ 70°C

•Stop Idd grows exponentially with temperature - 70°C rating is significantly lower than 85°C rating – good for applications that don't require 85C

•Parameters are characterized by design [C] and production tested [P]. Parameters that are production tested are checked on every device before it is shipped

•Typical values: the value that most parts will achieve

•Maximum values: the Limit (usually set in production testing) that parts will achieve



### **New** Product Specifications: S08QE128 & MCF51QE128

	S08QE128									51QE <sup>2</sup>	28 - O'	Douls			
		V	typ	max	temp					V	typ	max		temp	
Ρ			0.35	0.6		-40 to 25		Ρ	Р		3	0.6	0.8		-40 to 25
С		3	0.98	2	uA	70		С		3	3.0	11	uA	70	
Ρ	Stop 2		2.5	7.5		85		Ρ	Stop 2	3	8.0	20		85	
С			0.25	0.5		-40 to 25		С		2	0.6	0.8		-40 to 25	
С		2	1.4	1.9	uA	70		C C		2	2.5	10	uA	70	
С			1.91	6.5		85				2	6.0	12		85	
Ρ			0.45	1		-40 to 25		Ρ		3	0.8	1.3		-40 to 25	
С		3	1.99	4.2	uA	70		С		3	6.0	18	uA	70	
Ρ	Stop 2		5	15		85		Ρ	Stop 2	3	18.0	28		85	
С			0.35	0.7		-40 to 25		С	Stop 3	2	0.8	1.3		-40 to 25	
С		2	2.9	3.9	uA	70		С		2	5.0	16	uA	70	
С			3.77	13.2		85		С		2	12.0	20		85	

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### **Other Low Power Solutions from Freescale**












# Introducing new 8-bit MCUs with LCD capability: S08LL16/8, RS08LA8, RS08LE4





### Introducing the L Family

Introducing a trio of 8-bit MCU families (S08LL, RS08LA, RS08LE) with industry-leading LCD capabilities, including the ability to drive more segments with fewer pins (up to 8x mode). In addition, the S08LL family offers best-in-class, ultra-low-power performance.

#### Integrated LCD Driver

High segment on-chip LCD driver module is software-configurable and eliminates the need for separate display driver chip, reducing board space and total system cost.

#### Flexible Pin Functionality

With L family MCUs, developers can drive more segments with fewer pins, enabling smaller connectors and smaller footprint. Different functionality can be assigned to pins, enhancing design flexibility

#### **Ultra-Low Power**

Developers can choose from a wide range of products within the family to optimize their designs for power-conscious, cost-sensitive applications.







## **New Segment LCD Solutions**

Segment LCD Solutions	Key Features & Benefits
S08LL16/8	<ul> <li>The LL16/8 offers Freescale's ultra-low-power technology at 1.8V with winning features, such as 20MHz CPU, flash reprogramming and ADC accuracy. Intended for low-power and portable applications, such as thermostats and blood glucose meters.</li> </ul>
9RS08LA8	<ul> <li>The LA8 is a cost-effective MCU that features 6-channel 10-bit ADC, analog comparator, internal charge pump and internal oscillator.</li> </ul>
9RS08LE4	<ul> <li>The LE4 has the RS08 core, which provides 8-channel 10-bit ADC in 28-pin SOIC package options for small appliances and meters.</li> </ul>
Common Features	<ul> <li>LCD features can drive large segment (8x mode) LCDs with fewer pins. FP or BP reassignment simplifies PCB layout and provides the opportunity to optimize designs for EMI performance.</li> </ul>



## Mew MC9S08LL16 – Ultra Low Power with Segment LCD

Introducing the 8-bit MCU LL family with industry-leading LCD capabilities, including the ability to drive more segments with fewer pins (up to 8x mode). In addition, it offers best-in-class, ultra-low-power performance.

#### S08 Core

•Up to 20M CPU

•Temperature range of -40°C to 85°C, 1.8-3.6V Op Range

- •On-Chip Memory
  - FLASH read/program/erase over full operating voltage and temperature
  - 2K Random-access memory (RAM)
  - Flash size LL16: 16K-byte, 8K in Flash A, 8K in Flash B LL8: 10K-byte, 8K in Flash A, 2K in Flash B

#### •Clock Source Options

- Oscillator (XOSC) Loop-control Pierce oscillator; Crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz
- Internal Clock Source (ICS) Internal clock source module containing an FLL controlled by internal or external reference; supports bus frequencies up to 10 MHz

#### •System Protection

- Watchdog computer operating properly (COP) reset
- · Low-voltage detection with reset or interrupt
- Illegal opcode detection with reset
- FLASH block protect

#### •Single Wire Background Debug Interface



#### •Power-Saving Modes

- 2 very low power stop modes
- Reduced power wait mode
- Low power run and wait modes allow peripherals to run while voltage regulator is in standby
- Very low power external oscillator that can be used in stop2 or stop3 modes to provide accurate clock source
- 6 usec typical wake up time
- Peripheral clock gating



## **MC9S08LL16: Low Power Features**

#### Power Saving modes

- 2 very low power stop modes
- Reduced power wait mode
- Low power run and wait modes allow peripherals to run while voltage regulator is in standby
- 6 usec typical wake up time

#### Low Power LCD Module

- Low power LCD waveform
- Multi LCD power supply configuration
- Efficient internal charge pump to produce LCD bias voltages
- LCD display and blink in Low Power mode

#### Low Power Oscillator

Very low power external oscillator that can be used in stop2 or stop3 modes to provide accurate clock source in LP mode

#### Others

- TOD for low power time keeping
- Clock gating



### **Freescale Battery Charging Solutions**





### **Target Applications for Battery Chargers**





## **Freescale Battery Charger Benefits**

The industry's most flexible battery charger ICs that can be customized for a wide variety of applications during the final test phase of the manufacturing process

Flexibility	High Performance/Accuracy	Compact Packaging	
Not just three devices but a family of devices because of flexibility	These chargers provide the highest performance and accuracy in the industry	Meets customers' needs of manufacturing smaller, lighter portable devices	
Process allows quick customization to meet application needs	Output voltage accuracy up to 0.2% at room temperature	2x3 mm ultra thin dual flat no-lead (UDFN)	
Pin-out, feature set and charging parameters can be customized to customer requirements	Output voltage accuracy up to 0.4% at over temperature	Low profile package 0.65 mm	
Up to hundreds of configurations with initial devices	Charge current accuracy is 6% over temperature	Cost efficient	



### Where Does It Fit in System?





### MC3467x Product Roadmap

A complete family from the low end to the high end....



Applications : PC peripherals, cell phone, blue-tooth headset, MP3, gaming, PMP, portable Medical, POS, bar code scanners



semiconducto

### **Battery Charger Solutions: Product Overview**





### **Battery Charger Solutions: Competitive Overview**

		Max	Max	Safaty	Thormal	Dwr Doth	<u> </u>	Voltago	Status		
		voltage		Timer?	Reg?	mamt	Accuracy	Accuracy	Indication	OVP	
Vendor	Part Number	(V)	(A)	(Y/N)	(Y/N)	(Y/N)	(+/- %)	(+/- %)	(# of bits)	(V)	Package
TI	bq24061/2/3/4/5/6	18	1	Y	Y	N		0.5	3	6.5V/10.5	3x3DFN-10
TI	bq24030/2/5/8	18	1.5	Y	Y	Y	17	1	4	-	3.5x4.5QFN-20
TI	bq24020/2/3/4/5/6/7	7	1	Y	N	Ν		1	2	-	3x3DFN-10
Intersil	ISL6294	28	0.9	N	Y	N	10	1	2	6.5	2x3DFN-8
Intersil	ISL6299A	28/7	1	N	Y	N	10	1	2	-	3x3DFN-10
Intersil	ISL6292/B/C/D	7	2	Y	Y	N	10	1	2	-	3x3DFN-10/4x4/5x5
Intersil	ISL6297	7	1.5	Y	Y	N	10	0.7	2	-	4x4QFN-16
Maxim	MAX8808X/Y/Z	16	1	N	Y	N	10	1	2	7	2x2TDFN-8
Maxim	MAX8606	16	1	Y	Y	N		0.5	2	5.8	3x3TDFN-14
Maxim	MAX1551/5	7	0.28	N	Y	N	20	0.5	1	-	SOT23-5
LTC	LTC4055	5.5	1.25	Y	Y	Y	5	1	2	-	4x4QFN-16
LTC	LTC4065	5.5	0.75	Y	Y	N	5	1	1	-	2x2DFN-6
LTC	LTC4059A	10	0.9	N	Y	N	6	1	1	-	2x2DFN-6
LTC	LTC4075	10	0.95	Y	Y	N	5	1	2	-	3x3DFN-10
National	LM3658	6.5	1	Y	Y	N	15	1.5	2	-	3x3DFN-10
Freescale	MC34xxxx	28	1.2	Y	Y	N	5	0.5	3	5.5/6.8/11	2x3DFN-8/2x2DFN-8



## **Battery Charger Solutions: Summary**

- ✓• Industry's most flexible Li-ion and Li-polymer battery charger solution
- ✓• Complete charger for single-cell Li-ion and Li-polymer batteries
- ✓• Feature-rich and easily modified to meet the needs of a wide variety of applications
  - ✓ +/-0.7% output voltage accuracy over -20°C to +70°C (+/-0.4% at room temperature)
  - ✓ +/-0.7% output voltage accuracy over -40°C to +85°C (MC34675)
  - ✓ +/-5% charge current accuracy over -40°C to +85°C (+/-6% for MC34673
  - ✓ and MC34675)
- ✓• Factory-configurable parameters for faster time to market and lower system cost
- ✓• Meets AC/DC adapter standard YD/T 1591-2006 in the Chinese cell phone market
- Low external component count



### **Freescale Low Power Features**





### **Freescale Low Power Features**

- 1. Multiple power-saving modes
  - 6 modes totally
  - Low-power run and wait modes 
     New
- 2. Clock gating for the periphrals
- 3. Internal Clock Source (ICS) module allows to generate clock signals from a variety of sources
- 4. Ultra-low-power (ULP) 32kHz oscillator
- 5. New voltage regulator
  - Faster wake up times
- 6. Low power Peripherals Real Time Counter
  - Ultra-low power Real Time Counter (RTC)
  - Low power ADC





### **Operation Modes**







## QE8 – Run Mode

#### ► Run Mode

- Standard user mode default mode out of any reset
  - Clocks are enabled to CPU and all peripherals
  - All peripherals disabled out of reset.
- The voltage regulator is in active mode
- Typical IDD as low as 5.6 mA at 10 MHz Bus and 3V with all modules enabled.

#### Advantages

- All peripherals can be used without limitations
- Interrupts can be serviced without changing modes
- Flash can be reprogrammed across all VDDs and temperature

#### Limitations

· Consumes more current than other modes







## **QE8- Wait Mode**

#### ► Wait Mode

- The bus clock source remains active
- Clocks are disabled to CPU but peripherals can be clocked
- Typical IDD as low as 0.57 mA at 10 MHz CPU and 3V

#### ► Advantages

- Reduces power consumption versus run mode
- No stop recovery time; the interrupt is serviced immediately
- Reduces noise while taking A-to-D readings

### ► Limitations

• The voltage regulator remains active, consuming more current than stop or LP modes

#### ► Exit times :

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WAIT

## **QE8 Low-power Modes : LPRun**



#### ► Low-power Run (LPRun) Mode

- The bus clock source is limited to FBELP
- Typical IDD as low as 7.3  $\mu A$  at 32 kHz CPU and 3V when executing from RAM
- Typical IDD as low as 21 uA at 32 kHz CPU and 3V when executing from Flash
- The voltage regulator is in low-power mode

#### ► Advantages

- All peripherals can be used
- Reduces power consumption versus Run mode when high performance is not required
- Interrupts can be serviced without changing modes

#### ► Limitations

- Maximum frequency is limited (see reference manual)
- Flash cannot be programmed or erased







## Low-power Modes—LPWait



## ► Low-power Wait (LPWait) Mode

- The bus clock source is limited to FBELP
- Clocks are disabled to CPU but peripherals can be clocked
- Typical IDD as low as 1  $\mu A$  at 32 kHz CPU and 3V
- The voltage regulator is in low-power mode

## ►Advantages

- Reduces power consumption versus LPRun mode
- · No stop recovery time; the interrupt stacking begins immediately
- Reduces noise while taking A-to-D readings

## ► Limitations

- Consumes more current than stop modes
- Maximum frequency is limited
- Due to slower frequencies, may take longer to react to wake-up trigger than stop2 or stop3 modes







## **QE8-Low-power Modes: Stop3**

#### ► Stop3 Mode

- Bus and CPU clocks halted
- Voltage regulator in standby
- Typical IDD of 400 nA at 3V
- Exit with any active interrupt: ADC, ACMP, IRQ, KBI, LVD, RTC, SCI or reset

#### ▶ Exit times : 6 uS

#### Advantages

- Still has very low-current consumption
- RAM and register retain their values
   Does not require reinitializing peripherals
- Latency from interrupt event to code execution is only 5 us + 38 ICSOUT • cycles

#### Limitations

Not quite as low current as stop2







## **QE8- Low-power Modes: Stop2**

#### ► Stop2 Mode

- Partial power down mode with typical IDD as low as 300 nA at 3V
- Exit with wake-up pin (IRQ/RESET pin) or RTC
  - Stop2 recovery is always through a system reset

### Advantages

- Lowest-power consumption mode for these devices
- RAM contents are maintained, I/O pin states are latched.
- ► Exit times : 29 uS

### Limitations

- Register values are reset, but values can be saved to and restored from RAM
- Wake up latency from reset to code execution is ~5 us + 162 ICSOUT cycles.







## **CPU Mode Comparison Chart**

	Features	Exit Sources	Wake-up Time
Run	CPU clocks can be run at full speed Internal supply is fully regulated	n/a	n/a
Wait	CPU not clocked System clocks are running Full regulation is maintained	Any interrupt	Instantly
LP Run	Bus frequency is restricted to 125 kHz maximum Voltage regulator standby	Clear LP bit or interrupt with LPWUI set	n/a
LP Wait	CPU not clocked Bus frequency is restricted to 125 kHz maximum Full regulation is maintained	Any interrupt	Instantly
Stop 3	CPU not clocked Voltage regulator stand by Peripherals not clocked but powered for fast recovery	RTC, LVD/LVW, ADC, ACMP, IRQ, SCI, KBI or RESET	6 µs
Stop 2	CPU and peripherals not clocked Voltage regulator partial power down RAM content is retained	RTC, IRQ or RESET	29 µs

## **New Voltage Regulator**

- Voltage Regulator is always on when MCU is in Run or Wait modes
  - Also on when in stop3 with LVI or ADC enabled
  - Runs internal logic at lower voltage, therefore lower power
- Modified stand-by mode to allow execution in low power modes
  - New LPRun and LPWait modes allow peripherals to run while regulator is in stand-by
  - Condition for this is to have ICS configured in a special low power modes where bus frequency is restricted (125 KHz max)
  - New faster regulator start-up time! 6 uS
  - Allows more applications to use Stop modes



#### Periphrals Clock Gating µA Saved Through Clock Gating @ 20MHz CPU in FEE Mode

- Clock gating is the mechanism used to disable the clock tree to any unused peripheral
- Bus or peripheral clock runs to all modules
  - Regardless if they are enabled or not
- Saves power by not clocking unused gates

#### Using the system clock gating registers RUN IDD can be reduced by up to ~33%



Total Run Current with all module clocks disabled = 5050uA Total Run IDD with all module clocks enabled = 7480uA



## How does power relate to ICS?

- Software-selectable bus frequency divider (BDIV)
  - Available in all clock modes •
  - Allows frequency changes without losing FLL Lock in FEI and FEE •
  - Run fast only when needed •
- Low-power or high-gain oscillator options
  - Low-power limits voltage swing on oscillator pins to minimize power consumption
- The external reference can be left enabled in stop mode
  - 32 kHz crystal in low-power mode only adds 800nA to stop mode currents!
- Stop mode currents are affected only by the references enabled in stop mode, not the ICS mode before entering
  - Ex: if running FEE mode with ext oscillator enabled in stop mode, only the ext ٠ oscillator will be enabled when stop is entered, the FLL will be disabled automatically





## **Ultra-low Power Real-time Counter (RTC)**

- Enhancement from Real-Time Interrupt Module
- ▶ 1 kHz internal low-power oscillator (LPO)
  - 300 nA typical power consumption
  - No crystal required
  - Independent of internal bus clock source
- External clock option for greater accuracy
  - 550 nA typical power consumption with 32 kHz low power oscillator
- Programmable wake-up intervals
  - 8-bit counter
  - 15 selectable input clock prescalers
  - 8-bit user programmable modulo value
- ► Can be enabled in any mode

#### TIP

The internal LPO oscillator can be measured against the bus clock. User software can adjust RTC timeout to compensate for inaccurate LPO clock.







### Introduction to CodeWarrior & Processor Expert



## **CodeWarrior IDE (Integrated Development Environment)**

#### Fully featured and class leading IDE

- ► Full-chip simulation and flash programming
- Assembler, linker, and source level debugger supports all MCUs
- Highly optimized ANSI C compiler and C (code limitations)
- Automatic C code generation for on-chip peripherals with Processor Expert
- ► Special edition for S08 free up to 32k code
  - CodeWarrior for Microcontrollers
- ► Special edition for MCF51 free up to 64k code
  - CodeWarrior for Microcontrollers

😰 True-Time Simulator & Real-Time Debugger - C:\FAE - C for embedded\Lab	s\SOB Lab 5 - Arguments\P&E_FCS.ini	
Eile Yiew Run PEDebug ⊆omponent Data Window Help		
□☞묘 ४୭€ १♥ →>국국수→ →		
S Source	Assembly	
C:\FAE - C for embedded\Labs\S08 Lab 5 - Arguments\Sources\main.c Line: 15	main	
<pre>void main(void) (E function(); result2 = function2(0x07); result2 = function2(0x07); result2 = function2(0x07); result2 = function2(0x07); for();) (E for();) (E varA+; </pre>		
📓 Data:1		~
Address: 105 Size: 1 main.c Auto Symb Global VarA 16 unsigned char	# Register	
result2 8 unsigned char	HCS08 CPU Cycles: 2336	Auto
result3 0 unsigned int	A 8	*
For Help, press F1	9508GB60 STEPPED OVER	1



## What is Processor Expert?

#### A rapid application design tool with ...

- Graphical User Interface which allows an application to be specified by the functionality needed
- Automatic code generator which creates tested, optimized C code tuned to the application needs and selected Freescale MCU
- Built-in knowledgebase, which immediately flags resource conflicts and incorrect settings in the beginning phase

#### Creating...

Hardware Abstraction Layer (HAL) – hardware-dependent, low-level drivers with a known application programming interface (API)

#### **Benefits**

- Eases migration between Freescale devices
- Designers don't have to be intimately familiar with every page of a specification
- Errors are caught early in design cycle; therefore, designers get to market faster with higher quality product



### What is an Embedded Bean?

Embedded Beans are software components, which encapsulate the initialization and functionality of an embedded system's basic elements

- CPU core
- CPU on-chip peripherals
- FPGAs
- Stand-alone peripherals
- Virtual devices
- Pure software algorithms

Embedded Beans provide a hardware abstraction layer (HAL), which eases migration between devices



### What's Device Initialization

#### ► Device Initialization is...

- A Graphical User Interface with CPU, peripherals and pins, which allows registers to be setup via individual bits or parameters
- An automatic code generator which creates initialization code in C or assembly

Sevice Initialization [MCF51JM128VLK] from project Project	S Inspector Init_SCI	
😋 🗱 Select CPU Package 🛛 🕒 Generate Code 🛛 📮 Backup 🛛 🗁 Bestore 🦳 Help	Bean Parameters	Register Details
	✓ Device SCI2 ▼SCI2	Address Init.value Register Map
	E Settings	⊞ SCI2BDH 0xFFFF8040 00 H     ■ ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
a 🗘	Clock settings	SCI2BDL 0xFFFF8041 04 H
	SCI2 Clock Gate Enabled D	
	Baud rate divisor 4	SCI2C2 0xFFFF8043 00 H
旺 성성성공공보도 동양성공을 없었도도도 공중국	L ✓ Baud rate 65536 baud	
	Loop mode Disabled Disabled	SCI2S2 0xFFF8045 C0 H ● ● ● ○ ○ ○ ○ ●
PI2 R0 PM PI2 R0	V Receiver source Loop mode	SCI2C3 0xFFFF8046 00 H ●●
RESET PTUL RG	🚽 🖌 TxD pin direction Input 🚽	SCI2D 0xFFF8047 00 <u>H</u> ●●●●●●●
PTED_TPM PTA PTB PTC PTD PTJD_RG	🗸 🖌 Data Format 🛛 8 bits 🗨	SCGC1 0xFFFF980B FF H 0000000
PTE PTE PTE PTG PTH PTD2_KBI	🖌 🖌 Stop in Wait mode 🛛 Disabled 🕥	
	🖌 🖌 Wake up 🚽 Idle line wakeup 🚽	
TITE THE PTJ RGPIO RTC TPM1 Vieth	· ✓ Idle character counting After start bit 🗨	
PTC6.Rx TPM2 COP SCII SCI2 Veldad =	Receive Wake Up Idle Di Don't set IDLE bit	
PTF7_TKC SPH SPI2 ADC HC1 PTD1_AD	🖌 🖌 Parity None 💌	
TPTF5_TPM PTD_AD	🖌 🖌 Send break Disabled 🖸	
PTF8 IIC2 MISCAN USB_OTG ACMP PTB7_AD	Receiver wakeup Normal operation	
INTER DV CMT IntFLASH IRGModule KBH BIGE KDH	Break character generatic 10 or 11 bits	
PTE2 TPM PMGA DB CPU	Transmitter output Not inverted	
PTB3_TPM PTB3_SS2	Receiver input     Not inverted	
PTC7 PTB2_SPS	LIN Break detection Disabled	
PTH0_S0 PTB1_M0	E Pins	
MCF51JM128VLK PT60_MIS	RxD pin allocation Enabled	
	RxD pin PTC5_RxD2   PTC5_RxD2	
化甘草醇 医甲酮 化合物 化合物 化合金 化合金	TxD pin allocation Enabled	
	L V TxD pin PTC3_TxD2  ▼ PTC3_TxD2	
	Interrupts	
	Tx interrupt	
	H / Interrupt Vsci2tx Vsci2tx	
<b>U</b>	🔿 Dialla Baistand Laiteration   🗖   🔿   🥥   🔽 View Rec	ister Map
43 PTB1_MOSI2_ADF PTB1_MOSI2_ADF (none) General purpose IO, Port B, bit 1; SPI2 pin MOSI; ADC channel 1 //		) 🔹 undefined, reserved, read-only 🔜 🔨 🛄 🕺





## **Migration Aids**

- ► Porting initialization code/low level drivers with Processor Expert
  - Use GUI to map software components to resources on new silicon
  - Regenerate initialization code and low-level drivers
  - Limitations
    - Only code generated by Processor Expert can be reconfigured and regenerated.
- ► Porting initialization code with Device Initialization
  - Use GUI to select, configure and generate initialization code for new silicon
  - Replace initialization code in project



## **Evaluate Silicon**

# ► CPU Package and Peripherals

- Displays selected targeted MCU with its peripherals and pins
- Pins associated with a peripheral are highlighted when mouse hovers over the peripheral
- Help is available for pins and peripherals by moving the mouse over the item




## **Evaluate Silicon**

## ► CPU Block Diagram

- Every peripheral is represented by a block.
- Every block contains slots for every resource that can be allocated (e.g. pin or channel).
- If the resource is allocated, the slot contains the icon of the allocating component.





## **Unique in the Market**

### ▶ Processor Expert delivers functionality that is unique in the market.

	CodeWarrior - Processor Expert	RealView Tools Suite	Green Hills	IAR (VisualSTATE 6.1)	HITEX (startEasy)	Keil
Graphical Interface	Yes	Yes	Yes	Yes	Yes	Yes
Configurable Application Notes	Yes	No	No	Yes	Yes	No
Integrated Knowledgebase	Yes	No	No	No	No	No
Generates Initialization Code	Yes	No	No	Yes	Yes	No
Generates Low Level Drivers	Yes	No	No	Yes	No	No
Tools to Add Higher Level Drivers	Yes	No	No	No	No	No
Integration with UML Modeling Tools	Yes	Yes	Yes	Yes	No	Yes

\* Software support for ARM competitors



## **Digital Multimeter Design**



Agenda

## Introductory information

- System design
- Software Overview
- CodeWarrior, Processor Expert, and Beans
- Lab1: QE8
- Lab2: QE32
- Lab3: QE128 (HCS08)
- Lab4: QE128 (Coldfire V1)



# Digital Multimeter System Design

Hardware Overview







#### Digital Multimeter System Design Hardware Overview

Hardware Block Connection:

- ► Base Board (J1) connects DEMOQE (J1)
- ► Base Board (J2) connects TFT
- ► Base Board (J5) connects Touch panel board (J1)
- ► Four possible MCU daughter boards connect to DEMOQE:
  - MC9S08QE8
  - MC9S08QE32
  - MC9S08QE128
  - MCF51QE128



## **Digital Multimeter System Design**

Hardware Overview

#### **Functional Diagram:**





## Hardware & Software Re-use

To meet the time-to-market requirements of the DMM project, the re-use of Freescale reference h/ware & s/ware was essential -

- DEMOQE128 board & associated daughter cards
  - www.freescale.com/flexis
- DMM Connector/Expansion board
- DMM Software

[Freescale 3<sup>rd</sup> party vendor]



[Freescale]

#### C DISPLAY 3000

- DEMOQE128TFT LCD board & display driver software
  - S/ware is included with purchase of any DEMOQETFT LCD board
  - www.shop-en.display3000.com/pi19/pi18/pd38.html



- Capacitive touch software
  - www.freescale.com/proximity



Proximity-Nearness in Place, Time, Relation and Now Touch Sensors

MPR08X proximity sensors for intelligent touch control

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[Freescale]

#### DMM System Design Base Board Configuration



 Jumper JP4 and JP5 control input range for Voltage input 1 and 2

High Voltage input range: 0 – 15V

Low Voltage input range: 0 – 7.5V

 Jumper JP1 controls input range for Current input High Current input range: 100 uA~100 mA
 Low Current input range: 500 nA~500 uA

Default Jumper Settings				
Jumper	Setting			
JP1	500nA – 500uA (IL)			
JP2	(V)			
JP3	(V)			
JP4	0 – 7.5V (VL)			
JP5	0 – 7.5V (VL)			
JP6	Installed			
JP7	Installed			





### DMM System Design Operational Overview

## Using the DMM Base Board:

- ► Jumper JP4 controls input range for Voltage input 1
  - JP4 VL selects 0 ~ 15V
  - JP4 VH selects 0 ~ 7.5V
- ► Jumper JP5 controls input range for Voltage input 2
  - JP5 VL selects 0 ~ 15V
  - JP5 VH selects 0 ~ 7.5V
- ► Jumper JP1 controls input range for Current input 1
  - JP1 IL selects 500 nA 500 uA
  - JP1 IH selects 100 uA 100 mA





## DEMOQE Board Jumper Settings:

Accelerometer				
Jumper Pins				
J13	2&3			
J14	2&3			
J15	2&3			
J16	None			

Inputs				
Jumper Pins				
J12	None			
J18	1&2, 3&4			
J11	1&2, 3&4			

System Power				
Jumper Pins				
J3	2&3			
J4	3&4			
J5	3&4, 5&6			

RS232				
Jumper	Pins			
J6	1&2			
J7	1&2			
J8	2&3			

External Clock		Buzzer		IIC Pullups		Analog	
Jumper	Pins	Jumper	Pins	Jumper	Pins	Jumper	Pins
J17	1&2, 3&4	J19	1&2	J20	None	J21	None

LEDs		
Jumper	Pins	
J9	None	



#### **DEMOQE Board Jumper Locations**





#### Software Overview Architecture



- Three functional layers
- Each functional layer is unaware of the layer(s) above it
- Base code generated exclusively by Processor Expert Beans
- HAL layer generalizes hardwarespecific functionality
- Application layer implements demo application functionality
  - Object oriented module-based approach









- Base layer sources contained in "Base" and "Generated Code" source groups
- "Generated Code" source group contains all Beans-generated code
- "Base" source group contains Beans code that is tied to user modules through Processor Expert





- Hardware Abstraction Layer is contained in the "HAL" source group
- Contains sub-group for serial I/O utilizing Beans-generated functions
- Contains sub-groups for off-the-shelf TFT display and touchpad interface libraries
- HAL code is common for all targets





- Application modules are contained in the "Application" source group
- Each module implemented as one source and one header file
- Application layer
  The list of included application modules will change/increase as program complexity increases



#### Software Overview Directory Structure



- We will start with QE8 project and modify this project for migration to other targets
- Target-specific projects allow seminar labs to continue should something go wrong
- The majority of the source is common amongst all targets
- Only programctl modules differ from target to target



Agenda

- Introductory information
  - System design
  - Software Overview
- CodeWarrior, Processor Expert, and Beans
- Lab1: QE8
- Lab2: QE32
- Lab3: QE128 (HCS08)
- Lab4: QE128 (Coldfire V1)



#### **Processor Expert, and Beans**

- Beans are self contained configuration modules that automatically generate peripheral driver code
- ► Beans provide a high-level interface to low-level hardware functions
- Modifying Beans settings has little to no impact on the code using it; code is refactored on-the-fly
- CPU Beans allow the changing of target MCUs on-the-fly within the same project

Peripheral driver Beans in this project include:







#### **CodeWarrior, Processor Expert, and Beans Beans Configuration**

Freescale CodeWarrior File Edit View Search Project Processor Expert Device Initialization 💕 📕 ゆ ひ 🕆 🐂 🖷 🦓 📕 🧭 seminar.mcp P&E Multilink/Cyclone Pro 🔻 🟥 🔝 🖌 🌾 💺 Files Link Order Targets Processor Expert 🖃 🗁 Configurations ✓ & DEMOQE\_08QE8CFM × 🔈 DEMOQE\_08QE32CFT 🗶 象 DEMOQE\_08QE128CLH × 🔈 DEMODE 510E128CLH 🗁 Operating System E CPUs 🗄 🗸 🍘 Cpu:MC9S08QE8CFM 🗶 👜 Cpu:MC9S08QE32CFT 🗶 🕋 Cpu:MC9S08QE128CLH 🗙 翸 Cpu:MCF51QE128CLH 🖃 🗁 Beans 🗄 🗸 🙆 SM1:SPIMaster[SynchroMaster] 🕀 🗸 🎲 TI1:TimerInt 🛨 🗸 🔇 AD1:ADC 🕀 🗸 🙆 KB1:KBI 🗄 🗸 🌐 TPM\_Prox:Init\_TPM 🗄 🗸 🛞 TPM2\_HighSpeed:Init\_TPM 🖃 🗁 User Modules 🖌 🚟 seminar.c:main 🗸 🔜 Events.c:event 🗖 🗁 Generated Modules 🕀 🗁 Bean Modules 🖌 🧱 PE Const.h V III PE Error.h V E PE\_Timer.c ✓ 📰 PE\_Types.h Vectors.c 🗁 External Modules 🖻 🗁 Documentation seminar SIGNALS.txt 🔜 seminar\_Settings.xml seminar.txt

CPU Beans allow the changing of target MCUs on-the-fly within the same project

- Peripheral driver Beans in this project include:
  - SPI (SM1) ٠
  - Real Time Counter (TI1) •
  - ADC (ADC1) •
  - Keyboard Interrupt (KB1) ٠
  - Timer/PWM1 (TPM Prox) •
  - Timer/PWM2 (TPM\_HighSpeed) •
- User code that uses Beans is mapped to "User Modules" allowing on-the-fly refactoring when Beans settings or naming changes



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Technique 1: Using Processor Expert

- Processor Expert generates the underlying driver code
- ► If the target changes, the driver code will be re-generated automatically since driver function definitions are specific to a given Bean, and not the target MCU



Technique 2: Using the provided register map

- Freescale provides a standard header file containing the entire register map for all Flexis MCUs
- Contains named interrupt vector definitions
- ► This header file can be accessed directly, or through Beans
- Easy to use Word, Byte, or bit access to registers
- Flexis MCUs with compatible peripheral sets can be targeted easily; naming conventions are consistent





Technique 3: Defining standard primitive types

- Primitive type sizes can be different from one compiler to another
- Defining a fixed set of standard primitives will allow seamless migration between CPU targets and compilers

#### Example:

```
typedef unsigned char uint8;
typedef unsigned short uint16;
typedef unsigned long uint32;
typedef char int8;
```

typedef short int16; typedef long int32;

### Compiler Setup:





Things to avoid:

- Avoid using assembly code wherever possible
- Absolute memory declarations for memory access, peripheral addressing, and interrupt vectors

## Things to be cautious of:

- Timing routines
  - blocking cpu timers will not necessarily execute at the same rate
  - clocking may not be the same between targets
- ► Entering low power modes

More information: *Migrating from 8-bit S08 to 32-bit ColdFire V1 using CodeWarrior for Microcontrollers V6.x Application Note* 



## Low Power Considerations: Software

► Properly set the system options and configurations registers

- The stop instruction must be enabled
- Low voltage detect in stop mode must be disabled
- The internal bandgap signal must be disabled
- Enable/disable the IRQ and Reset pins as necessary
- ► Routines to enter low power modes should disable all un-necessary internal and external peripherals
  - SCI/SPI should be disable so that pin control is handled by GPIO
  - All unused GPIO should be configured
  - TFT display should be placed into low power mode

► Routines to recover from low power modes must handle reinitializing the TFT display







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LAB1: QE8

## **QE8** Overview

	QE8	QE32	S08QE128	51QE128	
CPU	S08 Up to 20 MHz	S08 Up to 50MHz	S08 Up to 50 MHz	ColdFire V1 Up to 50 MHz	
FLASH	8K Bytes	32K Bytes	128K Bytes	128K Bytes	
RAM	512 Bytes	2K Bytes	8K Bytes	8K Bytes	
ADC	10-ch 12-bit ADC	10-ch 12-bit ADC	24-ch 12-bit ADC	24-ch 12-bit ADC	
ТРМ	2 TPM (3-ch)	2 TPM (3-ch) 1 TPM (6-ch)	2 TPM (3-ch) 1 TPM (6-ch)	2 TPM (3-ch) 1 TPM (6-ch)	
SPI	1 SPI	1 SPI	2 SPI	2 SPI	
SCI	1 SCI	2 SCI	2 SCI	2 SCI	
IIC	1 IIC	1 IIC	2 IIC	2 IIC	
КВІ	8-ch KBI	16-ch KBI	16-ch KBI	16-ch KBI	
Rapid GPIO	NA	NA	NA	Yes	
Others	ICS, RTC, GPIO, BDM				



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### MCU: MC9S08QE8

Specs				
CPU	HCS08			
RAM	512 Bytes			
Flash	8192 Bytes			
Max Bus Clock	10 MHz			
Max CPU Clock	20 MHz			





#### Lab 1: QE8 Software Overview

### Program Mode: Digital Multimeter



- readings on two voltage inputs and one current input
- Can select input range with jumpers
- Readings displayed on the TFT LCD
- ► Can enable/disable voltage inputs
- User input is done through push buttons on LCD board
- Enters low power "sleep" mode after a user configurable timeout interval
- Measurements taken upon "wakeup" from sleep mode
- Wakeup sources RTC and KBI



#### Lab 1: QE8 Software Overview

### Program Mode: Digital Multimeter

- ► Implements a Digital Multimeter
  - Performs readings on two voltage inputs and one current input
  - Can select input range with jumpers
  - Readings displayed on the TFT LCD
  - Can enable/disable voltage inputs
- User input is done through push buttons on LCD board
- Enters low power "sleep" mode after a user configurable timeout interval
- Measurements taken upon "wakeup" from sleep mode
- Wakeup sources RTC and KBI



# Lab 1: QE8

**Graphical User Interface** 

- Single UI screen no program mode switching
- Very simple UI element definitions
- Mapping button functions one-to-one
  - Push button D4 to enable/disable voltage inputs
  - Push button D5 to select voltage range
  - Push button D7 to select current range
  - Push button D6 to select display timeout
- The active UI element is not highlighted



**DMM Mode** V1: V2: On/Off:  $|\mathsf{X}|$ On/Off:  $|\mathsf{X}|$ Value: 0.0V Value: 0.0V Range: LOW Range: LOW 11 Value: 0.0A **I1 Range: HIGH** 11 **Display Timeout: Os** Range Volt Volt Disp EN Range TO D7 ()D6 A0: D4 D5

## Using POT to measure voltage







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Non-blocking push-button polling:

- One channel of one TPM module used as a debounce timer
- ► A change in button values starts the debounce timer and disables further polling
- ► In the *configure\_debounce\_timer* function,
  - The TPM counter is read
  - Compare register is set such that a compare event happens 10 ms in the future
- Compare ISR sets debounce flag in programctl module and keys are polled again when this is detected by the program loop
- ► Generated ISR function and timer Bean used to accomplish this



#### Lab 1: QE8 Application Features

## **Graphical User Interface**

- Custom UI written on top of off-the-shelf LCD drawing library
  - Drawing library allows for lines, shapes, text
- ► 8k code size is the primary constraint
- Code was kept small through:
  - Simplified implementation of UI module used in QE32 and QE128 code
  - Mapping button functions one-to-one (no dynamic UI element highlighting)
  - Very simple UI element definitions cannot re-paint an element
  - Single UI screen no program mode switching
  - Minimized use of program modules external to programctl



### Program control structure

- ► This is the heart of the application; ties all module functionality together
- Program modes implemented by individual functions with program loops
- Program mode functions called from top-level switch statement in set\_next\_program\_mode(void)
- ► The QE8 currently has one program mode
- ► No blocking calls in any of the program modes
- Program modes are determined by the mode variable (static to programctl)
  - If this is changed anywhere, the current program mode function will drop out of
     its program loop and return
  - The next program mode will be called from the set\_next\_program\_mode
    function


# Sleep/Wakeup

•

- ► In power.c, stop mode functions are defined
  - Cpu\_SetStopMode() function generated by the CPU bean
- In programctl, when the power\_set\_mode\_stop3() function is called, code stops executing
- When a wakeup source (RTC, KBI, etc.) generates a wakeup condition, code resumes executing within the power\_set\_mode\_stop3() function and returns



# Low Power Design Challenge

► For the QE8 application the main Low power design challenge was configuring the TFT Display for low power

- The TFT display interface involves several GPIO and SPI lines
- In order to enter low power modes several steps were necessary
  - The SPI was disable in order to allow the SPI pins to be configured as GPIO
  - The CS and D/C lines were driven low
  - The RESET line Was driven low

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► Upon wake up the display has to be re-initialized in order to recover from the low power configuration

►NOTE: Low power designs should always place internal and external peripherals in a low power state, and handle recovery within the software routines



# Compile, Run, and Test!





## Lab 1: QE8 Testing

Stop Current				
SIDD(nA)	Condition	Note		
400	Stop3, 3V	External Crystal		
300	Stop2, 3V	disabled		
1350	Stop3, 3V	External Crystal		
1300	Stop2, 3V	enabled		



Test Point:

- ► Test on Jumper J5.5 and J5.6 Near DC Power jack.
- ► Test on Jumper J24 (next to buzzer).





## Lab 1: QE8 Self-Study Project Enhancement

# **Enhancement: Event Scheduler**

- ► Channels in a given TPM module are a finite resource
- Can maximize the use of TPM peripherals by scheduling events through dynamically configuring a TPM channel's compare interrupt
- Events objects are queued in a doubly linked list sorted by timer compare value
- Insertion sort algorithm used to add new elements to the list
- Compare ISR calls event callback (on\_timeout\_ptr in diagram)

#### Functions to be written:

```
int8 schedule_event(uint16 ticks_from_now, on_timeout_fn callback);
void ch_n_compare_isr(void);
```

#### Event queue:











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LAB2: QE32

# **QE32** Overview

	QE8	QE32 S08QE128		51QE128
CPU	S08 Up to 20 MHz	S08 Up to 50MHz	S08 Up to 50 MHz	ColdFire V1 Up to 50 MHz
FLASH	8K Bytes	32K Bytes	128K Bytes	128K Bytes
RAM	512 Bytes	2K Bytes	8K Bytes	8K Bytes
ADC	10-ch 12-bit ADC	10-ch 12-bit ADC	24-ch 12-bit ADC	24-ch 12-bit ADC
ТРМ	2 TPM (3-ch)	2 TPM (3-ch) 1 TPM (6-ch)	2 TPM (3-ch) 1 TPM (6-ch)	2 TPM (3-ch) 1 TPM (6-ch)
SPI	1 SPI	1 SPI	2 SPI	2 SPI
SCI	1 SCI	2 SCI	2 SCI	2 SCI
IIC	1 IIC	1 IIC	2 IIC	2 IIC
КВІ	8-ch KBI	16-ch KBI	16-ch KBI	16-ch KBI
Rapid GPIO	NA	NA	NA	Yes
Others	ICS, RTC, GPIO, BDM			



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### MCU: MC9S08QE32

Specs			
CPU	HCS08		
RAM	2k Bytes		
Flash	32k Bytes		
Max Bus Clock	25 MHz		
Max CPU Clock	50 MHz		





# **Proximity/Capacitive Sensing: Overview**

The S08QE32 based DMM design will include a proximity/capacitive touch sensing user interface implemented using Freescale's off-the-shelf capacitive touch software library

#### ► What is capacitance sensing?

- Technology that enables detection of touch by measuring capacitance
- Responds to a change in physical stimulus
- Used in many areas of consumer, industrial and automotive applications
- Can be used to measure liquid level and detect frost
- One of the most popular applications today is touch sensing
- ► Single Electrode



#### Multiplexed Electrodes









# **Proximity/Capacitive Sensing: Benefits**

#### User interface flexibility & product differentiation

- > Enables more intuitive user interfaces such as rotary wheels and linear sliders.
- Enables an evolution in user interfaces in a wide range of applications
  - Ability to hide buttons underneath the surface and illuminate them when needed
  - Ability to "morph" touchpad patterns depending on mode of device
- Gives greater flexibility for product designers
- Enhances reliability by eliminating mechanical button/switch wear & tear

#### **Reduced system power consumption**

- Enables battery-powered applications
- Satisfies the market need for "green" products

#### **Reduced cost and time-to-market**

- Enables current MCU users to "just add touch"
- Additional integration lowers component cost
- Providing complimentary enablement software lowers development cost and speeds time to market











### **Proximity/Capacitive Sensing: New Products**

#### MPR083 – Rotary Capacitive Touch Sensor Controller

- Sensitive touch panel control
  - 8-positon rotary
  - · Button and switch replacement
  - Multiple electrode configurations
  - Low 1.8 3.6 voltage operation
  - I<sup>2</sup>C interface



#### MPR084 – Touchpad Capacitive Touch Sensor Controller

- Sensitive touch panel control
  - 8 touch pads
  - · Button and switch replacement
  - Multiple electrode configurations
  - Low 1.8 3.6 voltage operation
  - I<sup>2</sup>C interface



#### Proximity Sensing Software Solution for Freescale S08 and ColdFire® V1 MCUs

#### Available on all S08/V1 MCUs (hundreds of MCUs)

- Complimentary (royalty/NRE free)
- Downloadable from freescale.com
- Development kits available as a plug-in module to the MCU development kits
- Allows customer to perform both control and UI functions.



# **Proximity/Capacitive Sensing Software Solution**

#### **Features**

- ►NRE/royalty-free solution
- ► Supports up to 32 electrodes
- ► Wide variety of hardware options
  - Compatible with HC9S08 and ColdFire V1 products
  - 1.8V–5.0V operation (MCU dependent)
  - Numerous package options (MCU dependent)
  - -40°C to +85°C operating temperature
- ► Programmable sampling period
- ► Simple averaging function as basic low pass filter
- Adjustable touch threshold setting
- ► Source code built on Codewarrior Suite
- Electrode touch buzzer sound feedback

#### **Applications**

- ► General Consumer
  - Remote controls / Cell phone / Appliances
- General Industrial
  - Building control panels / Machine user interface







### Lab 2: QE32 Touch Pad

- ► E8 Switch between Configuration Mode and Display Mode
- ► E7 Scroll Right through the UI elements
- ► E6 Select UI element
- ► E5 Scroll left through the UI elements
- ► E1 ~ E4 are implemented as a slider

► Freescale's off-the-shelf capacitive touch library is used

- ► KBI with capacitive touchpad can not wake the system up from the LP mode
- ► Only remaining wakeup source is the RTC
- ► Use the RTC to wakeup and poll the touchpad once every 250 ms in sleep mode



### Lab 2: QE32 Software Overview

## Program Mode: Enhanced Digital Multimeter



- readings on two voltage inputs and one current input
- Can select input range with jumpers
- Readings displayed on the TFT LCD
- Can enable/disable voltage inputs
- Implements an enhanced UI
- Separate screens for DMM configuration and display
- User input is done through capacitive touch pad
- Enters low power "sleep" mode after a user configurable timeout interval that can wake the system up
- Measurements now taken at user configurable intervals



### Lab 2: QE32 Graphic User Interface

Configuration Mode	Display Mode
Configuration	Values
V1 Settings V2 Settings	
On/Off: On/Off: 🔀	V1 Voltage: 0.217V
Range: LOW 🗢 Range: LOW 🗢	V1 Voltage: 0.217V
I1 Range: LOW 🗢	I1 Current: 20.25uA
Display Time: 1 🔽	
Measure Time: 1 🔽	
E5[<] E6[0] E7[>] E8[M]	E5[<] E6[0] E7[>] E8[M]



# Changes in Processor Expert

- 1. Click on Change MCU/Connection
- 2. Select MC9S08QE32 from the list
  - Ensure that *P&E Multilink Cyclone Pro* is selected

seminar.mcp

P&E Multilink/Cyclone Pro

Errors: 2, warnings: 0, hints: 0

🍸 ERROR: Error in the bean setting. N

T ERROR: Error in the bean setting. N

🖃 🍸 📾 KB1

🖃 🍸 🔇 AD1

Files Link Order Targets Processor Expert

- Ensure that the Backup project before changes box is unchecked
- 3. Note the Processor Expert errors
- 4. Click the Processor Expert tab in left panel
- 5. Right click the KBI Bean's icon and click the *Bean Enabled* menu item to disable it; it is not needed
- 6. Right click the *TPM\_Prox:Init\_TPM* bean's icon and click the *Bean Enabled* menu item to enable it





😩 🖗 😽 👘



# Changes in Processor Expert

- 7. Double click *AD1:ADC* icon to bring up Bean Inspector for this bean
  - in *Channel0*, click dropdown for PTA0 to remove error
  - in *Channel2*, click dropdown for PTA1 to remove error

Sean Inspector AD1:ADC		
Bean ItemsVisibility Help < >		View Regs >
Properties Methods Events Comment		
🖌 Bean name	AD1	
✓ A/D converter	ADC	- ADC
✓ Sharing	Disabled	0
Interrupt service/event	Disabled	0
I A/D channels	4	+ -
Channel0		
A/D channel (pin)	PTA0_KBIP0_TPM1CH0_ADP0_ACMP1PLUS	Unknown Peripheral name: PTA0_KBIP0_TPM1CH0_ADP0_ACMP1PLUS
🚺 🗤 A/D channel (pin) signal	PTA0_KBI1P0_TPM1CH0_ADP0_ACMP1PLUS	
- 🖸 Channel1	PTA1_KBI1P1_TPM2CH0_ADP1_ACMP1MINUS	A/P channel (select pin name).
A/D channel (pin)	PTA2 KBI1P2 SDA ADP2	ERROR: Unknown Penpheral name: PTAU_KBIPU_TPMTCHU_ADPU_ACMPTPLI

- 8. Close the bean inspector (saves changes)
- 9. Double click *SM1:SPIMaster* icon to bring up Bean Inspector for this bean
  - ► Under Settings > Shift clock rate, expand this option by clicking the ellipsis
  - Scroll down to the max speed (8.371 MHz) and click it; click OK to save





# Changes in Processor Expert

- 10. Expand the *TI1:TimerInt* bean
- 11. Double click the red X beside *SetPeriodMS* function to enable it to be generated. This should turn into a green check mark I SetPeriodMS
  - 🗹 M SetPeriodSec
- 12. Double click *TI1:TimerInt* bean icon
- 13. Click the ellipsis next to the Interrupt period setting
  - ► Change Init value to 10 ms
  - ► Change Low limit to 10 ms
  - Change High limit to 500 ms

<ul> <li>Interrupt period</li> </ul>		1 sec				<b></b>		
<ul> <li>Same period in modes</li> </ul>	A							
✓ Bean uses entire timer	🐃 Timing - Inter	rrupt period						×
Initialization	Proceedere Page value	e Hich speed mode	li ow coeed mode	Slow speed mode	Adjusted values			1
🖌 🖌 Enabled in init. code	Clask severes	Auto salast	Disabled	Disabled	high: DTClatCli			-
Events enabled in init.	Clock source:	Auto select	Disabled	Disabled	nigh. HTCINICIK			
E CPU clock/speed selection	Prescaler:	Auto select	Disabled	Disabled	high: 64			
High speed mode		10 11 11 11						
V Low speed mode	Huntime setting type	: I nom time interval	<u> </u>		Possible settings	Llock path		
└ ✓ Slow speed mode	Value type	Value	Unit		From	Till	Step 🖉	
	Init.value:	10 💌	ms	•	30.581µs	7798.165µs	30.581µs	
	Low limit:	10 💌	ms	-	61.162µs	15.596ms	61.162µs	
	High limit:	500 👱	ms	•	122.324µs	31.193ms	122.324µs	

14. Note the warning generated by PE

15.



🖃 **? 🎯** 🕅

👒 Errors: 0, warnings: 1, hin<u>ts: 0</u>



## Changes in the CodeWarrior Project

- 1. Click the *Files* tab on the left panel
- 2. Remove both *programctl* files by right clicking them and selecting *Remove*
- 3. Remove both *sui* files the old simplified UI from the QE8
- 4. Right click on the Application source group and click Add Files..
- 5. Browse from the top-level directory to: <top\_level>\src\common\Application and select the ui and ui\_screens source files
  - These are the source files for the enhanced UI
- 6. Browse from the top-level directory to: <top\_level>\src\s08\qe32 and select the programctl files
  - ► These implement the target-specific program control structure





## Changes in the CodeWarrior Project

- 7. Click the *Edit* > *Standard Settings* menu
- 8. Click on the *Access Paths* on the left pane
- 9. Click on the old QE8 directory and press the *Remove* button
- 10. Press OK on the Standard Settings dialog
- 11. Open seminar.c from the file browser on the left panel
- 12. Modify the *start\_program\_ctrl* function to take the *PROGRAM\_MODE\_NORMAL\_DMM\_CONFIG* setting as an argument
  - Starts the program off in normal DMM mode instead of the old QE8 DMM mode
  - Can see program mode definitions in programctl.h
  - ► Browse the code to see how program modes are switched



## What have we just accomplished?

- ► We now have:
  - More RAM
  - More Flash
  - More peripherals
  - Pin-compatibility
  - Identical tool chain, development environment, design flow
- ► We are running on a completely different processor target
- Switching processors typically involves lengthy redesigns
- Demonstrated the ability to enhance our product with minimal impact on:
  - The original HW/SW design
  - The existing design flow



### Lab 2: QE32 Software Overview

# Program Mode: Enhanced Digital Multimeter

- ► Implements a Digital Multimeter
  - Performs readings on two voltage inputs and one current input
  - Can select input range with jumpers
  - Readings displayed on the TFT LCD
  - Can enable/disable voltage inputs
- Implements an enhanced UI
- Separate screens for DMM configuration and display
- User input is done through capacitive touch pad Freescale's off-the-shelf capacitive touch library is used
- Enters low power "sleep" mode after a user configurable timeout interval that can wake the system up
- Measurements now taken at user configurable intervals
- Press E8 to scroll through program modes



Lab 2: QE32 Testing

# Compile, Run, and Test!





# Enhanced Graphical User Interface

- Code size limitation no longer a major issue
- Instead of fixed one-to-one mappings for button functions, can now intelligently highlight UI elements and select them
  - UI elements each have an "on\_select" callback in addition to the many new dynamically modifiable attributes
- Widgets now contain basic color attributes
- ► UI widget definitions and drawing functions contained in *ui* module
- Screen configurations and widget declarations contained in *ui\_screens* module
- Can implement basic object model allowing inheritance and generalized widget actions
  - Recursive painter A top-level redraw function that traverses the list of on-screen to find "dirty" widgets that need to be re-drawn
  - *on\_select* callbacks for widgets allow actions to be mapped



Low power touchpad polling and display:

- Cannot use KBI with capacitive touchpad to wake the system up
- Only remaining wakeup source is the RTC
- Cannot tight poll on touchpad in sleep mode due to power concerns

# Solution:

- Use the RTC to wakeup and poll the touchpad once every 250 ms in sleep mode
- ► No need to debounce anymore



# Low Power Design Challenge

► With the addition of the capacitive touch pad interface, the low power design strategy had to change slightly in order to handle this new interface

Low power touchpad polling and display:

- Cannot use KBI with capacitive touchpad to wake the system up
- Only remaining wakeup source is the RTC
- Cannot tight poll on touchpad in sleep mode due to power concerns

Solution:

- Use the RTC to wakeup and poll the touchpad once every 250 ms in sleep mode
- ► No need to debounce anymore

NOTE: Implement timed polling schemes to lower overall average power consumption



## UI navigation through button callbacks

- ► All program modes have the same user input interface
  - [E5:SCROLL LEFT] [E6:SELECT] [E7:SCROLL RIGHT] [E8:MODE SWITCH]
- Scrolling through UI elements with E5 and E7:
  - Every UI screen has a linked-list of UI elements; pressing E5 or E7 traverses to the next or previous (respectively) element in this list
  - The current element is de-highlighted, and the next is highlighted
- ► Selecting a UI element with E6:
  - UI widgets all inherit from the UIElement type
  - This UIElement type defines an element that is a function pointer to functions with a uint8 select\_function(void) signature
  - Pressing the select button, E6, calls this callback
- Switching program modes with E8:
  - The main program loop for each program mode is conditional on the mode variable
  - When E8 is polled and active, the polling function changes the mode variable



### Lab 2: QE32 Self-Study Project Enhancement

# Enhancement: Touchpad slider widget

- Use the enhanced UI to create a slider widget that can represent one value in a continuous range
- ► Use the remaining four capacitive touch pads E1 to E4 to implement the slider
- Use the touchpad library in the HAL code to read adjacent pad values and interpolate between the two highest ones to determine slider position

Design challenges:

- How will this widget be integrated into the current polling scheme?
- How will the widget's *on\_select* callback be called?







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LAB2: QE128

# **S08QE128 Overview**

	QE8	QE32 S08QE128		51QE128
CPU	S08 Up to 20 MHz	S08 Up to 50MHz	S08 Up to 50 MHz	ColdFire V1 Up to 50 MHz
FLASH	8K Bytes	32K Bytes	128K Bytes	128K Bytes
RAM	512 Bytes	2K Bytes	8K Bytes	8K Bytes
ADC	10-ch 12-bit ADC	10-ch 12-bit ADC	24-ch 12-bit ADC	24-ch 12-bit ADC
ТРМ	2 TPM (3-ch)	2 TPM (3-ch) 1 TPM (6-ch)	2 TPM (3-ch) 1 TPM (6-ch)	2 TPM (3-ch) 1 TPM (6-ch)
SPI	1 SPI	1 SPI	2 SPI	2 SPI
SCI	1 SCI	2 SCI	2 SCI	2 SCI
IIC	1 IIC	1 IIC	2 IIC	2 IIC
КВІ	8-ch KBI	16-ch KBI	16-ch KBI	16-ch KBI
Rapid GPIO	NA	NA	NA	Yes
Others	ICS, RTC, GPIO, BDM			



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### Lab 3: QE128 (HCS08) Device Overview

### MCU: MC9S08QE128

Specs			
CPU	HCS08		
RAM	8k Bytes		
Flash	128k Bytes		
Max Bus Clock	25 MHz		
Max CPU Clock	50 MHz		





### Lab 3: QE128 (HCS08) Software Overview



# New Program Mode

- 5 Modes (screens) for: DMM configuration, Display, Scatter plot, Data logger for Accelerometer and DMM inputs
- Scatter plot
  - Shows the accelerometer's output on a two-axis display
  - Can select which two axes of the accelerometer are displayed
- Data logger for Accelerometer and DMM inputs
  - Can capture data from both inputs
  - Scroll through captured data in a display window
  - Send captured data out to a serial port (use PE Micro USB scope utility)



# Lab 3: QE128 (HCS08) New Graphic User Interface



Scatter Plot Mode

Data logger for Accelerometer Mode



# Lab 3: QE128 (HCS08)

**New** Graphic User Interface

Data logger for DMM inputs Mode





### Lab 3: QE128 (HCS08) Migration Process

## Changes in the CodeWarrior Project

- 1. Click on *Change MCU/Connection*
- 2. Select MC9S08QE128 from the list
  - Ensure that P&E Multilink Cyclone Pro is selected
  - Ensure that the Backup project before changes box is unchecked
- 3. Click the *Files* tab on the left panel
- 4. Remove both *programctl* files by right clicking them and selecting *Remove*
- 5. Right click on the *Application* source group and click *Add Files...*
- 6. Browse from the top-level directory to: <top\_level>\src\s08\qe128 and select the programctl files
  - These implement the target-specific program control structure









### Lab 3: QE128 (HCS08) Migration Process

# Changes in the CodeWarrior Project

- 7. Browse from the top-level directory to:
   <top\_level>\src\common\Application and select
   logging.c/logging.h, and bitmap\_screens.c
  - ► The "logging" files implement the datalogger functionality
  - The bitmap\_screens contains the bitmap arrays for the accelerometer scatter-plot background graphic
- 8. Right click the HAL/Serial source group and select Add Files...
- 9. Browse from the top-level directory to: <top\_level>\src\common\HAL\Serial and select serialio.c/serialio.h files
  - These file implement the higher level RS232 functionality and utilize the SERIAL bean we will add
- 10. Open serialio.c and add #include "SERIAL.h" at the top of the file to the list of included header files.


### Changes in the CodeWarrior Project

- 11. Under the Libs source group remove the ansiis.lib file
- 12. Right click the Libs source group and click Add Files...
- 13. Browse to the CodeWarrior HCS08 library file directory, typically

```
C:\Program Files\Freescale\CodeWarrior for
Microcontrollers 6.2\lib\hcs08\lib
```

12. Select the ansibim.lib file.



### Changes in the CodeWarrior Project

- 9. Click the *Edit* > *Standard Settings* menu
- 10. Click on the Access Paths on the left pane
- 11. Click on the old QE32 directory and press the Remove button
- 12. On the left pane, click the Compiler for HC08 option
- 13. Click the *Options* button
- 14. Select the Code Generation tab.
- 15. Scroll down and uncheck, then check the *Memory Model* checkbox
- 16. On the radio buttons that appear, select *Banked Memory Model*. Press OK to exit this dialog.
- 17. Press OK on the Standard Settings dialog.

Optimizations	Output Input	Language
Host	Code Generation	Messages
Maximum load fac Minimum number o Minimum load fact Switch off code ge Double is IEEE32 Memory Model MMIL sunport	tor for switch tables of labels for switch tables or for switch tables of labels for switch search tables eneration	8
Do not use CLR fo Qualifier for virtual	or volatile variables in the direct table pointers	page
(C Tiou Memory Mod	el odel	
Small Memory M	Nodel	
Banked Memor	y Model	
Cs08 -DNO_FLOA OnP=g -OnPMNC -V WmsqSd5912	ATMb -Ous -Of -OnB=alr -On VmsgSd1420 -WmsgSd4000 -W	icn -OnCstVar /msgSd4001



### Changes in Processor Expert

- 1. Click the Processor Expert tab in left panel
- 2. Right click the KBI Bean's icon and click the *Bean Enabled* menu item to disable it; it is not needed
- 3. Right click the *TPM\_Prox:Init\_TPM* bean's icon and click the *Bean Enabled* menu item to enable it
- 6. Double click *SM1:SPIMaster* icon to bring up Bean Inspector for this bean
  - Click the dropdown at the top for "Channel" and select SPI1 to resolve the naming conflict
  - Click the dropdown for the input pin and select the option for PTB4 to resolve the naming conflict
- 7. Close the bean inspector (saves changes)

Bean ItemsVisibilityHelp < >			View Reg
Properties Methods Events Comment			
🖌 Bean name	SM1		
🖌 Channel	SPI1	- 501	
Interrupt service/event	Disabled		
Settings			
- 🖌 Bidirectional mode	Disabled	2	
🖃 Input pin	Enabled	2	
- 🖌 Pin	PTB4_TPM2CH1_MIS01	PB4_TPM2CH1_MIS01	
Pin signal			



### **Changes in Processor Expert**

- 8. Under the *CPUs* category, right click the QE128 CPU icon and select *View Target CPU Package.*
- 9. Right click the SCI1 peripheral.
- 10. Select Add Bean/Template. Click yes to add to the other configurations.
- 11. From the resulting menu, select Asynchro Master. This generates the bean with RS232/UART functionality.

PTE

H TPML P

ACMPS

TPM2

Show Peripheral Initialization Show Peripheral Structure

Help on Target CPU Window

Search Related Info in MCU PDF Documentation

AsynchroSe

AsynchroSlav

- 10. Double click the bean icon to open the bean inspector
- 11. Change the name of the bean from *AM1* to *SERIAL*
- 12. Click the ellipsis next to the *Baud Rate* category.
- 13. Set the baud rate to 57600.





### Changes in Processor Expert

- 14. Open the function list for the SERIAL bean and ensure that the GetTxComplete is enabled.
- 16. Under the *CPUs* category, right click the QE128 CPU icon and select *CPU Inspector*.
- 17. Select the *Build Options* tab.
- 18. Select *Banked* for the memory model.
- 19. Ensure that the stack size is 256 bytes or higher.
- 20. Build the project.
- 21. The linker will report an error about running out of allocation space.
- 22. Go back to the CPU inspector and click the circular arrow beside *Generate PRM File* to disable PRM file generation.

- 🛛 M	TurnRxOn
- 🔀 🖪	TurnRxOff
- 🛛 🖪	LoopMode
- 🗹 🖪	SetIdle
- 🔀 🖪	Standby
- 🛛 M	SetDirection
- 🛛 🖪	GetRxIdle
- 🗹 M	GetTxComplete

💊 Bean Inspector Cpu:MC9S08QE128C	:LH	
Bean ItemsVisibility Help < >		
Properties Methods Events Build options	<u>J</u> sed <u>Comment</u>	
Compiler	CodeWarrior HCS08 C Con	npiler
🖌 Generate macros	yes	0
🖂 User initialization		
🚽 🗸 User data declarations	(string list)	
🗁 🖌 User code before PE initialization	(string list)	
User code after PE initialization	(string list)	
✓ Memory model	Banked	-
🗄 Generate PRM file	no	0



### Changes to the Linker Settings

- 1. Click the *Files* tab on the left panel to return to the source browser.
- 2. Under the *Project Settings/Linker Files* source group, double click the *seminar.prm* file to bring up the linker configuration file for this project.
  - We will need to ensure that the banked memory is set up properly for the extra flash on the S08 QE128
- 3. Move the *DEFAULT\_ROM* value to after *PAGED\_ROM* on the line below
- 4. Save the PRM file and re-bulid the project.

NON_BANKED	FAULT ROM, ROM_VAR,	STRINGS INTO	ROM;
PAGED_ROM		✓* routines INTO PPAGE	<pre>which can be banked */ _0,PPAGE_2,PPAGE_4,PPAGE_5,PPAGE_6,PPAGE_7,ROM1;</pre>
NON_BANKED, F	VAR, STRINGS INTO	ROM;	
PAGED_ROM, DEF.	AULT_ROM	✓* routines INTO PPAGE	<pre>which can be banked */ _0,PPAGE_2,PPAGE_4,PPAGE_5,PPAGE_6,PPAGE_7,ROM1;</pre>



#### Lab 3: QE128 (HCS08) Software Overview

### New Program Modes:

- ► Scatter plot
  - Shows the accelerometer's output on a two-axis display
  - Can select which two axes of the accelerometer are displayed
- Data logger for Accelerometer and DMM inputs
  - Can capture data from both inputs
  - Scroll through captured data in a display window
  - Send captured data out to a serial port (use PE Micro USB scope utility)
- ► DMM modes from QE32 are preserved as-is



# Lab 3: QE128 (HCS08) Testing

### DEMOQE Board Jumper Settings:

Accelerometer					
Jumper Pins					
J13	2&3				
J14	2&3				
J15	2&3				
J16	None				

Inputs					
Jumper Pins					
J12	None				
J18	1&2, 3&4				
J11	1&2, 3&4				

System Power					
Jumper Pins					
J3	2&3				
J4	3&4				
J5	3&4, 5&6				

RS232				
Jumper	Pins			
J6	2&3			
J7	2&3			
J8	2&3			

External Clock			Buzzer		IIC Pullups			Analog
Jumper	Pins	Jumper	Pins		Jumper	Pins	Jumper	Pins
J17	1&2, 3&4	J19	1&2		J20	None	J21	None

LEDs				
Jumper Pins				
J9	None			



#### Lab 3: QE128 (HCS08) Testing

# Compile, Run, and Test!

Remove QE32 module



Insert QE128 module



#### Open PE Micro USB Terminal utility





### Lab 3: QE128 (HCS08) Application Features

### Scatter Plot

- ► Increased flash space allows a richer UI experience
- Large bitmap is used to store the scatter plot background image
- Bitmap utilizes paged memory on S08
- Must put accelerometer jumpers J16 on when using accelerometer modes, such as the scatter plot
  - Jumpers on pins 1&2, 3&4, and 7&8

### Datalogger

- Increased RAM allows for storage of DMM/Accelerometer data
- Serial bean functions used in *serialio* HAL module to perform Tx routines



### Lab 3: QE128 (HCS08) Code Highlights

### Serial transmit routines

- ► Note the use of PE bean-generated code in the custom HAL code
- The function, int8 serialio\_write\_string(uint8\_t\* str) provides an example of this
- Open the Processor Expert tab and open the function list for the SERIAL bean to see which of the available functions were used in serialio.c

### Bitmap allocation and display

- The bitmap representing the scatter plot background image was generated using a bitmap to array converter utility provided by the TFT vendor
- ► This array is contained in the *Application/bitmap\_screens.c* source file
- When the red cursor representing the accelerometer deflection needs to be updated, the previous cursor is erased, the bitmap is redrawn in this location only, and the new cursor is written
  - See the uint8 UI\_PaintScatterPlot(...) function in ui.c



#### Lab 3: QE128 (HCS08) Flash Programmability

### Flash can be programmed at a wide rage of voltages

- ► Range of voltages: 1.8V to 3.6V
- Can test this out on the DEMOQE board
  - Turn off power to the board
  - Ensure that the *REG\_VDD* jumper is in place on J5
  - Remove the jumper on J4 from the 3V position (pins 3&4) and place it onto the 2.1V position (pins 1&2)
  - Plug the USB cable into the board
  - Turn on the board
  - Program the device in CodeWarrior and observe that it programs successfully
  - Turn off the board
  - Place the jumper on J4 back onto the 3V position
  - Turn on the board and observe that the demo application still runs



# Lab 3: QE128 (HCS08)

Self-Study Project Enhancement

### Enhancement: Flash Datalogger

- Modify the datalogger program mode so that it transfers logged values into flash once the RAM is full
- ► Will use the IntFLASH peripheral on the MCU
- Utilize the flash programming bean based on the IntFLASH peripheral in Processor Expert to:
  - Set up the flash paging and space allocation in the MCU memory map
  - Enable read/write functions to manipulate flash segments





## LAB4: MCF51QE128



# **51QE128 Overview**

	QE8	QE32	S08QE128	51QE128		
CPU	S08 Up to 20 MHz	S08 Up to 50MHz	S08 Up to 50 MHz	ColdFire V1 Up to 50 MHz		
FLASH	8K Bytes	32K Bytes	128K Bytes	128K Bytes		
RAM	512 Bytes	2K Bytes	8K Bytes	8K Bytes		
ADC	10-ch 12-bit ADC	10-ch 12-bit ADC	24-ch 12-bit ADC	24-ch 12-bit ADC		
ТРМ	2 TPM (3-ch)	2 TPM (3-ch) 1 TPM (6-ch)	2 TPM (3-ch) 1 TPM (6-ch)	2 TPM (3-ch) 1 TPM (6-ch)		
SPI	1 SPI	1 SPI	2 SPI	2 SPI		
SCI	1 SCI	2 SCI	2 SCI	2 SCI		
IIC	1 IIC	1 IIC	2 IIC	2 IIC		
КВІ	8-ch KBI	16-ch KBI	16-ch KBI	16-ch KBI		
Rapid GPIO	NA	NA	NA	Yes		
Others	ICS, RTC, GPIO, BDM					



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### Lab 4: QE128 (Coldfire V1) Device Overview

#### MCU: MCF51QE128

Specs					
CPU	Coldfire V1				
RAM	8k Bytes				
Flash	32k Bytes				
Max Bus Clock	25 MHz				
Max CPU Clock	50 MHz				

 Peripherals:

 ► ADC (24-ch, 12-bit)
 ► SPI (2)
 ► RTC

 ► Comparators (2)
 ► I2C (2)
 ► KBI (16-ch)

 ► SCI (2)
 ► TPM (1x 6-ch, 2x 3-ch)



### Lab 4: QE128 (Coldfire V1) Software Overview

### New Program Mode

- Real-time graph
  - Plots the input signal from the DMM inputs or accelerometer axes in real-time
  - Utilizes the added processing power of the Coldfire to erase and re-draw all points on the screen as fast as data comes in
  - Can capture one screen of data at a time at the push of a button
- ► Oscilloscope
  - Implements an oscilloscope function that can operate on DMM inputs or accelerometer axes
  - Triggers on the rising edge of a signal throughout the input voltage range, configurable by the user
  - User can set the timebase in terms of sampling rate in milliseconds



• • • • • • • 0  $\bullet \bullet \bullet$ Freescale Accelerometer

### Lab 4: QE128 (Coldfire V1) New Graphic User Interface



Oscilloscope Mode

Accelerometer Graph Mode



### Lab 4: QE128 (Coldfire V1) CPU Comparison

MC9S08QE128				
CPU	HCS08 (8-bit)			
Address Bus	16-bit			
Data Bus	8-bit			
Instruction Set	HCS08			
Interrupt Support	32 interrupts, no nesting			

MCF51QE128					
CPU	Coldfire V1 (32-bit)				
Address Bus	24-bit				
Data Bus	32-bit core, 8-bit peripheral				
Instruction Set	Coldfire V1 Rev. C				
Interrupt Support	256 interrupts, nesting supported				



#### Lab 4: QE128 (Coldfire V1) CPU Comparison

### **CPU Registers:**

#### HCS08



#### **Coldfire V1**





### Changes in Processor Expert

- 1. Click on Change MCU/Connection
- 2. Select MCF51QE128 from the list
  - ► Ensure that *P&E Multilink Cyclone Pro* is selected
  - Ensure that the Backup project before changes box is unchecked
- 3. Click the Processor Expert tab in left panel
- 4. Right click the CPU bean's icon and select the CPU Inspector option
- 5. Select the properties tab
- 6. Set the Internal Oscillator Frequency to 39 (kHz)
- 7. Set the Internal Bus Clock to 19.968 (MHz)

seminar.mcp
🕪 P&E Multilink/Cyclone Pro
Files Link Order Targets Processor Expert

E HC08	Connections
E-HCS08	Full Chip Simulation
E RS08	P&E Multilink/Cyclone Pro
	CEv 1 Open Source BDM
HIMCESTAC Family	
MCF51QE128	
MCF510E64	L
MCF510E96	Connect to P&E BDM Multilink (USB and
+ MCF51JM Family	parallel) or P&E Cyclone Pro (USB, Serial
Flexis	and TCP/IP).
	Backup project before changes.



### Changes in Processor Expert

- 8. Right click the KBI Bean's icon and click the *Bean Enabled* menu item to disable it; it is not needed
- 9. Right click the *TPM\_Prox:Init\_TPM* bean's icon and click the *Bean Enabled* menu item to enable it
- 10. Right click the *TPM2\_HighSpeed:Init\_TPM* bean's icon and click the *Bean Enabled* menu item to enable it
- 11. Double click the TPM2\_HighSpeed bean to open the Bean Inspector
- 12. Press the plus sign (+) beside the *Channels* heading to add a second TPM channel
- 13. Set the Capture/Compare Device to TPM21 and the Mode to Output compare
- 14. Set interrupt priorities for all of the TPM channels to remove the errors
- 15. Enable the interrupt for this channel and name it TPM2\_CompareISR\_1
- 16. Since the Coldfire core supports interrupt priorities, these need to be set for all interrupts in the TPM bean

### Changes in Processor Expert

- 17. Double click the SERIAL bean to open the Bean Inspector
- 18. Click the ellipsis beside the *Baud Rate* option to open the baud rate dialog
- 19. Change the tolerance to 2% to remove the error.
  - The resultant baud rate is only 0.01% over the original tolerance for the S08 QE128, which is marginal
- 20. Double click the SPI bean to open the Bean Inspector
- 21. Click the ellipsis to set a new shift clock rate.
- 22. Set the new shift clock rate to 9.984 MHz, the last option in the dropdown list.



### Changes in the CodeWarrior Project

- 1. Click the *Files* tab on the left panel
- 2. Remove both *programctl* files by right clicking them and selecting *Remove*
- 3. Right click on the Application source group and click Add Files...
- 4. Browse from the top-level directory to: <top\_level>\src\cf\qe128 and select the programctl files
- 5. Click the *Edit* > *Standard Settings* menu
- 6. Click on the Access Paths on the left pane
- 7. Click on the old s08\qe128 directory and press the Remove button
- 8. Press OK on the Standard Settings dialog
- 9. Open up the Libs source group and remove the ansibim.lib file





### Changes in the CodeWarrior Project

- 10. Open Events.c. This file contains all Beans-generated interrupt service routines.
- 11. Insert the following lines into the TPM2\_CompareISR\_1 at the bottom of the file:
  - This allows the compare interrupt to sample data as part of the fixed frequency sampling code in the signal acquisition module (signalacq)

```
/*
         _____
**
     Interrupt handler : TPM2_CompareISR_1
**
¥¥
**
     Description :
        User interrupt service routine.
     Parameters : None
              : Nothing
     Returns.
    ISR(TPM2_CompareISR_1)
 /* Write your interrupt code here ... */
 //clear compare flag
 TPM2C1SC CH1F = 0;
 //call sampling function from signalacq module
 sample data isr();
```



### Changes in the CodeWarrior Project

- 10. Open seminar.c. This file contains the main function and all initialization code.
- 11. Insert the highlighted line into main():
  - We now need to initialize the signal acquisition module for use with the fixed frequency sampling code.

void main(void)
{
 /\* Write your local variable definition here \*/
 /\*\*\* Processor Expert internal initialization. DON'T REMOVE THIS CODE!!! \*\*\*/
 PE\_low\_level\_init();
 /\*\*\* End of Processor Expert internal initialization.
 /\* Write your code here \*/
 //initialize application modules
 petrl\_init();
 signalacq\_init();|
 App\_Init();
 //start program\_control (will never exit)
 start\_program\_ctrl(PROGRAM\_MODE\_NORMAL\_DMM\_CONFIG);





### Lab 4: QE128 (Coldfire V1) Software Overview

### New Program Modes:

- ► Real-time graph
  - Plots the input signal from the DMM inputs or accelerometer axes in real-time
  - Utilizes the added processing power of the ColdFire to erase and re-draw all points on the screen as fast as data comes in
  - Can capture one screen of data at a time at the push of a button
- Oscilloscope
  - Implements an oscilloscope function that can operate on DMM inputs or accelerometer axes
  - Triggers on the rising edge of a signal throughout the input voltage range, configurable by the user
  - User can set the sampling interval in milliseconds
- All previous program modes are preserved as-is



#### Lab 4: QE128 (Coldfire V1) Testing

## Compile, Run, and Test!

#### Insert QE128 CF module



#### Insert QE128 CF module



#### Open PE Micro USB Terminal utility





### Lab 4: QE128 (Coldfire V1) Code Highlights

### Fixed Frequency Sampling (Signal Acquisition Module)

- All sampling functions have the same signature one function pointer stores the currently active sampling function
  - **Pointer definition:** uint16 (\*sample\_fn)(void);
- Sampling function externally set with enumerated input types using the function, int8 assign\_sampling\_input(sampling\_input\_t sample\_input)
- Sampling function called from the ISR for TPM2's Ch. 1 compare ISR generated by the TPM2\_HighSpeed bean
  - **ISR contained in Events.c, browse to:** ISR(TPM2\_CompareISR\_1)
  - Main processing in ISR done in sample\_data\_isr()
- Cannot modify signal acquisition module's parameters while a transfer is in progress
  - sampling\_in\_progress flag implements this functionality



### Lab 4: QE128 (Coldfire V1) Code Highlights

Graphing UI Widgets (User Interface Module)

- Operate on buffered ADC data
- ► Can draw an arbitrary number of points on-screen
- Can operate in free-running mode (single point updates) or buffered mode
  - This can be seen in the graph and oscilloscope functions
- Axis labels and tigger level indicator are also part of this widget; can be set and re-drawn independent of the graph portion of the widget



Power Consumption Comparison

### 32-bit Can be lower power than 8-bit

- It's not simply about processor speed or instruction size, but execution efficiency of those instructions
- ► Compare:
  - HCS08 core has one 8-bit accumulator and one 16-bit index register
  - Coldfire V1 core has eight dedicated 32-bit address and data registers
- **Example 1**: Compare the disassembly of highlighted line of code, below

```
C code from sample_data_isr function in signalacq.c
void sample_data_isr(void)
{
    //sample data with sampling function
    sample_buffer[sample_count] = sample_fn();
    ...
}
```



**Power Consumption Comparison** 

### 32-bit Can be lower power than 8-bit

#### Coldfire V1 disassembly of signalacq.c

```
Summary:
  586: void sample_data_isr(void)
;
   587: {
   588:
          //sample data with sampling function
   589:
          sample_buffer[sample_count] = sample_fn();
                               sample data isr:
0x0000000
                               sample data isr:
0x00000000
            0x206D0000
                                      movea.l
                                               _sample_fn(a5),a0
0x00000004
            0x4E90
                                      jsr
                                                (a0)
0x0000006
            0x73AD0000
                                      mvz.b
                                                _sample_count(a5),d1
A0000000x0
            0 \times 41 ED0000
                                      lea
                                                sample buffer(a5),a0
0x0000000E
            0x31801A00
                                               d0,(a0,d1.1*2)
                                      move.w
```



- 3 move instructions
- 1 jump instruction
- 1 load instruction



**Power Consumption Comparison** 

### 32-bit Can be lower power than 8-bit

#### HCS08 disassembly of signalacq.c

589:	sample	e_buffer[sample_	count]	= sample_fn();
0000	ce0000	[4]	LDX	sample_count
0003	58	[1]	LSLX	
0004	89	[2]	PSHX	
0005	320001	[5]	LDHX	<pre>sample_fn:1</pre>
8000	c60000	[4]	LDA	sample_fn
000b	8b	[2]	PSHH	
000c	8b	[2]	PSHH	
000d	8b	[2]	PSHH	
000e	ac000000	[8]	CALL	_CALL_STAR08_FAR
0012	8b	[2]	PSHH	
0013	8c	[1]	CLRH	
0014	9f	[1]	TXA	
0015	9eee02	[4]	LDX	2,SP
0018	d70001	[4]	STA	<pre>@sample_buffer:1,</pre>
001b	86	[3]	PULA	
001c	d70000	[4]	STA	<pre>@sample_buffer,X</pre>

Summary:

Х

- 1 shift instruction
- 1 jump instruction
- 4 load instructions
- 5 push (stack) instructions
- 1 pull (stack) instruction
- ▶ 1 clear instructions
  - 1 transfer instruction

#### Three times as many instructions as the CFV1



**Power Consumption Comparison** 

### 32-bit Can be lower power than 8-bit

- **Example 2**: Faster execution time does not necessarily mean more power
  - Less time in run-mode means less total power consumption
  - E.g., Doing the same operation in half the time on a fast CPU is equivalent to taking twice as long despite using half the wattage on the slow CPU
  - Area under the power curve represents total power consumed





### Lab 4: QE128 (Coldfire V1) Self-Study Project Enhancement

### Enhancement: Spectrum Analyzer

- Both the oscilloscope and the real-time graph program modes operate on buffered data
- Write code that captures data at a fixed sampling interval by using the fixed frequency sampling functions in the signal acquisition module
- Run an FFT algorithm on this data to generate the frequency spectrum data
- Plot this processed data on-screen in a similar way to how it has been done with the oscilloscope and real-time graph program modes
  - Can modify the graph widget to interpolate points using lines instead of drawing single dots



## Low Power Resources




# **Low Power Application Notes & Training**

#### •Application Notes

- •AN3460 Low Power Design enabled by MC9S08QE128 & MCF51QE128 MCUs
- •AN3629: Migrating from the 9S08QE32 to the MCF51QE32
- •AN3502: Differences between the TI MSP430 and QE128
- •AN3506: Migrating from TI's MSP430 to the 9S08QE128 or MCF51QE128
- •AN3467: Using Processor Expert with Flexis MCUs
- •AN3464: Migrating code between ColdFire V1 and V2
- •AN3466: Differences Between a Cortex M3 Processor and the MCF51QE128
- •QRUG QE128 (QE128 Peripheral Module Quick Reference Guide)

#### •Flexis QE Virtual Lab @ http://www.techonline.com/product/virtualab/202200251



•Online training presentations @ www.freescale.com/flexis



# **Flexis QE Family Development Tools**

ΤοοΙ	Resale Price (\$)	MCUs Supported	Comments
EVBQE128	325	MC9S08QE128/96/64/32 MCF51QE128/64/32	Evaluation board for in-depth application development. Contains socket to allow evaluation of MC9S08QE or MCF51QE devices
DEMOQE128	99	MC9S08QE128/96/64/32 MCF51QE128/64/32	DEMOQE128 board + MC9S08QE128 daughter card + MCF51QE128 daughter card
DEMO9S08QE32	69	MC9S08QE32/16	DEMOQE32 board + MC9S08QE32 daughter card
DEMO9S08QE8	69	MC9S08QE8/4	DEMOQE8 board + MC9S08QE8 daughter card
DC51QE128	10	MCF51QE128/64/32	MCF51QE128 daughter card. Use with DEMOQE128
DC9S08QE128	10	MC9S08QE128/96/64	MC9S08QE128 daughter card. Use with DEMOQE128
DC9S08QE32	10	MC9S08QE32/16	MC9S08QE32 daughter card. Can be used with DEMO9S08QE8, DEMO9S08QE32, & DEMOQE128 boards
DC9S08QE8	10	MC9S08QE8/4	MC9S08QE8 daughter card. Can be used with DEMO9S08QE8, DEMO9S08QE32, & DEMOQE128 boards



# **MC9S08LL16** Development Tools

#### Cost-effective development kits

- DEMO9S08LL16 \$69 MSRP
- DEMO9RS08LA8
   \$59
   MSRP
- DEMO9RS08LE4 \$59 MSRP
- Integrated USB-to-BDM interface
  - No USBMULTILINKBDME required \$99 savings!
- Integrated USB-to-BDM circuit
  - In-circuit debugging & Flash programming
  - Without emulation requirements of serial monitors or other debugging techniques in the industry.
- Demo board can be powered by the USB circuit
  - No need for external power supply.

#### CodeWarrior Development Studio for Microcontrollers v6.2

- Complimentary Special Edition with compiler sizes of 32K
- Single tool suite that supports software development for future migration opportunities for both 8-bit or 32-bit and includes rapid application development tool, Processor Expert
- Online training, webcast, technical documentation and application notes available at <u>www.freescale.com/lcd</u>







## Freescale MicroSelector Finding the right Freescale MCU for your design

#### Enables you to:

### http://www.freescale.com/microselector

•Find the best fit - filter by features in our wide variety of controller solutions:

•8-bit products (RS08, HC08 and HCS08 families)

- •16-bit products (DSC and S12X families)
- •32-bit products (ColdFire, i.MX and Power)

•Find package and temperature range offerings.

•Documentation - read collateral for each family.

•Visit the Product Page

#### Using MicroSelector:

- 1) Download Freescale MicroSelector Installer.
- 2) Unzip and execute the file.
- 3) Open Freescale MicroSelector.
- 4) Choose Product Type: Microcontroller / Digital Signal Controller / Microprocessor
- 5) Navigate to find information

	13	MICrose	ector	version	Rev22.04	.1	select	or update v	web page			₽ fr	eesca semicondu
ype	Select features :					os	Voltage	Temp range		Pin count available			
1CU	SPI	SCI/UART	IIC	Comp	ADC	Timer	• uCLINUX	<ul> <li>below 1.8v</li> </ul>	• 0 to 70	o 6 pin	• 48 pin • :	L44 pin 💿 324 pi	in • 672 pin
DSC	PWM	CAN	LCD	USB	Ethernet	VLP	LINUX	• 1.8 to 3.6v	<ul> <li>-20 to 85</li> </ul>	• 8 pin	• 52 pin • 1	160 pin • 360 pi	n • 740 pin
IPU	LIN	RTC	Co-Pro	Crypto	DMA	SDIO	• WINCE Other	0 1.8 to 5.5v	-40 to 85	• 15 pin	• 64 pin • 1	L/6 pin • 388 pi L96 pin • 404 pi	n • 783 pin in • 1023 pin
	SSI	IIS	PCI	SATA	FBI	PCMCIA	<u> </u>	• 3.0 to 3.6v	• -40 to 125	• 24 pin	•81pin •3	208 pin • 416 pi	'n
telp	DDRC	DSPHAV						• 3.0 to 5.5v	$\square$	• 28 pin	• 100 pin • 2	225 pin • 457 pi	n
L	DDRC		d					• 4.5 to 5.5v		• 32 pin	• 112 pin • 2	256 pin • 516 pi	n
			Clear				Mouse	Action : Ou	ck View 🔻	• 44 pin	• 128 pin • 2	289 pin • 668 pi	in
	0010300	MC9508QD											
		MC9S08QA											
			MC9508QG										
			MC95085H										
			MC9508SG										
			68HC908QB	/C									
				68HC908JE	wc/a								
				68HC908G	Z								
				MC9S08RE	/RG								
				MC9208GB	GI								
					MCOCORAN	u .							
				MC9508AC	MC9S08AV	v							



# LCD Hardware <a href="http://www.display3000.com">www.display3000.com</a>

► The LCD board used in the DMM design is DEMOQE128TFT

- Price \$78
- Available from <u>www.display3000.com</u>
- 176x132 64k colour plug-in LCD module
- Kit includes
  - Free license of E-S030 graphics converter software
  - Board schematics
  - CD with heavily commented C (CodeWarrior) software showing you everything you can do with the display
  - Detailed documentation about how to use/program and details on sample s/ware routines (more than 50 pages)





# What did I learn?

# Goal:

• I developed a scalable handheld battery operated product

# **Objectives:**

- I was provided with an understanding of Freescale's low power solutions
- I was educated on the benefits of designing products based on Freescale devices
- I was provided with the techniques required to design a low power, scaleable handheld product with a rich human-machine interface



# Thank you







