

# 功率半导体器件与功率集成电路

## — — 现状及展望

电子科技大学

张 波

[zhangbo@uestc.edu.cn](mailto:zhangbo@uestc.edu.cn)

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功率半导体概述

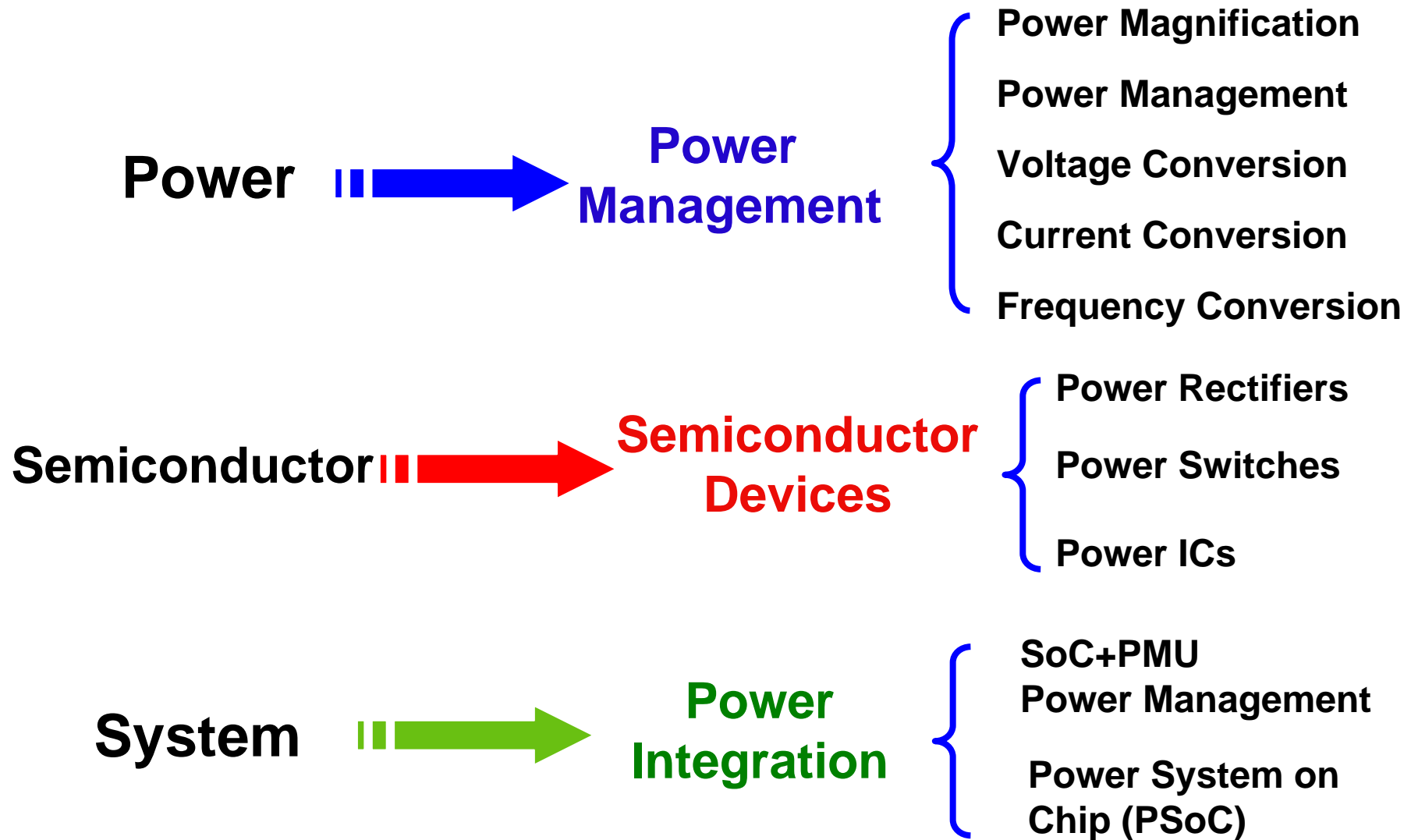
2

功率半导体发展趋势分析

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我国功率半导体发展现状

# 功率半导体概述 - 定义



# Traditional power semiconductor devices

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**Power Semiconductor Devices**



**Power Rectifier**

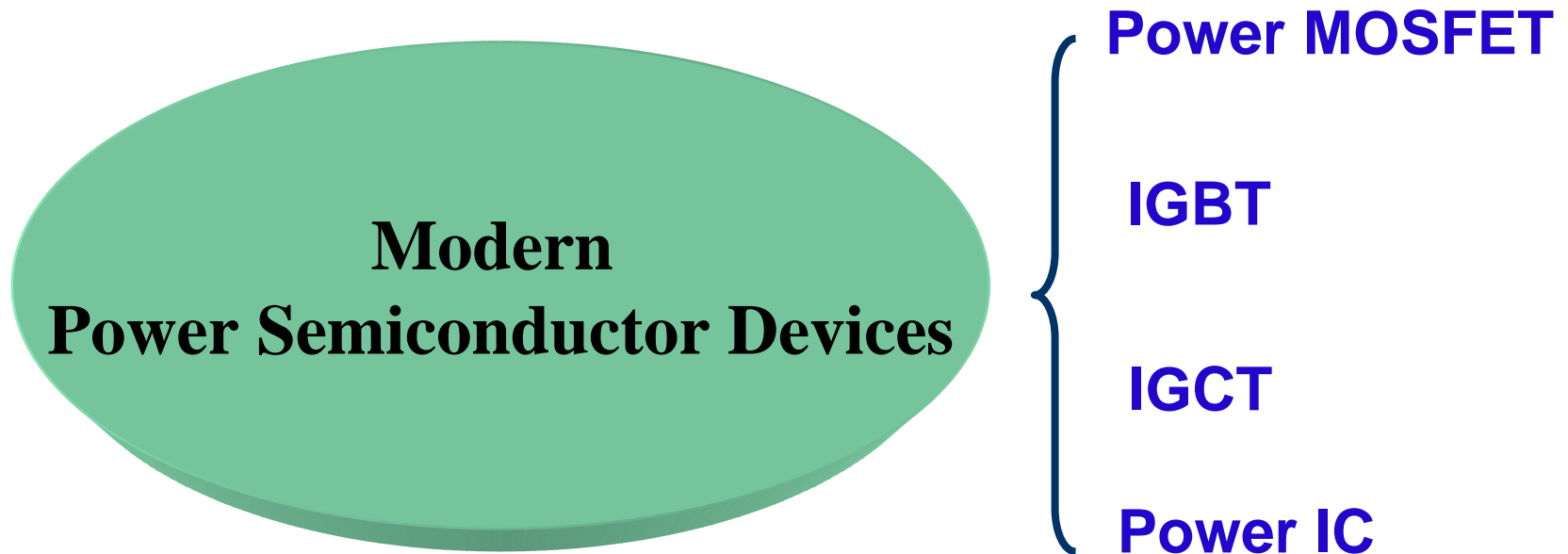
**Power Bipolar Transistor**

**Thyristor**

**Industry Application**

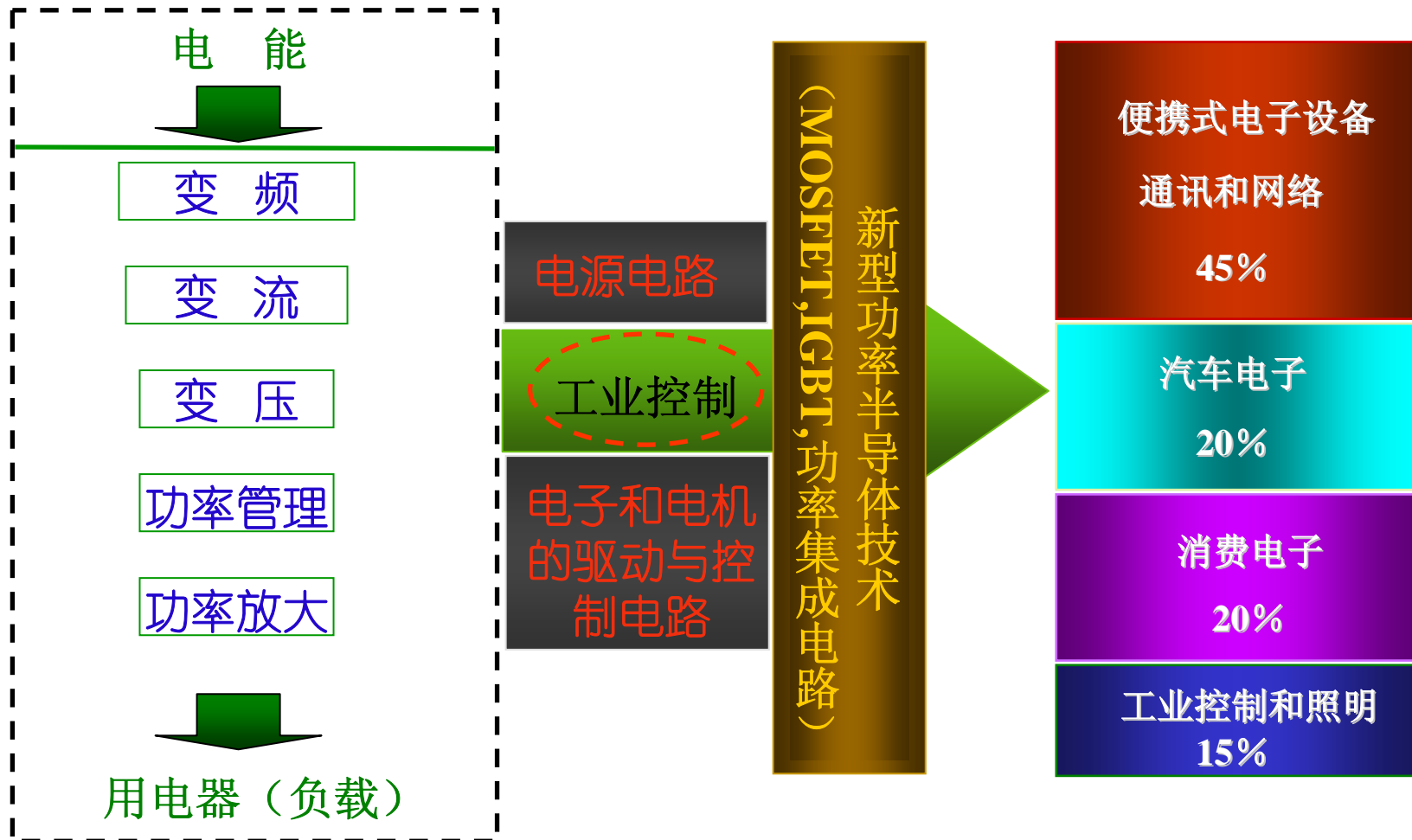
# Modern power semiconductor devices

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# Applications

功率半导体是一门更好利用电能的科学，由于新型功率半导体技术的发展，它的应用范围从工业控制延伸到信息电子



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## 二. 功率半导体发展趋势分析

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2.1 半导体技术发展蓝图

2.2 功率半导体器件发展趋势

2.3 功率半导体集成技术发展



## 2.1 半导体技术发展蓝图

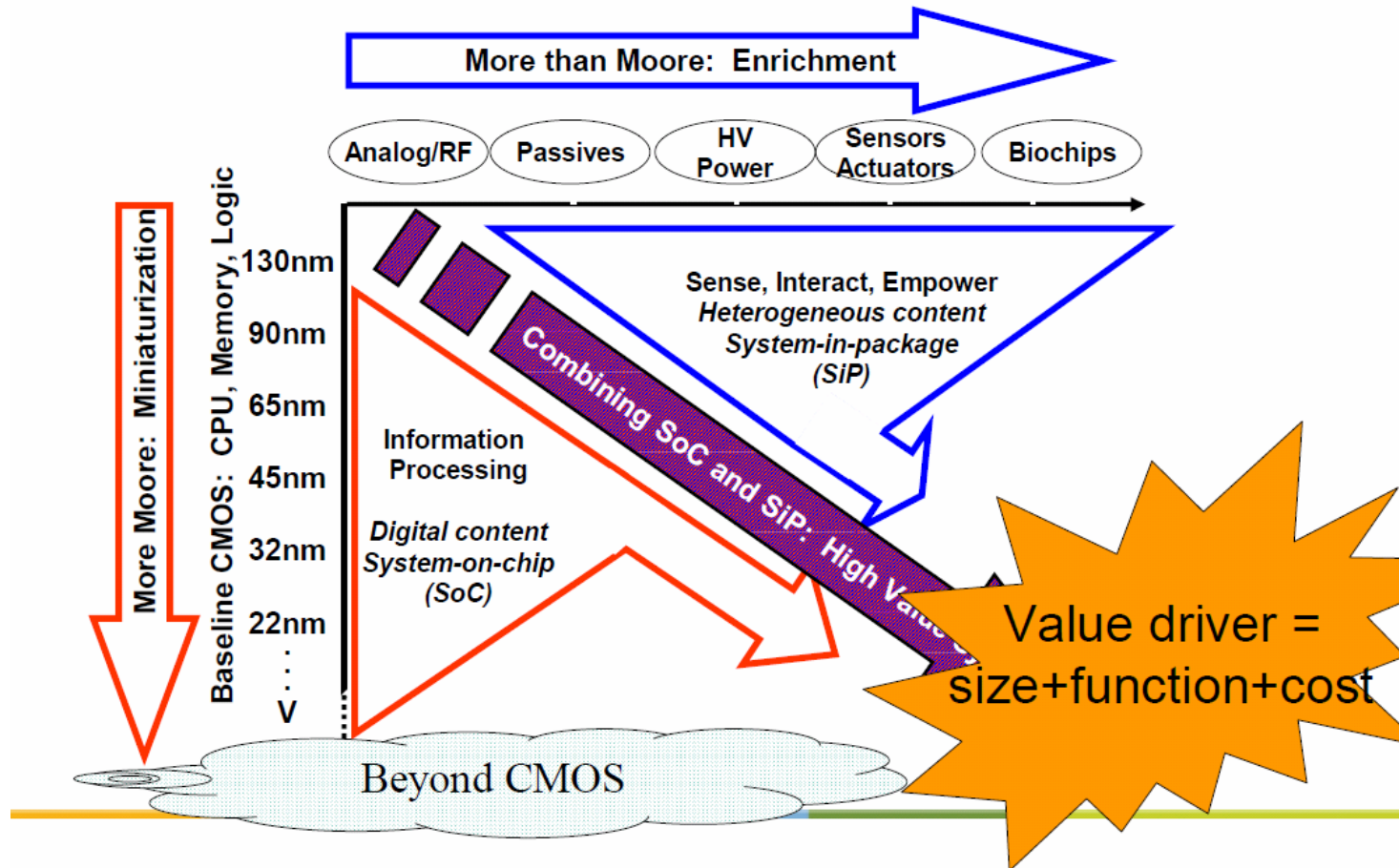
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**(1) More Moore**

**(2) More than Moore**

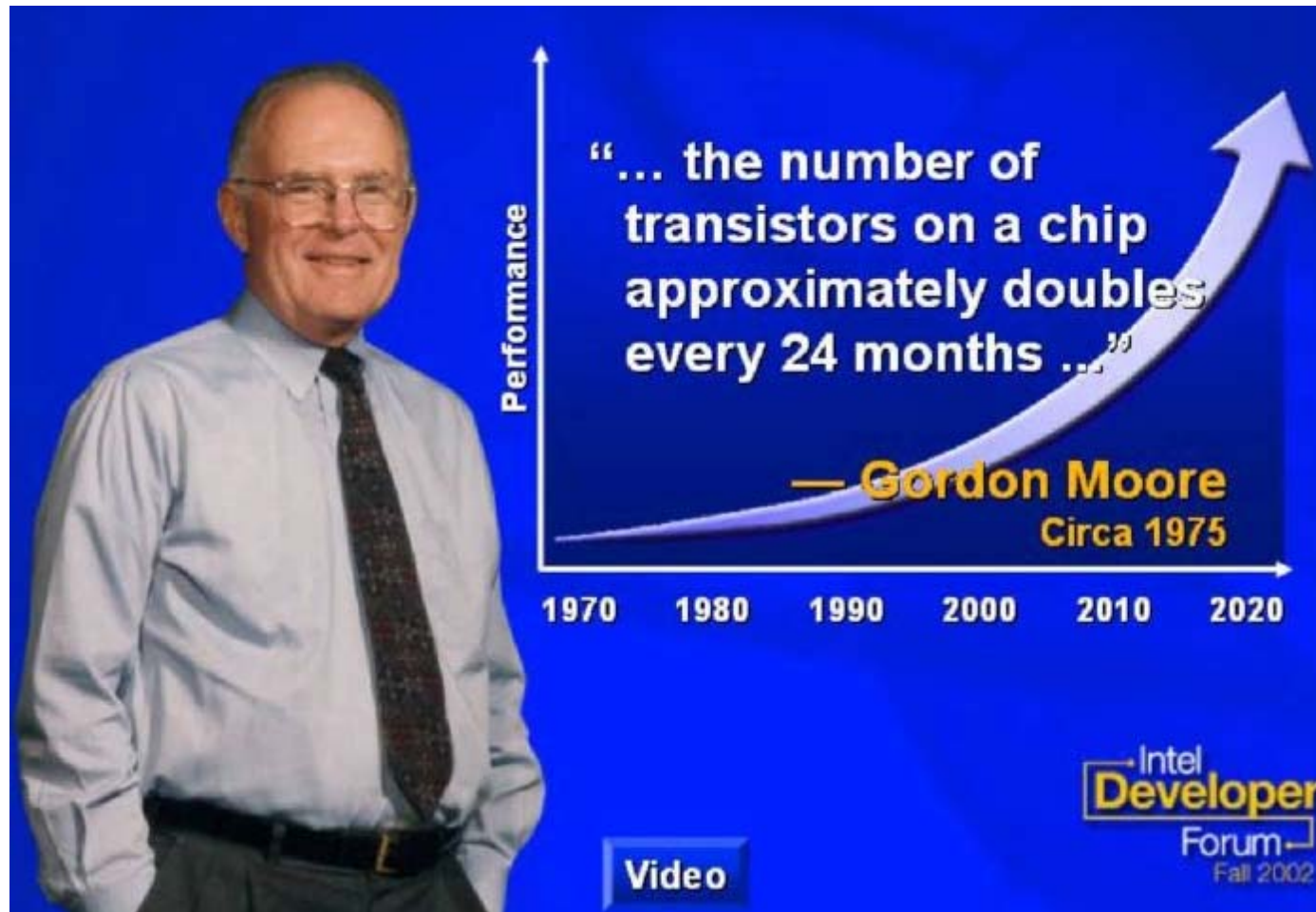
## 2.1 半导体技术发展蓝图

### The New Landscape of Nanoelectronics Tech: Moore's Law & More than Moore

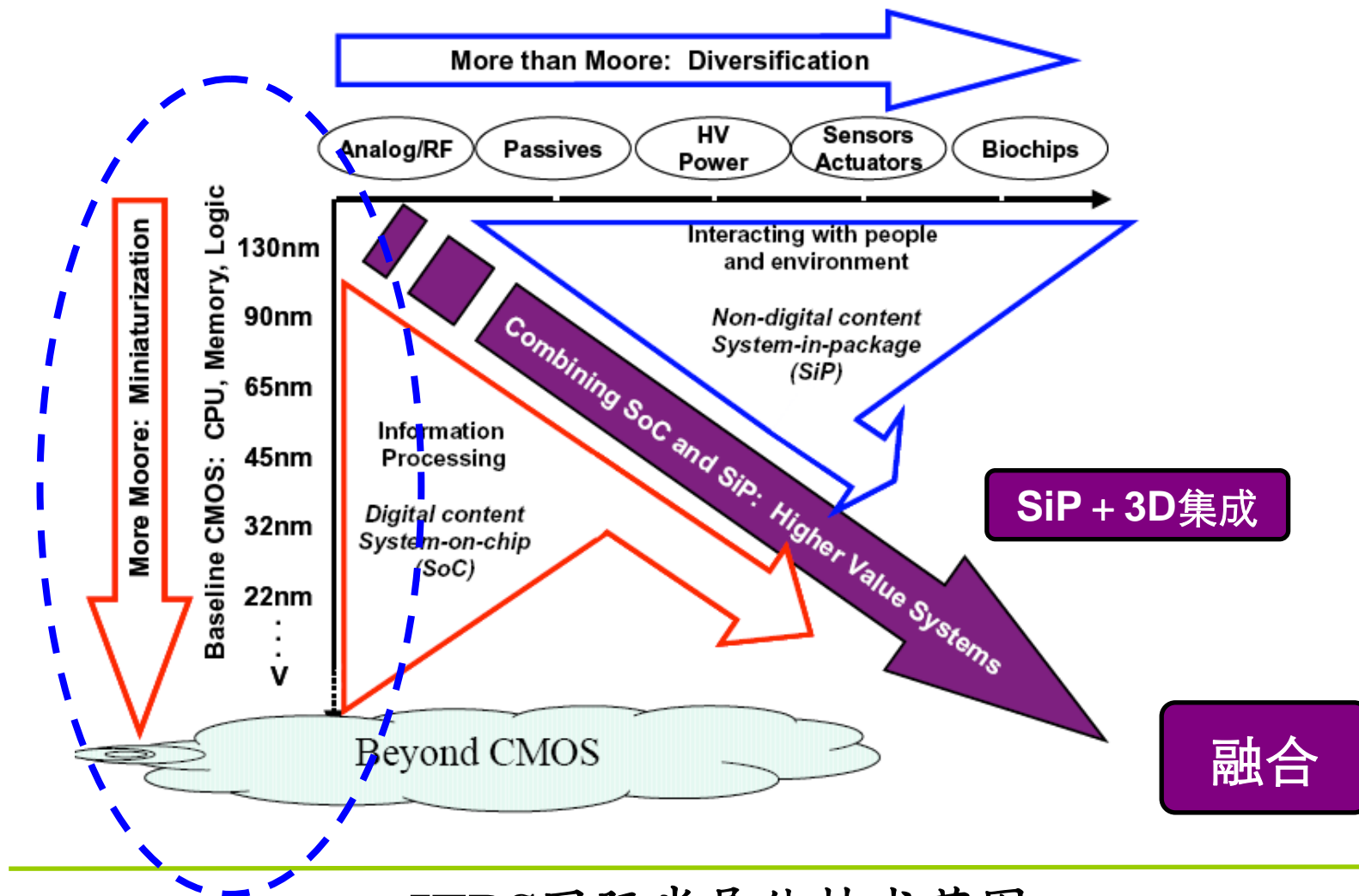


## 2.1 半导体技术发展蓝图

### The Moore's Law

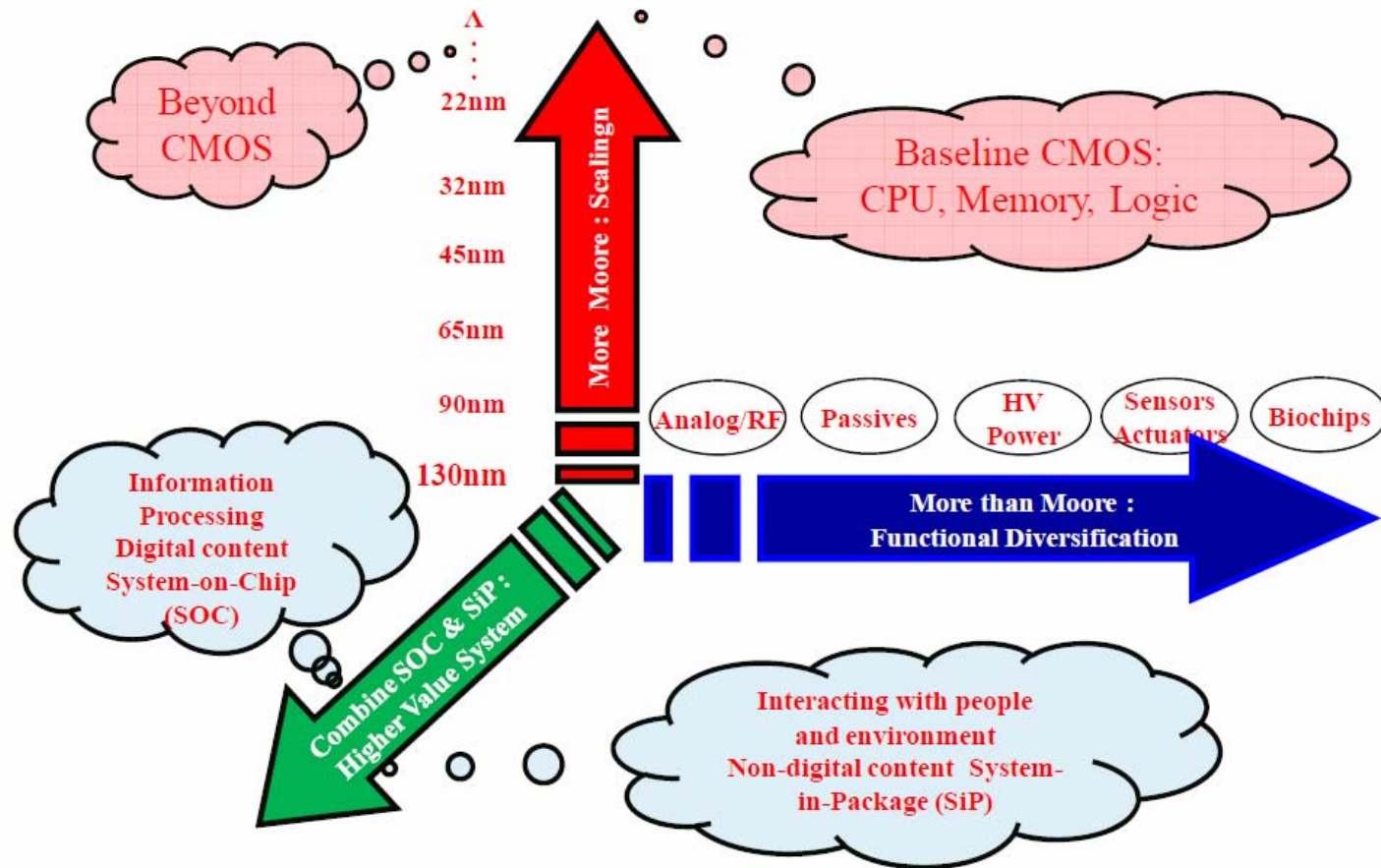


## 2.1 半导体技术发展蓝图



ITRS国际半导体技术蓝图

## 2.1 半导体技术发展蓝图



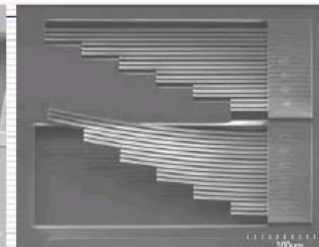
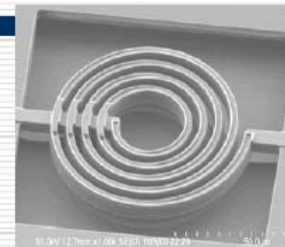
ITRS国际半导体技术蓝图

# More Than Moore

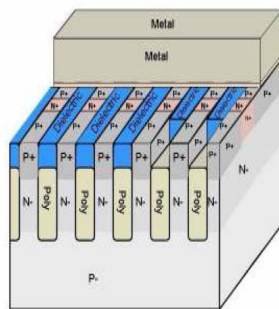
## More Than Moore



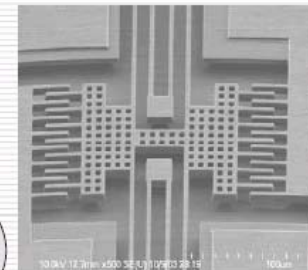
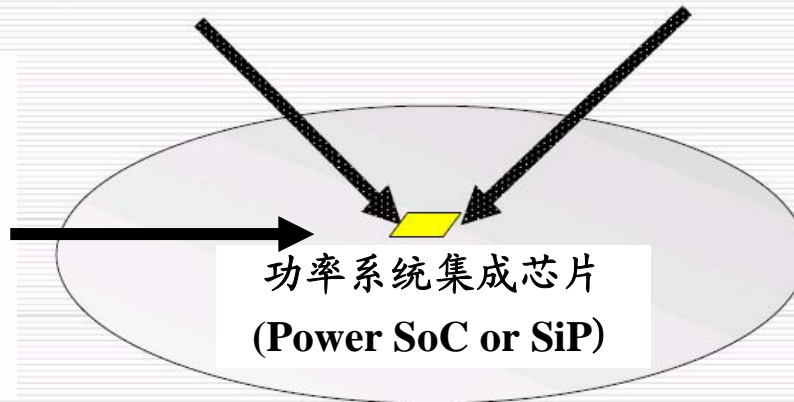
傳統類比、數位、射頻  
電路晶片設計與製造



微機電機械結構整合製造



功率器件



## 2.2 功率半导体器件发展趋势

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- (1) 新结构 (新机理)
- (2) 新材料
- (3) 更多功能的集成

# Power Rectifier

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New material

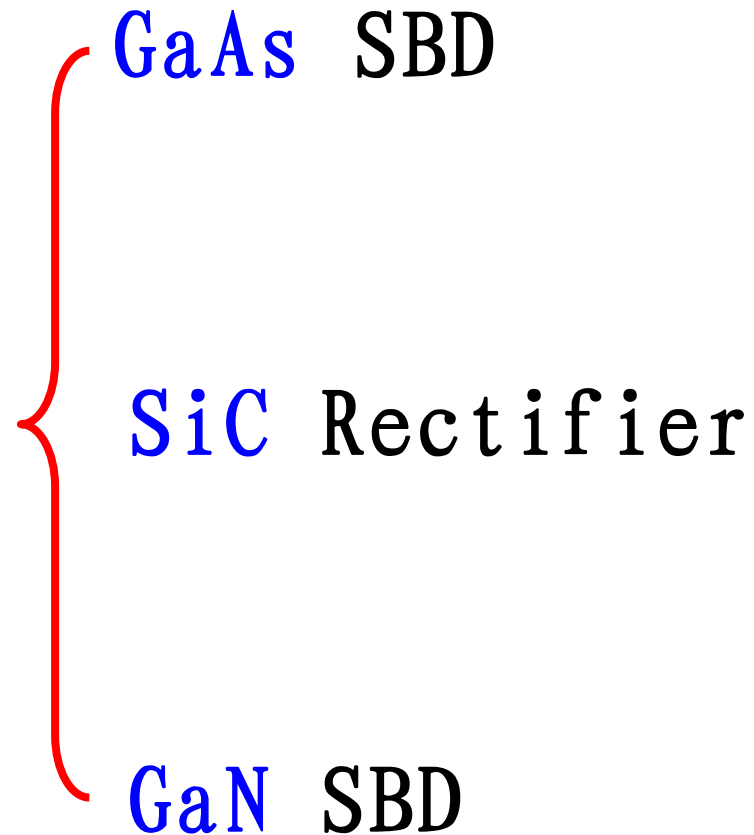
New Structure

New Mechanism



# Power Rectifier Based on New Material

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# Power Rectifier Based on New Structure

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JBS、MPS、TMBS、TMPS



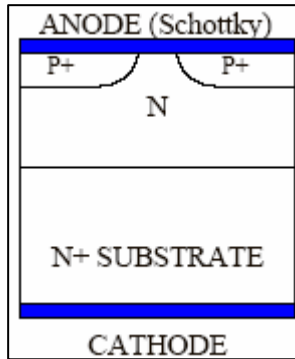
**Merge the advantages of PiN diode and schottky barrier junction.**

SSD、SPEED、SFD、ESD、BJD

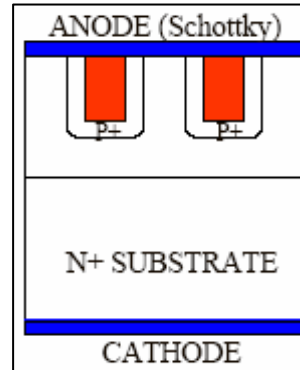


**Optimize the exceeding carriers and their extracting path.**

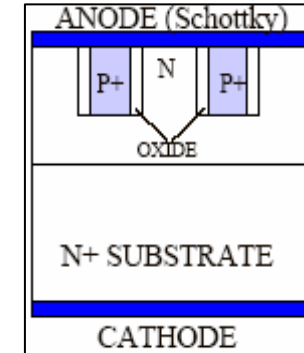
# JBS/MPS Series



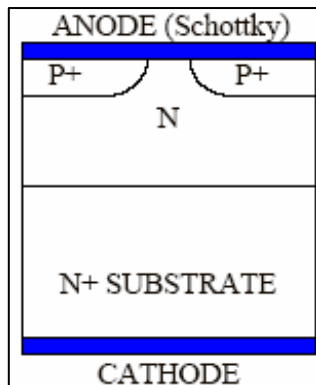
**Si JBS Rectifier  
(1980)**



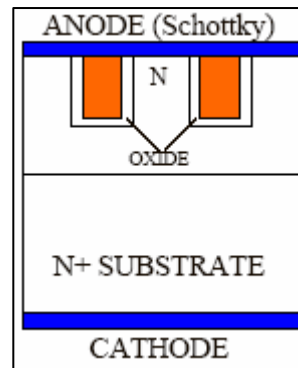
**Si TJBS Rectifier  
(1990)**



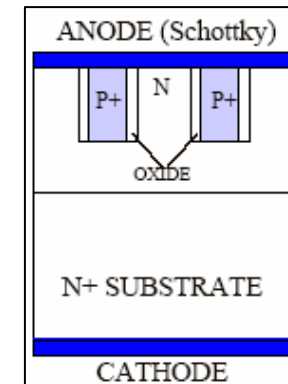
**Si TSOX JBS Rectifier  
(1998)**



**Si MPS Rectifier  
(1987)**

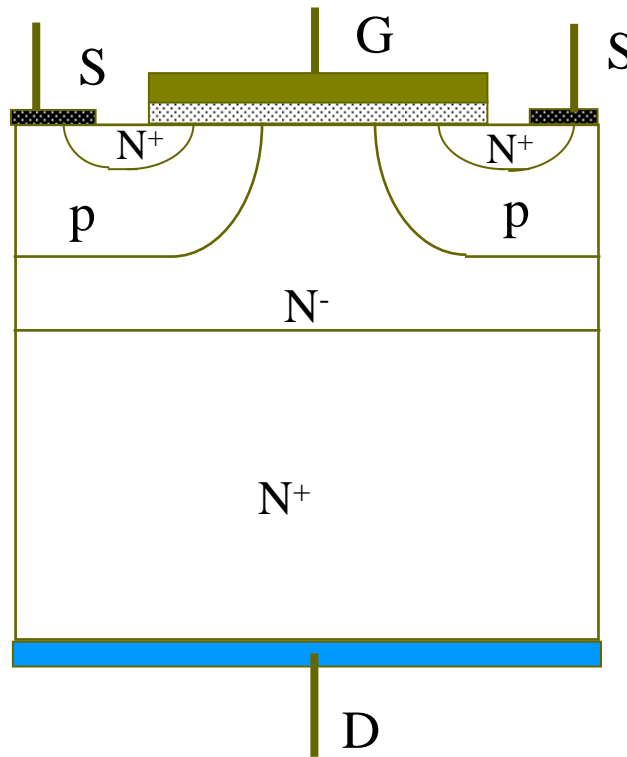


**Si TMPS Rectifier  
(1990)**



**Si TSOX MPS Rectifier  
(1998)**

# Synchronous Rectifier



Si DMOS Synchronous rectifier (SR)

# 功率双极晶体管

## Power Bipolar Transistor

1950s

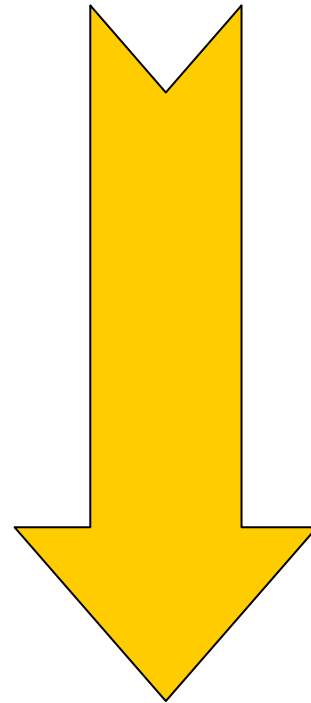


1980s

Ge



Si



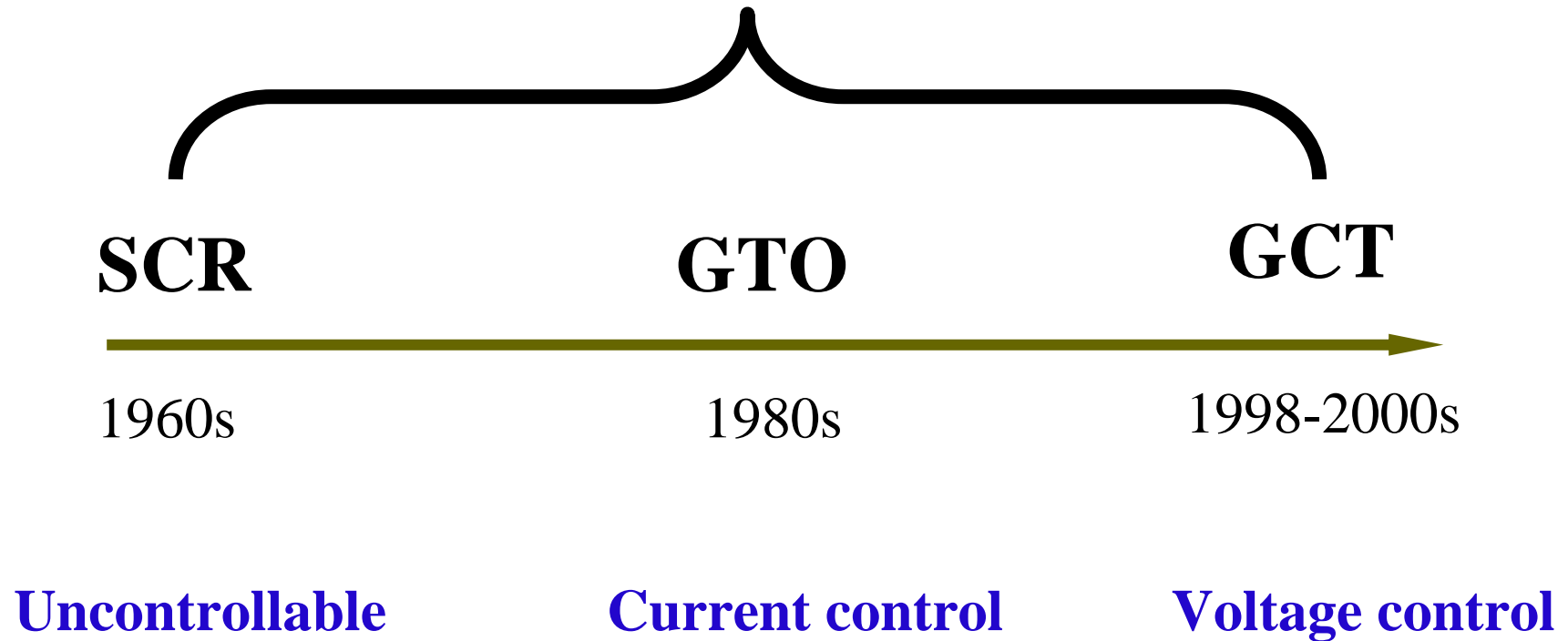
**Maturity**  *SiC*

GTR: 600A/150V、400A/550V、50A/1000V

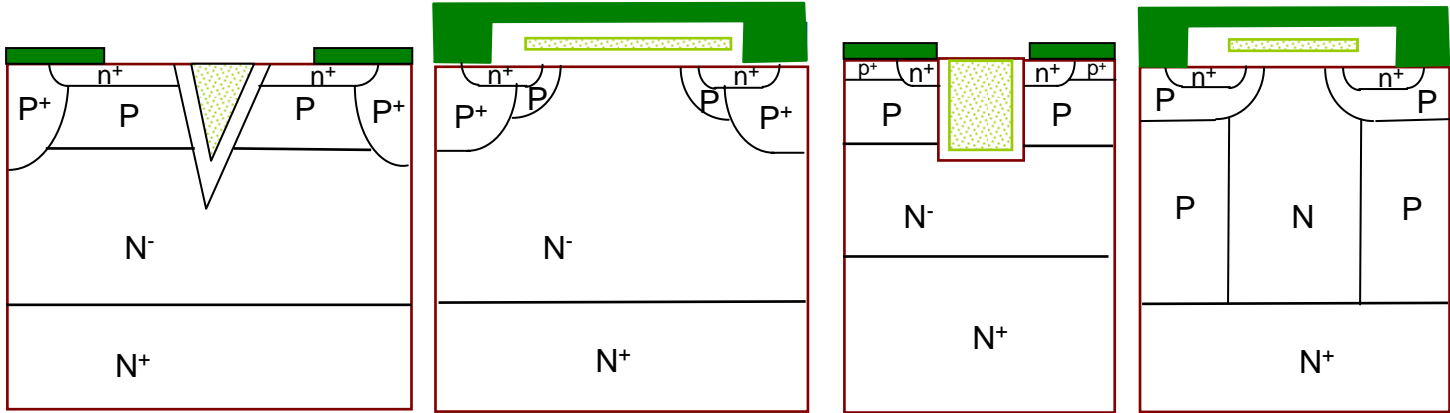
# Thyristor

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## Thyristors



# Power MOSFET



40 μ m

**VVMOS**

1975

20 μ m

**VDMOS**

1980

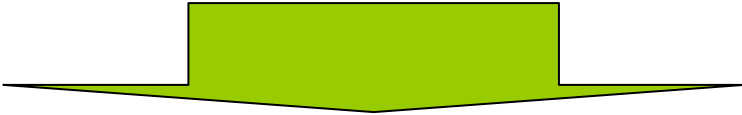
6 μ m

**Trench MOSFET Super Junction**

1990

1997

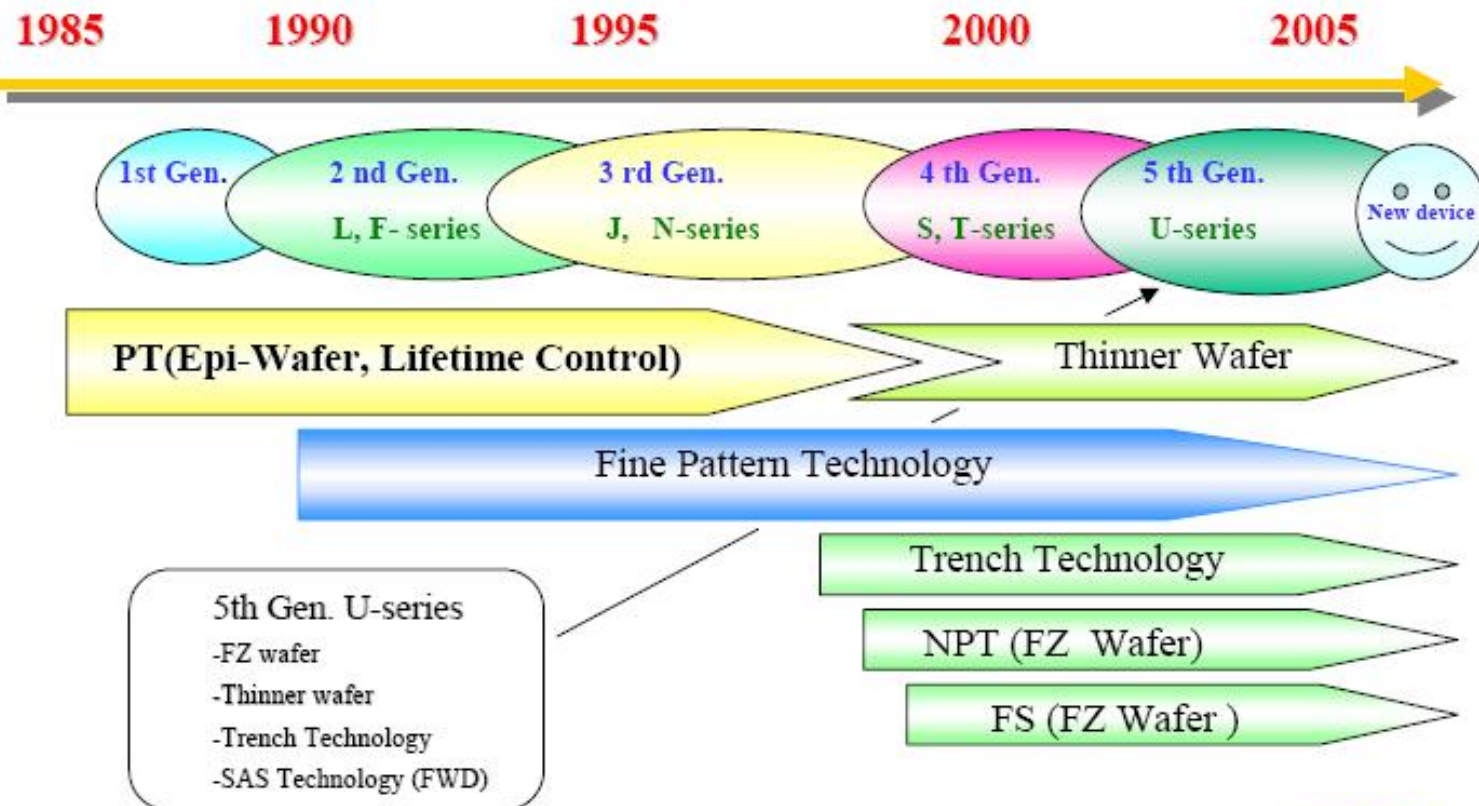
➔ 0.18 μm



- **10 μ m to VDSM design rule: 120M Cells/inch<sup>2</sup>(Gen-8) HEXFET )**
- **60 V device: 7 mΩ-cm<sup>2</sup> to 0.75 mΩ-cm<sup>2</sup>(normal structure)**

# IGBT

## Trend of Fuji's IGBT chips



*Quality is our message*

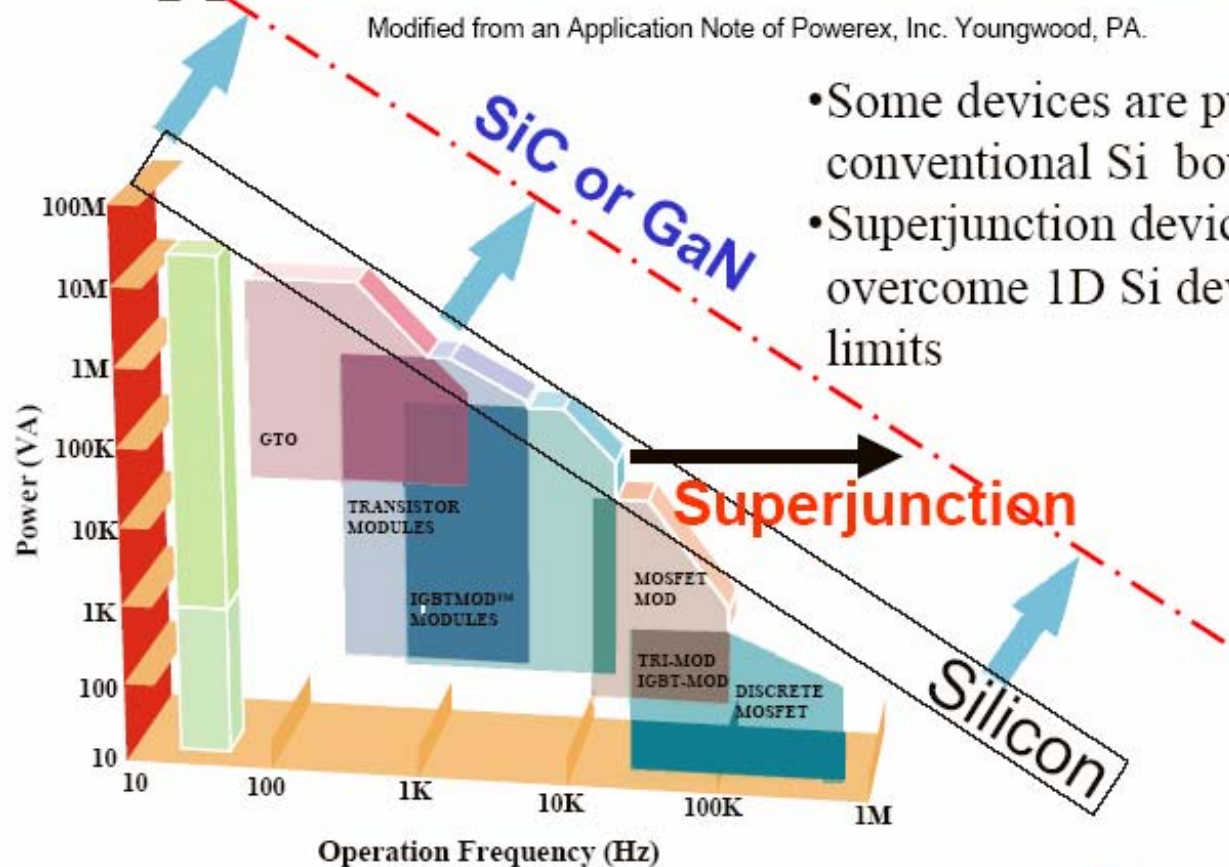




# 新材料 - 宽禁带半导体

## Applications of Power Devices

Modified from an Application Note of Powerex, Inc. Youngwood, PA.



- Some devices are pushing conventional Si boundary
- Superjunction devices overcome 1D Si device limits

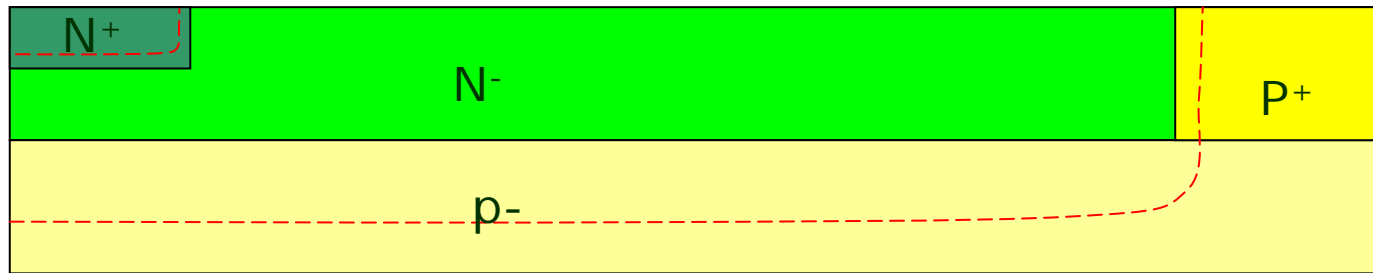
## 2.3 功率集成技术的发展

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- (1) 可集成器件的发展
- (2) **BCD**工艺集成技术
- (3) **Power SoC**

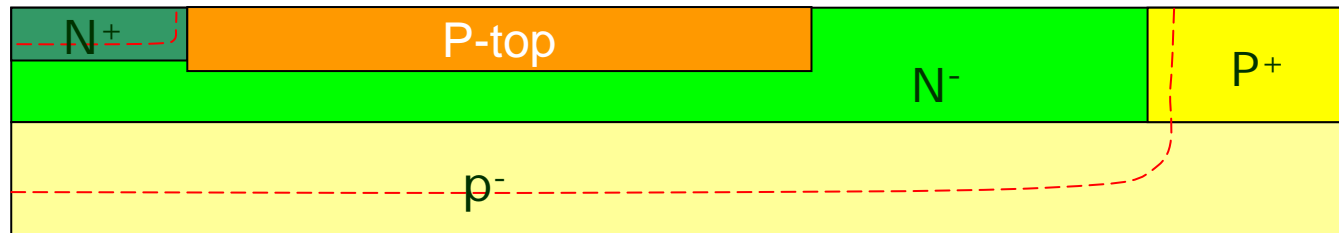
# 可集成器件的发展

$$E_s < E_C$$



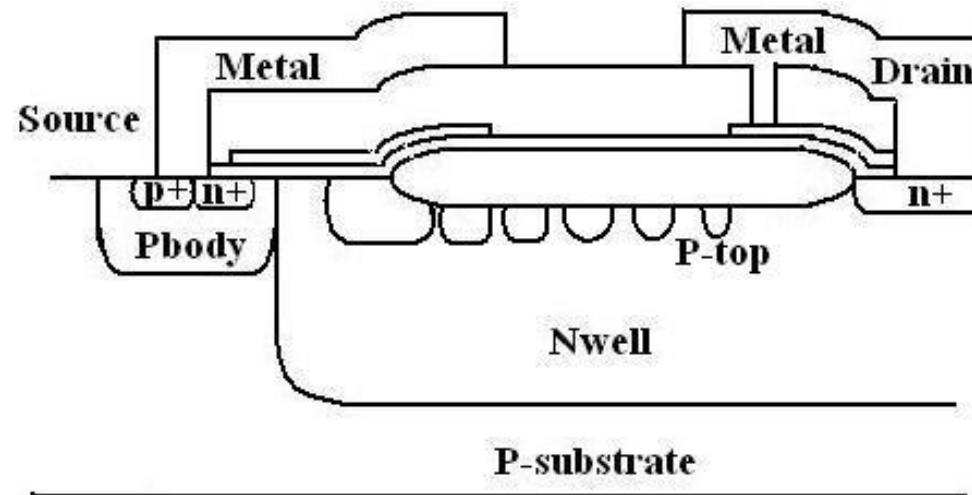
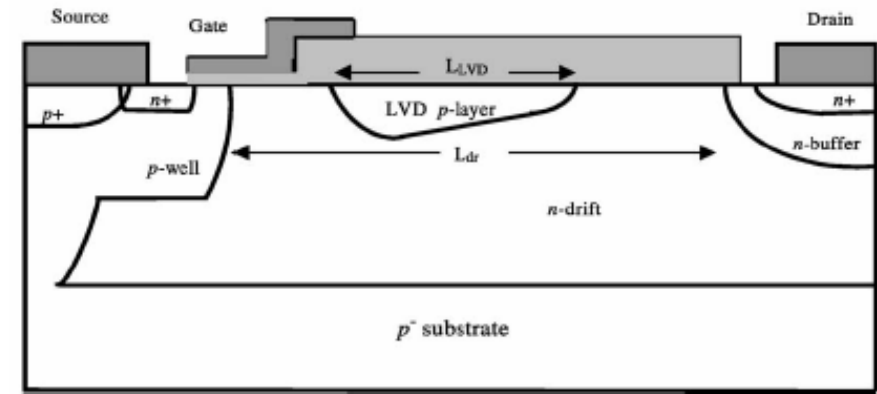
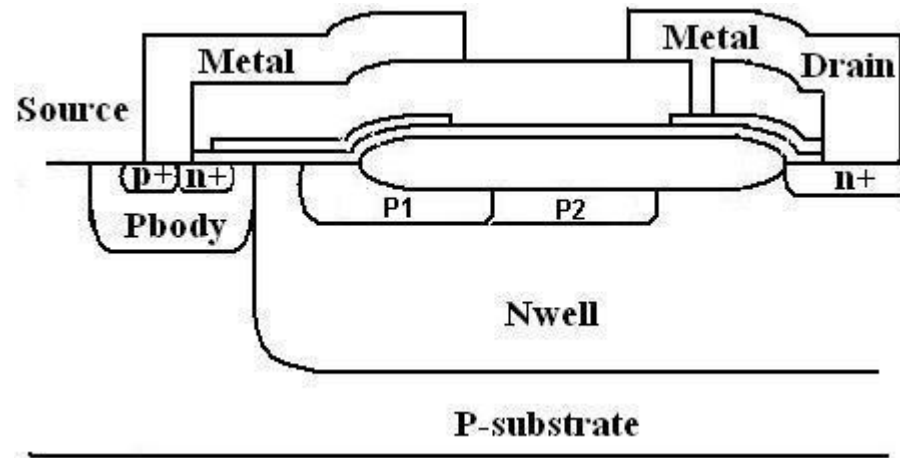
**Single-Resurf**

$$E_s < E_C$$

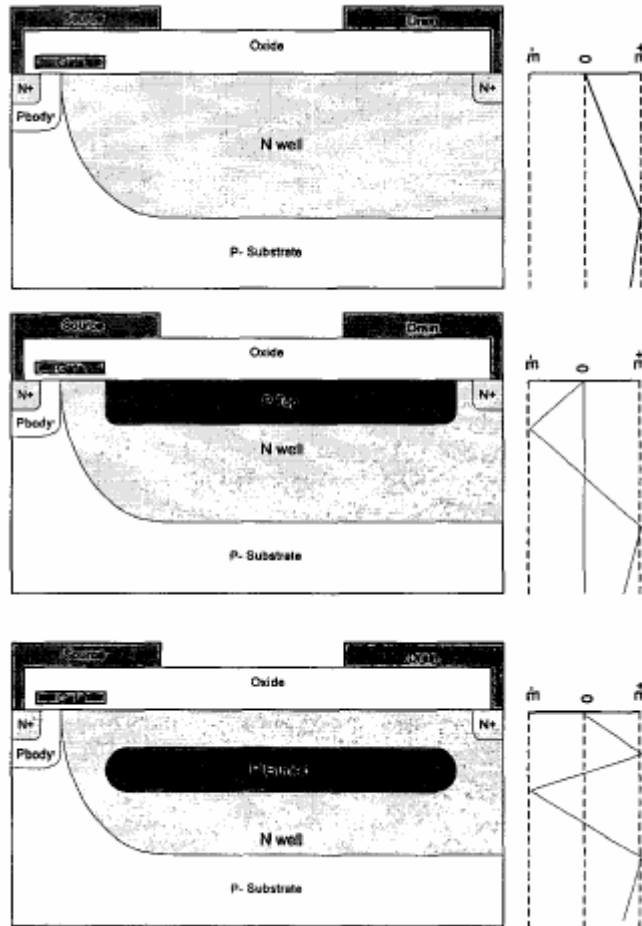


**Double-Resurf**

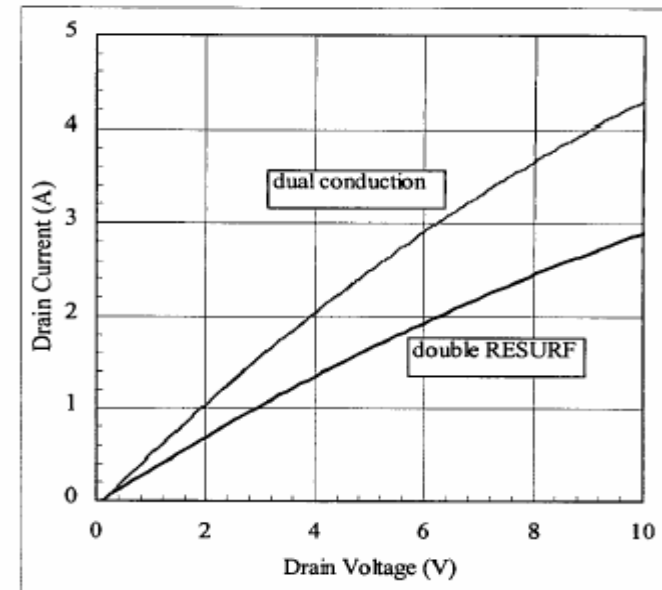
# Double RESURF with Non-Uniform P-top



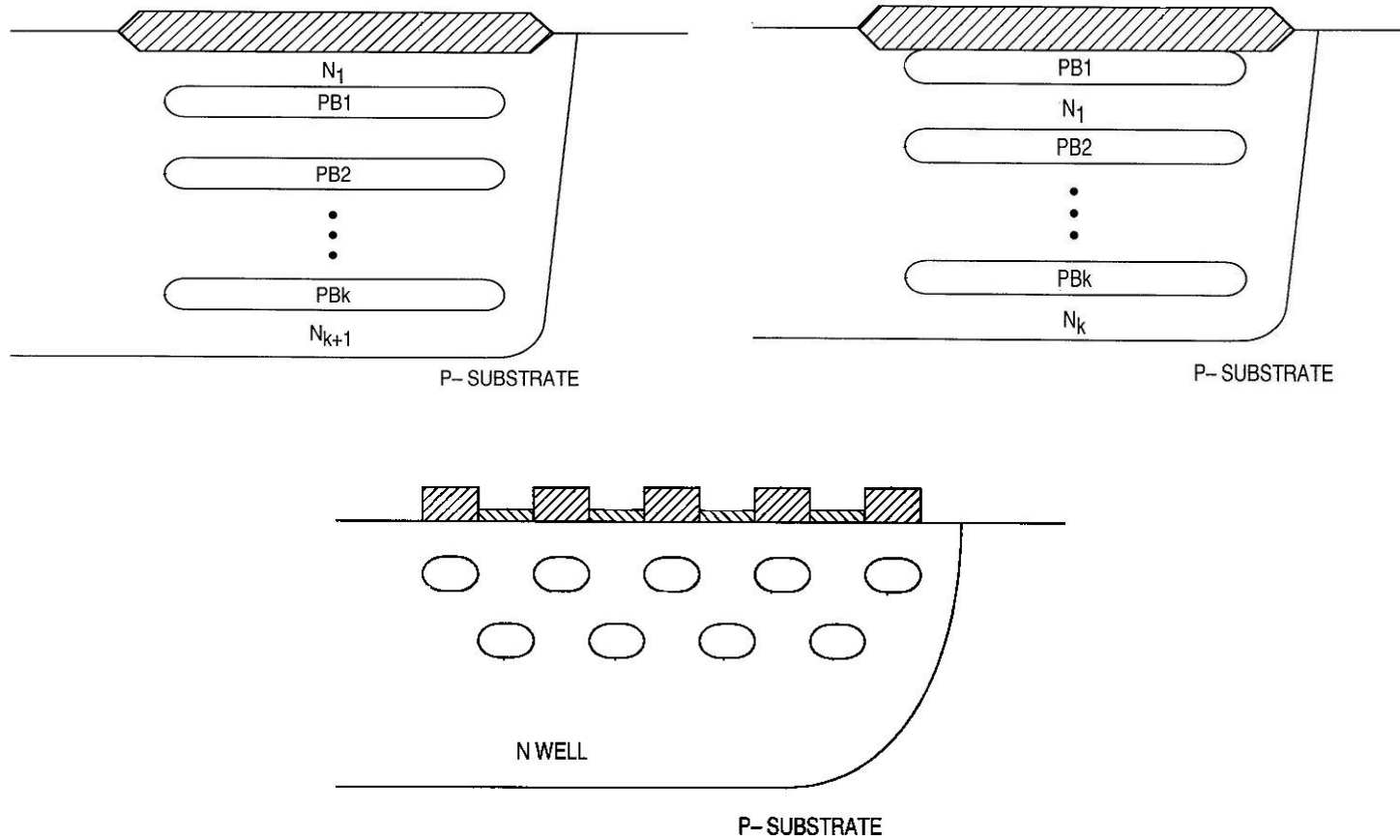
# LDMOS with dual conduction paths



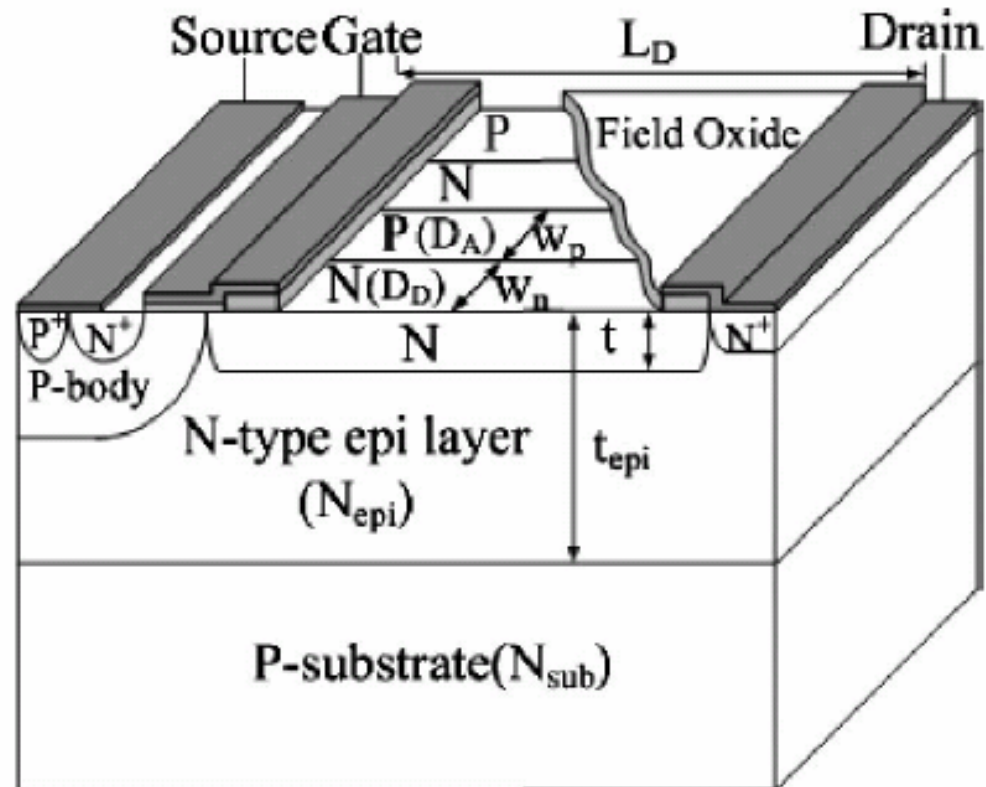
Z.Hossain, M.Imam, J.Fulton, and M.Tanaka, “**Double RESURF 700V N-channel LDMOS with best-in-class on-resistance**”, in Proc. Int. ISPSD Conf., p.137 2002



# High-voltage transistor with multi-layer conduction region



# 3D RESURF



Bo Zhang, et. al., High-Voltage LDMOS With Charge-Balanced Surface Low On-Resistance Path Layer, *IEEE ELECTRON DEVICE LETTERS*, VOL. 30, NO. 8, 2009

## Optimizing Technology of Bulk Electric Field for Lateral High-Voltage Devices

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**REBULF for bulk silicon lateral high-voltage devices**

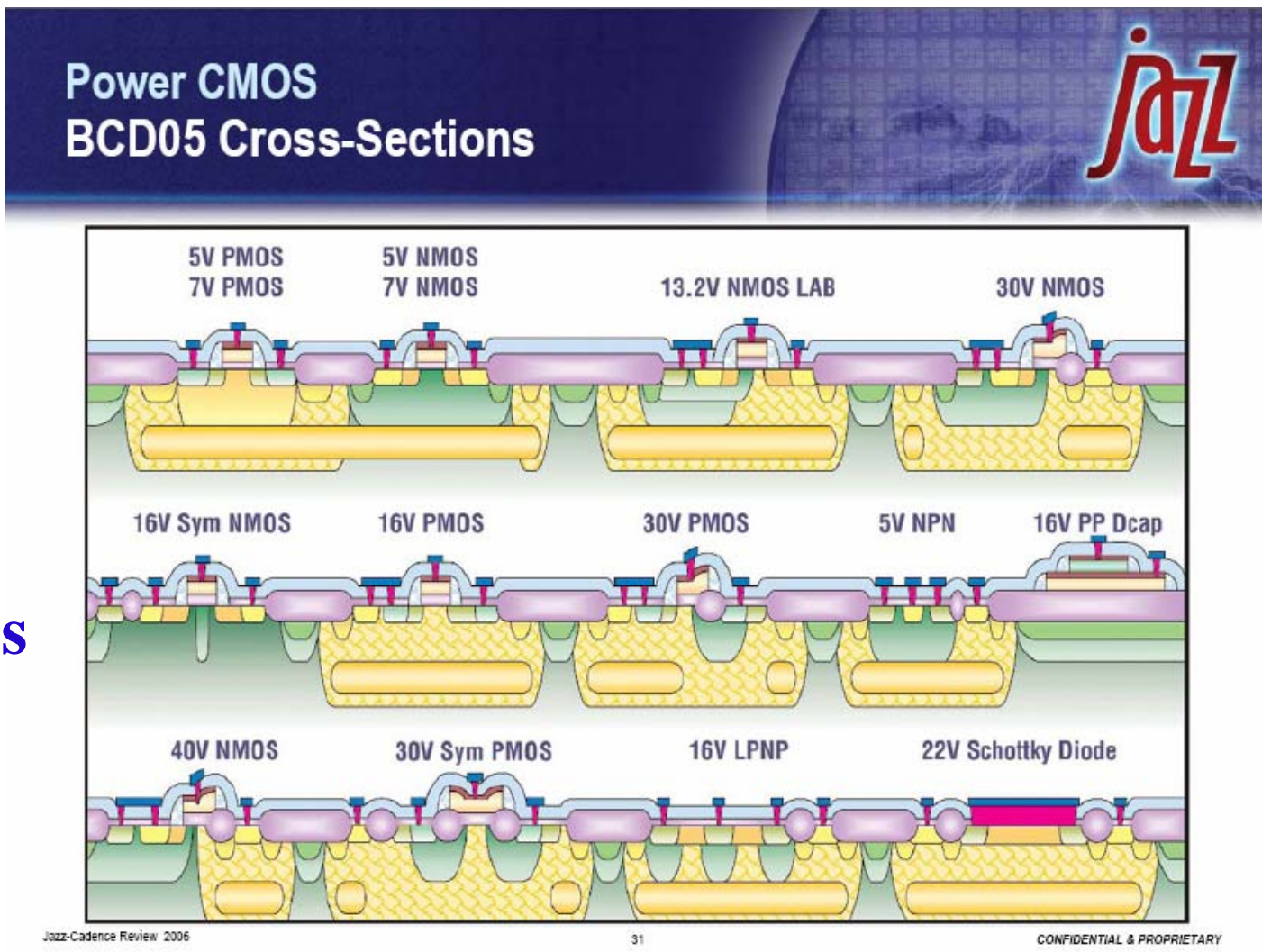
**ENDIF for SOI lateral high-voltage devices**

- **REBULF ----- Reduced Bulk Field**
- **ENDIF ----- ENhanced Dielectric layer Field**

Bo Zhang, et. al., “Field Enhancement for Dielectric Layer of High-Voltage Devices on Silicon on Insulator”, to be published in *IEEE on Trans. Electron Devices*.

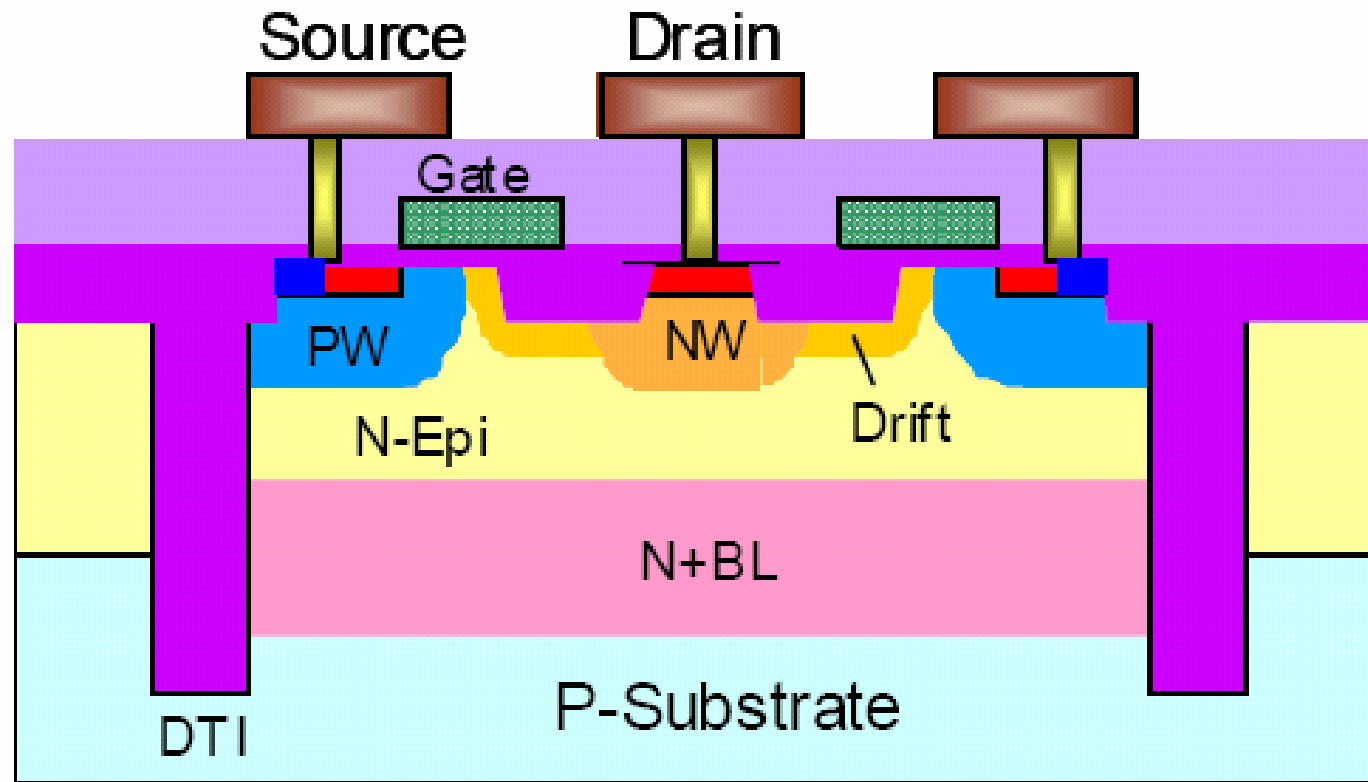


# BCD工艺集成技术

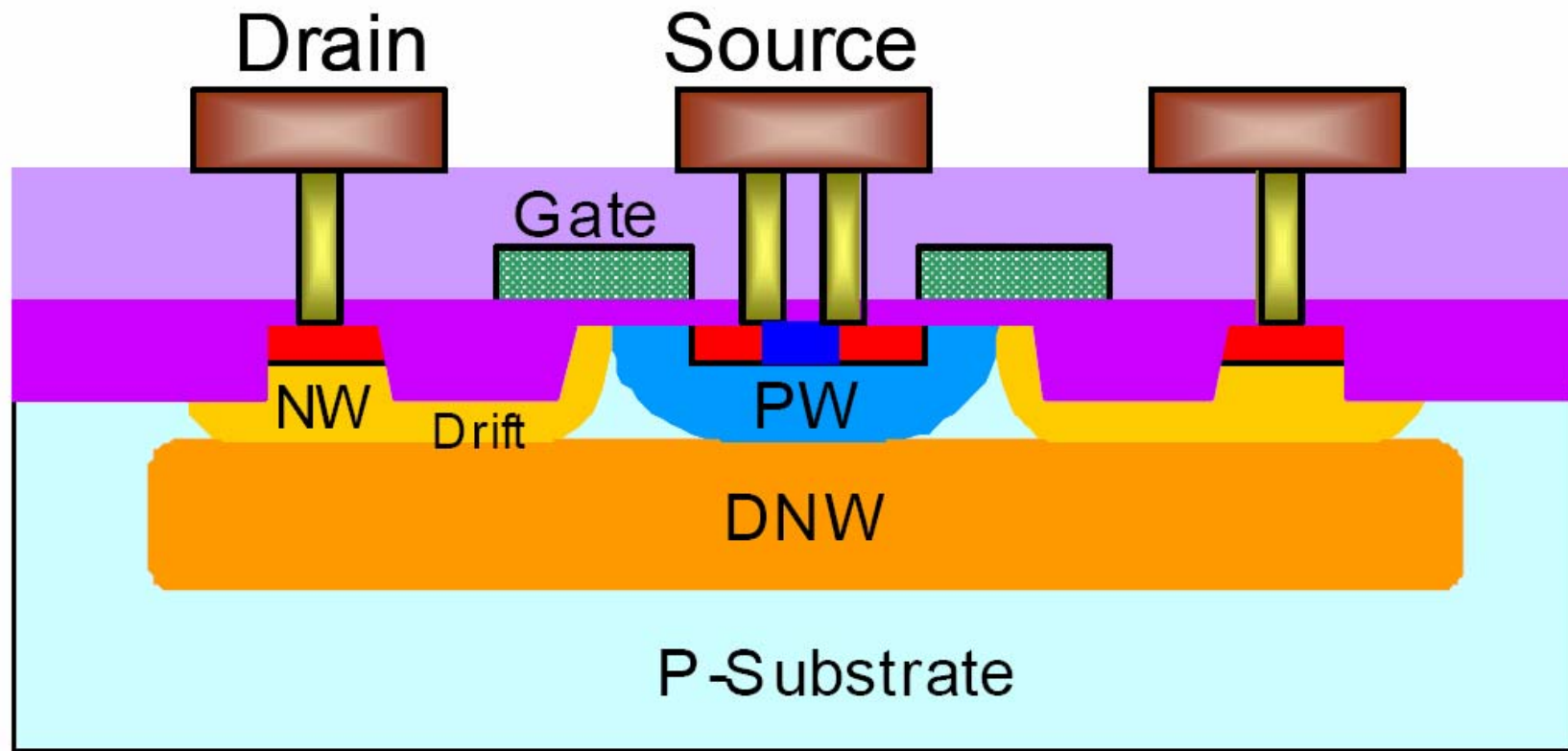


Si基  
BCD Process

# Toshiba's 5th generation 60V 0.13 $\mu\text{m}$ BCD Process

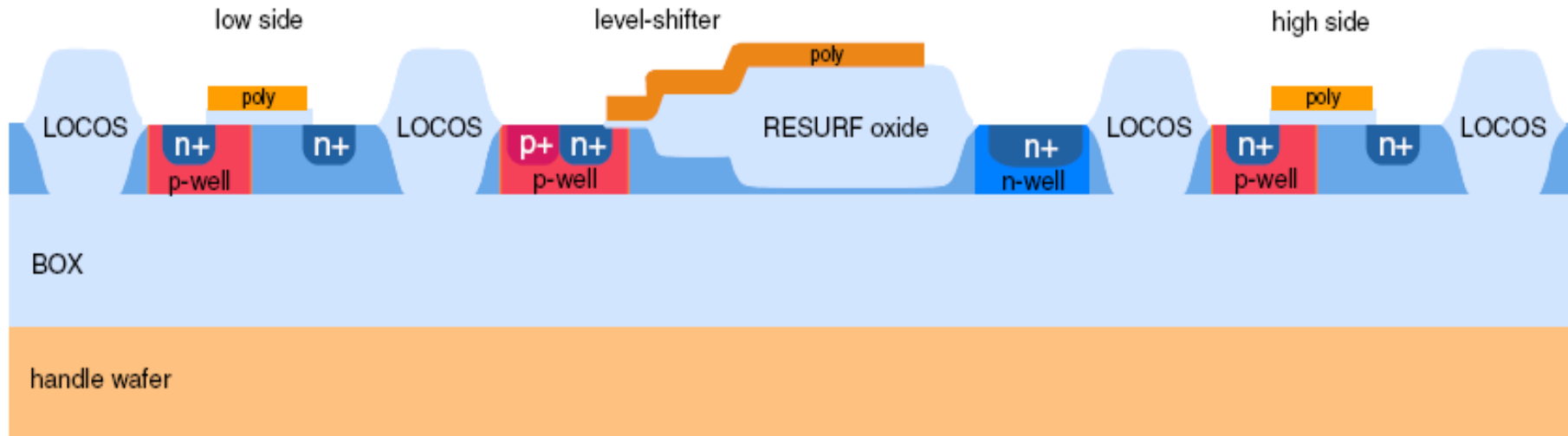


# Toshiba's 5th generation 18V 0.13 $\mu\text{m}$ CD Process



# BCD工艺集成技术

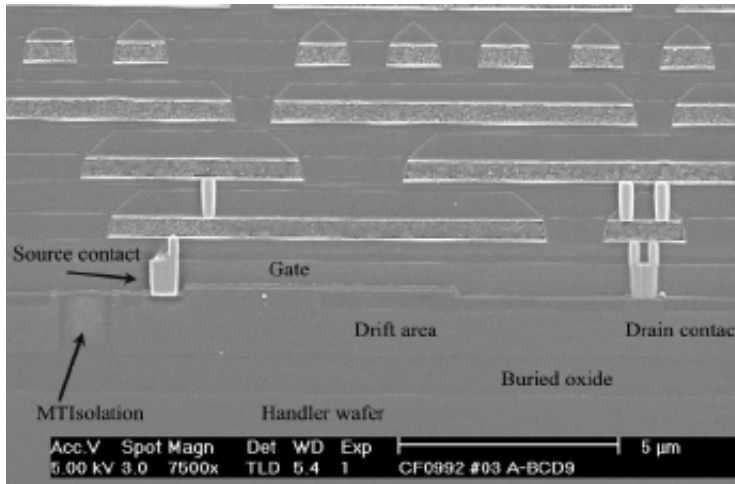
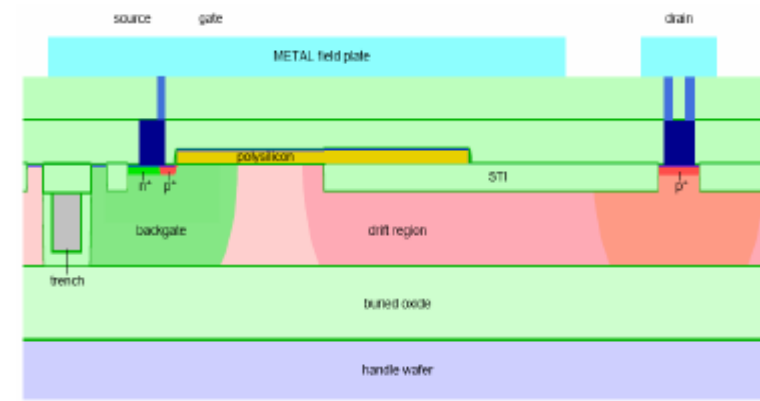
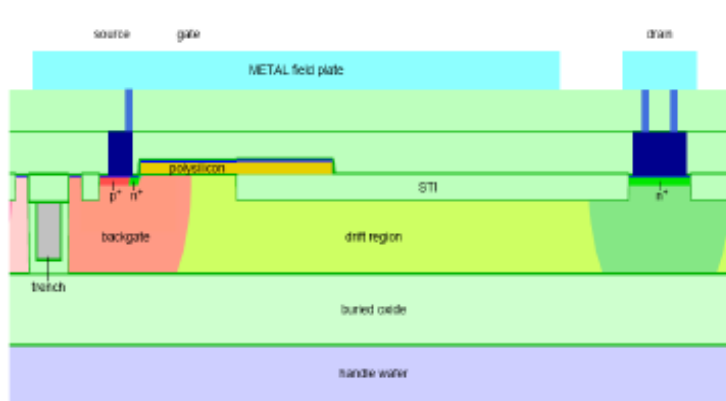
## SOI基BCD Process



Philips Corporation

# BCD工艺集成技术

## SOI基BCD Process



Wessels P, Swanenberg M, Claes J, et al. **Advanced 100V, 0.13 μ m BCD** process for next generation automotive applications. 2006 International Symposium on Power Semiconductor Devices and ICs, Vol.18: 197-120

Philips Corporation

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我国功率半导体发展现状

# 我国功率半导体发展现状

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- 普通二极管、三极管国内的自给率已经很高，但是在高档的功率二极管，大部分还依赖进口，国内的产品性能还有不小的差距。
- 在功率管领域，逐步有国内的企业技术水平上升到MOS工艺，并逐步上量，进口替代已然开始。
- 在电源管理领域，前十名都见不到国内的企业。

# 我国功率半导体发展现状

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- IGBT已从封装向芯片发展，从PT结构向NPT发展。
- BCD工艺已从无到有，从低压向高压发展，从硅基向SOI基发展。



谢谢!

