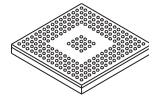


MCF548x ColdFire® Microprocessor

Supports MCF5480, MCF5481,
MCF5482, MCF5483, MCF5484, and
MCF5485

MCF548x



TEPBGA-388
27 mm x 27 mm

Features list:

- ColdFire V4e Core
 - Limited superscalar V4 ColdFire processor core
 - Up to 200MHz peak internal core frequency (308 MIPS [Dhrystone 2.1] @ 200 MHz)
 - Harvard architecture
 - 32-Kbyte instruction cache
 - 32-Kbyte data cache
 - Memory Management Unit (MMU)
 - Separate, 32-entry, fully-associative instruction and data translation lookahead buffers
 - Floating point unit (FPU)
 - Double-precision conforms to IEEE-754 standard
 - Eight floating point registers
- Internal master bus (XLB) arbiter
 - High performance split address and data transactions
 - Support for various parking modes
- 32-bit double data rate (DDR) synchronous DRAM (SDRAM) controller
 - 66–133 MHz operation
 - Supports DDR and SDR DRAM
 - Built-in initialization and refresh
 - Up to four chip selects enabling up to one GB of external memory
- Version 2.2 peripheral component interconnect (PCI) bus
 - 32-bit target and initiator operation
 - Support for up to five external PCI masters
 - 33–66 MHz operation with PCI bus to XLB divider ratios of 1:1, 1:2, and 1:4
- Flexible multi-function external bus (FlexBus)
 - Provides a glueless interface to boot flash/ROM, SRAM, and peripheral devices
 - Up to six chip selects
 - 33 – 66 MHz operation
- Communications I/O subsystem
 - Intelligent 16 channel DMA controller
 - Up to two 10/100 Mbps fast Ethernet controllers (FECs) each with separate 2-Kbyte receive and transmit FIFOs
 - Universal serial bus (USB) version 2.0 device controller
 - Support for one control and six programmable endpoints, interrupt, bulk, or isochronous
 - 4-Kbytes of shared endpoint FIFO RAM and 1 Kbyte of endpoint descriptor RAM
 - Integrated physical layer interface
 - Up to four programmable serial controllers (PSCs) each with separate 512-byte receive and transmit FIFOs for UART, USART, modem, codec, and IrDA 1.1 interfaces
 - I²C peripheral interface
 - Two FlexCAN controller area network 2.0B controllers each with 16 message buffers
 - DMA Serial Peripheral Interface (DSPI)
- Optional Cryptography accelerator module
 - Execution units for:
 - DES/3DES block cipher
 - AES block cipher
 - RC4 stream cipher
 - MD5/SHA-1/SHA-256/HMAC hashing
 - Random Number Generator
- 32-Kbyte system SRAM
 - Arbitration mechanism shares bandwidth between internal bus masters
- System integration unit (SIU)
 - Interrupt controller
 - Watchdog timer
 - Two 32-bit slice timers alarm and interrupt generation
 - Up to four 32-bit general-purpose timers, compare, and PWM capability
 - GPIO ports multiplexed with peripheral pins
- Debug and test features
 - ColdFire background debug mode (BDM) port
 - JTAG/ IEEE 1149.1 test access port
- PLL and clock generator
 - 30 to 66.67 MHz input frequency range
- Operating Voltages
 - 1.5V internal logic
 - 2.5V DDR SDRAM bus I/O
 - 3.3V PCI, FlexBus, and all other I/O
- Estimated power consumption
 - Less than 1.5W (388 PBGA)

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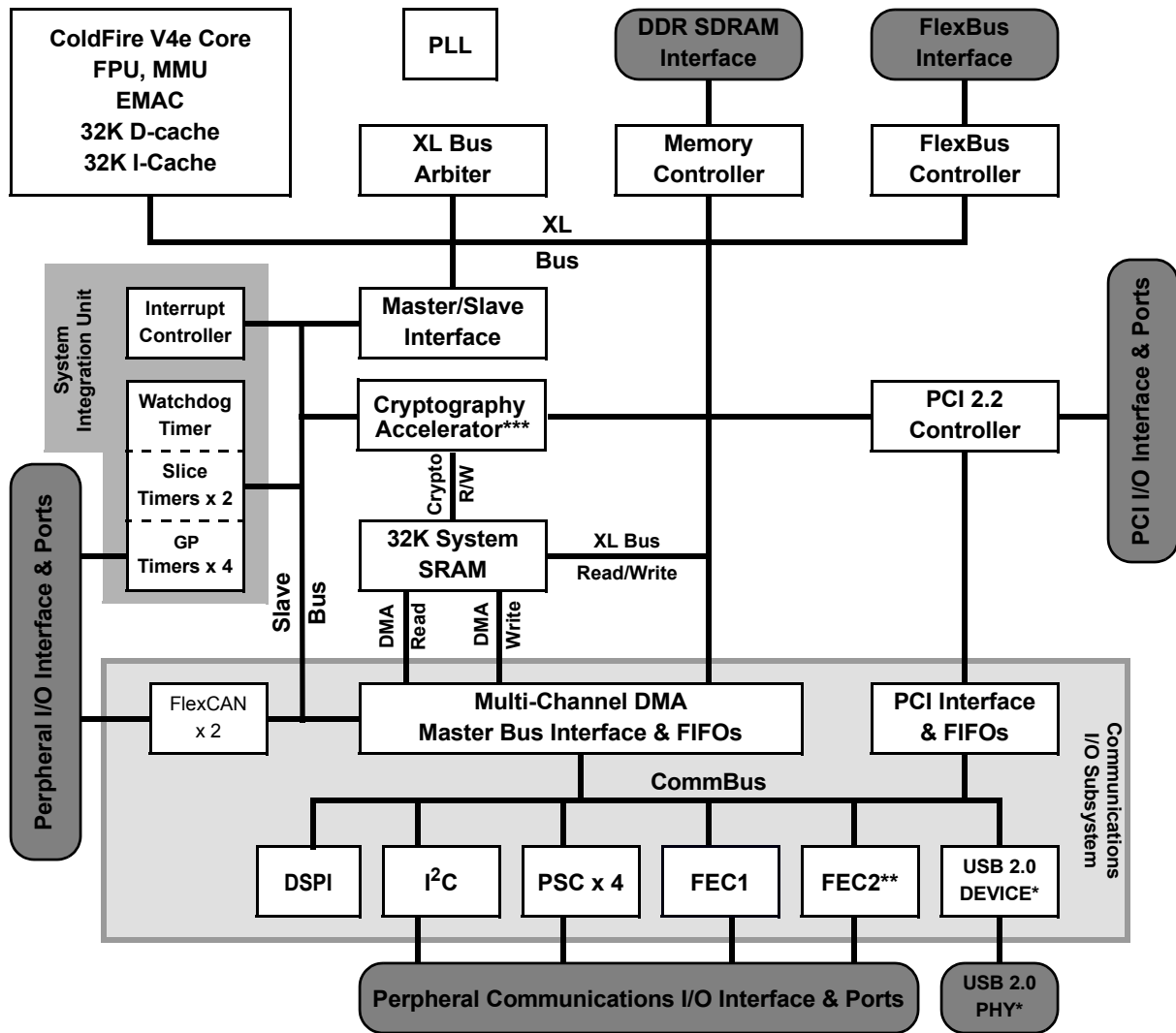


Figure 1. MCF548X Block Diagram

1 Maximum Ratings

Table 1 lists maximum and minimum ratings for supply and operating voltages and storage temperature. Operating outside of these ranges may cause erratic behavior or damage to the processor.

Table 1. Absolute Maximum Ratings

| Rating | Symbol | Value | Units |
|---|--------------|--|-------|
| External (I/O pads) supply voltage (3.3-V power pins) | EV_{DD} | -0.3 to +4.0 | V |
| Internal logic supply voltage | IV_{DD} | -0.5 to +2.0 | V |
| Memory (I/O pads) supply voltage (2.5-V power pins) | $SD V_{DD}$ | -0.3 to +4.0 SDR Memory -0.3 to +2.8 DDR Memory | V |
| PLL supply voltage | $PLL V_{DD}$ | -0.5 to +2.0 | V |
| Internal logic supply voltage, input voltage level | V_{in} | -0.5 to +3.6 | V |
| Storage temperature range | T_{stg} | -55 to +150 | °C |

2 Thermal Characteristics

2.1 Operating Temperatures

Table 2 lists junction and ambient operating temperatures.

Table 2. Operating Temperatures

| Characteristic | Symbol | Value | Units |
|--|------------|------------------|-------|
| Maximum operating junction temperature | T_j | 105 | °C |
| Maximum operating ambient temperature | T_{Amax} | <85 ¹ | °C |
| Minimum operating ambient temperature | T_{Amin} | -40 | °C |

¹ This published maximum operating ambient temperature should be used only as a system design guideline. All device operating parameters are guaranteed only when the junction temperature lies within the specified range.

2.2 Thermal Resistance

Table 3 lists thermal resistance values.

Table 3. Thermal Resistance

| Characteristic | | Symbol | Value | Unit |
|--|-------------------------|----------------|----------------------|------|
| 324 pin TEPBGA — Junction to ambient, natural convection | Four layer board (2s2p) | θ_{JMA} | 20–22 ^{1,2} | °CW |
| 388 pin TEPBGA — Junction to ambient, natural convection | Four layer board (2s2p) | θ_{JMA} | 19 ^{1,2} | °CW |
| Junction to ambient (@200 ft/min) | Four layer board (2s2p) | θ_{JMA} | 16 ^{1,2} | °CW |
| Junction to board | — | θ_{JB} | 11 ³ | °CW |
| Junction to case | — | θ_{JC} | 7 ⁴ | °CW |
| Junction to top of package | Natural convection | Ψ_{jt} | 2 ^{1,5} | °CW |

¹ θ_{JA} and Ψ_{jt} parameters are simulated in accordance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of θ_{JA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

² Per JEDEC JESD51-6 with the board horizontal.

³ Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

⁴ Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

⁵ Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

3 DC Electrical Specifications

Table 4 lists DC electrical operating temperatures. This table is based on an operating voltage of $EV_{DD} = 3.3 V_{DC} \pm 0.3 V_{DC}$ and IV_{DD} of $1.5 \pm 0.07 V_{DC}$.

Table 4. DC Electrical Specifications

| Characteristic | Symbol | Min | Max | Units |
|--|-------------------|------|------|-------|
| External (I/O pads) operation voltage range | EV_{DD} | 3.0 | 3.6 | V |
| Memory (I/O pads) operation voltage range (DDR Memory) | $SD V_{DD}$ | 2.30 | 2.70 | V |
| Internal logic operation voltage range ¹ | IV_{DD} | 1.43 | 1.58 | V |
| PLL Analog operation voltage range ¹ | $PLL V_{DD}$ | 1.43 | 1.58 | V |
| USB oscillator operation voltage range | USB_OSV_{DD} | 3.0 | 3.6 | V |
| USB digital logic operation voltage range | $USBV_{DD}$ | 3.0 | 3.6 | V |
| USB PHY operation voltage range | USB_PHYV_{DD} | 3.0 | 3.6 | V |
| USB oscillator analog operation voltage range | USB_OSCAV_{DD} | 1.43 | 1.58 | V |

Table 4. DC Electrical Specifications (continued)

| Characteristic | Symbol | Min | Max | Units |
|--|------------------------|------------------------|--------------------------|-------|
| USB PLL operation voltage range | USB_PLLV _{DD} | 1.43 | 1.58 | V |
| Input high voltage SSTL 3.3V/2.5V ² | V _{IH} | V _{REF} + 0.3 | SD V _{DD} + 0.3 | V |
| Input low voltage SSTL 3.3V/2.5V ² | V _{IL} | V _{SS} - 0.3 | V _{REF} - 0.3 | V |
| Input high voltage 3.3V I/O pins | V _{IH} | 0.7 x EV _{DD} | EV _{DD} + 0.3 | V |
| Input low voltage 3.3V I/O pins | V _{IL} | V _{SS} - 0.3 | 0.35 x EV _{DD} | V |
| Output high voltage I _{OH} = 8 mA, 16 mA, 24 mA | V _{OH} | 2.4 | — | V |
| Output low voltage I _{OL} = 8 mA, 16 mA, 24 mA ⁵ | V _{OL} | — | 0.5 | V |
| Capacitance ³ , V _{in} = 0 V, f = 1 MHz | C _{IN} | — | TBD | pF |
| Input leakage current | I _{in} | -1.0 | 1.0 | μA |

¹ IV_{DD} and PLL V_{DD} should be at the same voltage. PLL V_{DD} should have a filtered input. Please see [Figure 2](#) for an example circuit. There are three PLL V_{DD} inputs. A filter circuit should be used on each PLL V_{DD} input.

² This specification is guaranteed by design and is not 100% tested.

³ Capacitance C_{IN} is periodically sampled rather than 100% tested.

4 Hardware Design Considerations

4.1 PLL Power Filtering

To further enhance noise isolation, an external filter is strongly recommended for PLL analog V_{DD} pins. The filter shown in [Figure 2](#) should be connected between the board V_{DD} and the PLL V_{DD} pins. The resistor and capacitors should be placed as close to the dedicated PLL V_{DD} pin as possible.

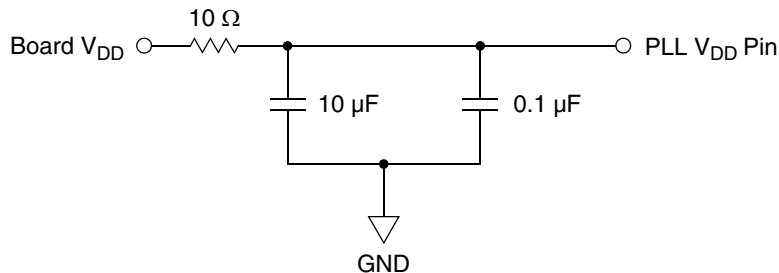
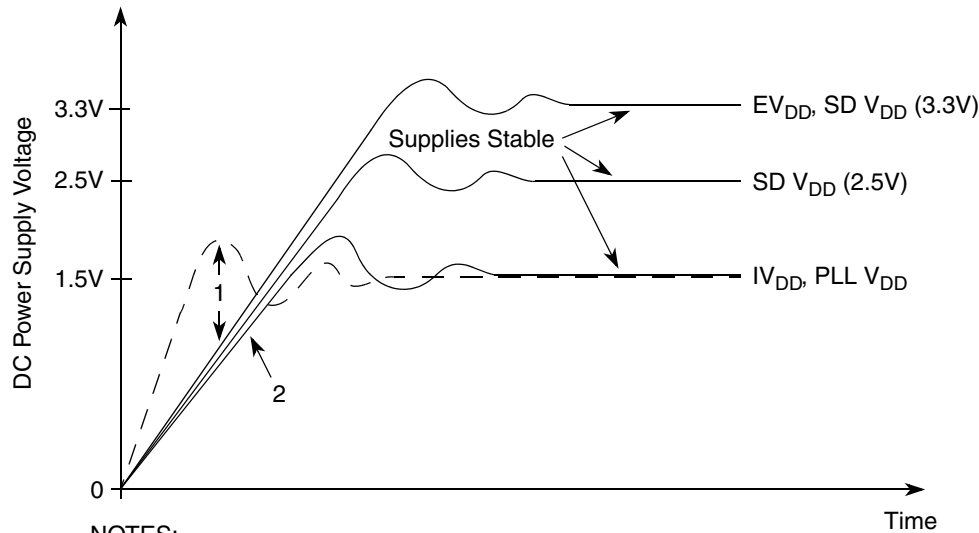


Figure 2. System PLL V_{DD} Power Filter

4.2 Supply Voltage Sequencing and Separation Cautions

[Figure 3](#) shows situations in sequencing the I/O V_{DD} (EV_{DD}), SDRAM V_{DD} (SD V_{DD}), PLL V_{DD} (PLL V_{DD}), and Core V_{DD} (IV_{DD}).



NOTES:

1. IV_{DD} should not exceed EV_{DD} or $SD V_{DD}$ by more than 0.4V at any time, including power-up.
2. Recommended that $IV_{DD}/PLL V_{DD}$ should track $EV_{DD}/SD V_{DD}$ up to 0.9V, then separate for completion of ramps.
3. Input voltage must not be greater than the supply voltage (EV_{DD} , $SD V_{DD}$, IV_{DD} , or $PLL V_{DD}$) by more than 0.5V at any time, including during power-up.
4. Use 1 microsecond or slower rise time for all supplies.

Figure 3. Supply Voltage Sequencing and Separation Cautions

The relationship between $SD V_{DD}$ and EV_{DD} is non-critical during power-up and power-down sequences. $SD V_{DD}$ (2.5V or 3.3V) and EV_{DD} are specified relative to IV_{DD} .

4.2.1 Power Up Sequence

If $EV_{DD}/SD V_{DD}$ are powered up with the IV_{DD} at 0V, the sense circuits in the I/O pads cause all pad output drivers connected to the $EV_{DD}/SD V_{DD}$ to be in a high impedance state. There is no limit to how long after $EV_{DD}/SD V_{DD}$ powers up before IV_{DD} must power up. IV_{DD} should not lead the EV_{DD} , $SD V_{DD}$, or $PLL V_{DD}$ by more than 0.4V during power ramp up or there is high current in the internal ESD protection diodes. The rise times on the power supplies should be slower than 1 microsecond to avoid turning on the internal ESD protection clamp diodes.

The recommended power up sequence is as follows:

1. Use 1 microsecond or slower rise time for all supplies.
2. $IV_{DD}/PLL V_{DD}$ and $EV_{DD}/SD V_{DD}$ should track up to 0.9V, then separate for the completion of ramps with $EV_{DD}/SD V_{DD}$ going to the higher external voltages. One way to accomplish this is to use a low drop-out voltage regulator.

4.2.2 Power Down Sequence

If $IV_{DD}/PLL V_{DD}$ are powered down first, sense circuits in the I/O pads cause all output drivers to be in a high impedance state. There is no limit on how long after IV_{DD} and $PLL V_{DD}$ power down before EV_{DD} or $SD V_{DD}$ must power down. IV_{DD} should not lag EV_{DD} , $SD V_{DD}$, or $PLL V_{DD}$ going low by more than 0.4V during power down or there is undesired high current in the ESD protection diodes. There are no requirements for the fall times of the power supplies.

The recommended power down sequence is as follows:

1. Drop $IV_{DD}/PLL V_{DD}$ to 0V
2. Drop $EV_{DD}/SD V_{DD}$ supplies

4.3 General USB Layout Guidelines

4.3.1 USB D+ and D- High-Speed Traces

1. High speed clock and the USB D+ and USB D- differential pair should be routed first.
2. Route USB D+ and USB D- signals on the top layer of the board.
3. The trace width and spacing of the USB D+ and USB D- signals should be such that the differential impedance is 90Ω .
4. Route traces over continuous planes (power and ground)—they should not pass over any power/ground plane slots or anti-etch. When placing connectors, make sure the ground plane clear-outs around each pin have ground continuity between all pins.
5. Maintain the parallelism (skew matched) between USB D+ and USB D-. These traces should be the same overall length.
6. Do not route USB D+ and USB D- traces under oscillators or parallel to clock traces and/or data buses. Minimize the lengths of high speed signals that run parallel to the USB D+ and USB D- pair. Maintain a minimum 50mil spacing to clock signals.
7. Keep USB D+ and USB D- traces as short as possible.
8. Route USB D+, USB D-, and USB VBUS signals with a minimum amount of vias and corners. Use 45° turns.
9. Stubs should be avoided as much as possible. If they cannot be avoided, stubs should be no greater than 200mils.

4.3.2 USB VBUS Traces

Connecting the USB VBUS pin directly to the 5V VBUS signal from the USB connector can cause long-term reliability problems in the ESD network of the processor. Therefore, use of an external voltage divider for VBUS is recommended. [Figure 4](#) and [Figure 5](#) depict possible connections for VBUS. Point A, marked in each figure, is where a 5V version of VBUS should connect. Point B, marked in each figure, is where a 3.3V version of VBUS should connect to the USB VBUS pin on the device.

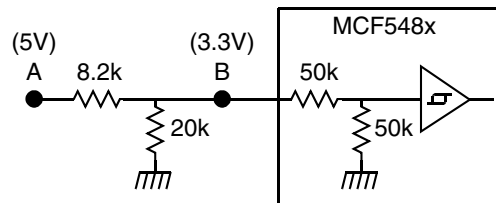


Figure 4. Preferred VBUS Connections

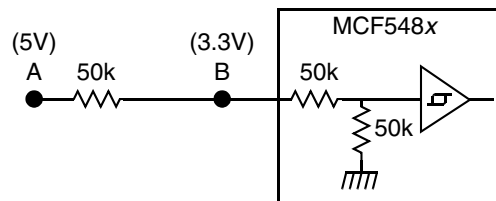


Figure 5. Alternate VBUS Connections

4.3.3 USB Receptacle Connections

It is recommended to connect the shield and the ground pin of the B USB receptacle for upstream ports to the board ground plane. The ground pin of the A USB receptacles for downstream ports should also be connected to the board ground plane, but industry practice varies widely on the connection of the shield of the A USB receptacles to other system grounds. Take precautions for control of ground loops between hosts and self-powered USB devices through the cable shield.

4.4 USB Power Filtering

To minimize noise, an external filter is required for each of the USB power pins. The filter shown in [Figure 6](#) should be connected between the board EV_{DD} or IV_{DD} and each of the USB V_{DD} pins.

- The resistor and capacitors should be placed as close to the dedicated USB V_{DD} pin as possible.
- A separate filter circuit should be included for each USB V_{DD} pin, a total of five circuits.
- All traces should be as low impedance as possible, especially ground pins to the ground plane.
- The filter for USB_PHYVDD to VSS should be connected to the power and ground planes, respectively, not fingers of the planes.
- In addition to keeping the filter components for the USB_PLLVDD as close as practical to the body of the processor as previously mentioned, special care should be taken to avoid coupling switching power supply noise or digital switching noise onto the portion of that supply between the filter and the processor.
- The capacitors for C2 in the table below should be rated X5R or better due to temperature performance.

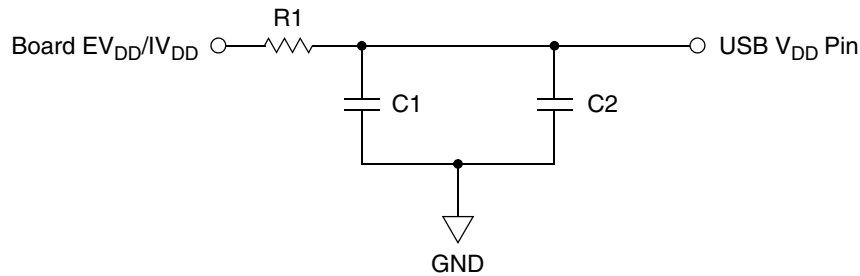


Figure 6. USB V_{DD} Power Filter

NOTE

In addition to the above filter circuitry, a 0.01 F capacitor is also recommended in parallel with those shown.

[Table 5](#) lists the resistor values and supply voltages to be used in the circuit for each of the USB V_{DD} pins.

Table 5. USB Filter Circuit Values

| USB V_{DD} Pin | Nominal Voltage | R1 (Ω) | C1 (μ F) | C2 (μ F) |
|---|-----------------|-----------------|---------------|---------------|
| USBVDD (Bias generator supply) | 3.3V | 10 | 10 | 0.1 |
| USB_PHYVDD (Main transceiver supply) | 3.3V | 0 | 10 | 0.1 |
| USB_PLLVDD (PLL supply) | 1.5V | 10 | 1 | 0.1 |
| USB_OSCVDD (Oscillator supply) | 3.3V | 0 | 10 | 0.1 |
| USB_OSCAVDD (Oscillator analog supply) | 1.5V | 0 | 10 | 0.1 |

4.4.1 Bias Resistor

The USBRBIAS resistor should be placed as close to the dedicated USB 2.0 pins as possible. The tolerance should be $\pm 1\%$.

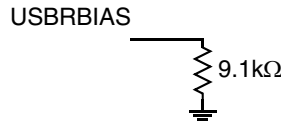


Figure 7. USBRBIAS Connection

5 Output Driver Capability and Loading

Table 6 lists values for drive capability and output loading.

Table 6. I/O Driver Capability¹

| Signal | Drive Capability | Output Load (C _L) |
|---|------------------|-------------------------------|
| SDRAMC (SDADDR[12:0], SDDATA[31:0], \overline{RAS} , \overline{CAS} , SDDM[3:0], \overline{SDWE} , SDBA[1:0]) | 24 mA | 15 pF |
| SDRAMC DQS and clocks (SDDQS[3:0], SDRDQS, SDCLK[1:0], \overline{SDCLK} [1:0], SDCKE) | 24 mA | 15 pF |
| SDRAMC chip selects (\overline{SDCS} [3:0]) | 24 mA | 15 pF |
| FlexBus (AD[31:0], \overline{FBCS} [5:0], ALE, R/\overline{W} , $\overline{BE}/\overline{BWE}$ [3:0], \overline{OE}) | 16 mA | 30 pF |
| FEC (EnMDIO, EnMDC, EnTXEN, EnTXD[3:0], EnTXER) | 8 mA | 15 pF |
| Timer (TOUT[3:0]) | 8 mA | 50 pF |
| FlexCAN (CANTX) | 8 mA | 30 pF |
| \overline{DACK} [1:0] | 8 mA | 30 pF |
| PSC (PSCnTXD[3:0], $\overline{PSCnRTS}/\overline{PSCnFSYNC}$, | 8 mA | 30 pF |
| DSPI (DSPISOUT, DSPICS0/SS, DSPICS[2:3], DSPICS5/PCSS) | 24 mA | 50 pF |
| PCI (PCIAD[31:0], PCIBG[4:1], PCIBG0/PCIREQOUT, PCIDEVSEL, PCICXBE[3:0], PCIFRM, PCIPERR, PCIRESET, PCISERR, PCISTOP, PCIPAR, PCITRDY, PCIIRDY) | 16 mA | 50 pF |
| I2C (SCL, SDA) | 8 mA | 50 pF |
| BDM (PSTCLK, PSTDDATA[7:0], DSO/TDO, | 8 mA | 25 pF |
| RSTO | 8 mA | 50 pF |

¹ The device's pads have balanced sink and source current. The drive capability is the same as the sink capability.

6 PLL Timing Specifications

The specifications in [Table 7](#) are for the CLKIN pin.

Table 7. Clock Timing Specifications

| Num | Characteristic | Min | Max | Units |
|-----|---|-----|-----|-------|
| C1 | Cycle time | 20 | 40 | ns |
| C2 | Rise time (20% of V _{dd} to 80% of v _{dd}) | — | 2 | ns |
| C3 | Fall time (80% of V _{dd} to 20% of V _{dd}) | — | 2 | ns |
| C4 | Duty cycle (at 50% of V _{dd}) | 40 | 60 | % |

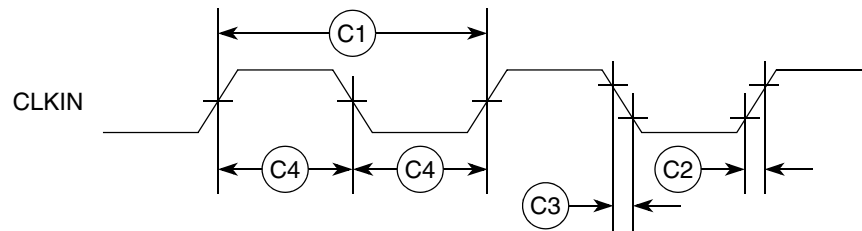


Figure 8. Input Clock Timing Diagram

[Table 8](#) shows the supported PLL encodings.

Table 8. MCF548x Divide Ratio Encodings

| AD[12:8] ¹ | Clock Ratio | CLKIN—PCI and FlexBus Frequency Range (MHz) | Internal XLB, SDRAM Bus, and PSTCLK Frequency Range (MHz) | Core Frequency Range (MHz) |
|-----------------------|-------------|---|---|----------------------------|
| 00011 | 1:2 | 41.67–50.0 | 83.33–100 | 166.66–200 |
| 00101 | 1:2 | 25.0–41.67 | 50.0–83.33 ² | 100.0–166.66 |
| 01111 | 1:4 | 25.0 | 100 | 200 |

¹ All other values of AD[12:8] are reserved.

² DDR memories typically have a minimum speed of 83 MHz. Some vendors specify down to 75 MHz. Check with the memory component specifications to verify.

[Figure 9](#) correlates CLKIN, internal bus, and core clock frequencies for the 1x–4x multipliers.

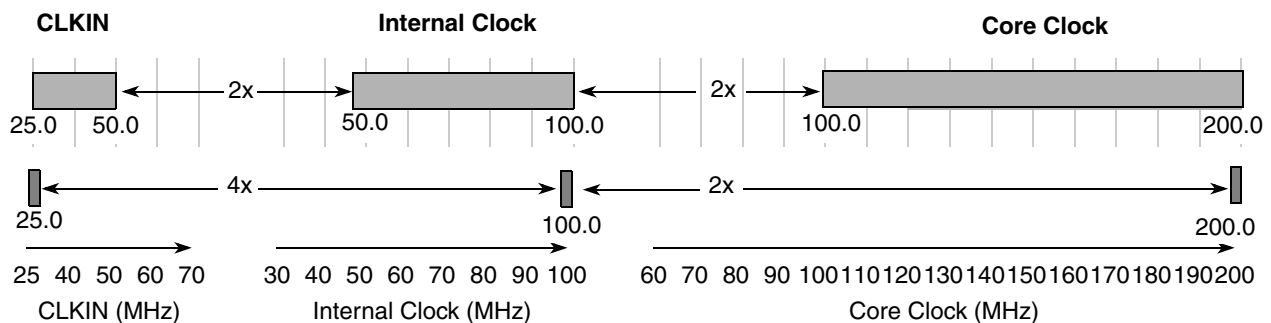


Figure 9. CLKIN, Internal Bus, and Core Clock Ratios

7 Reset Timing Specifications

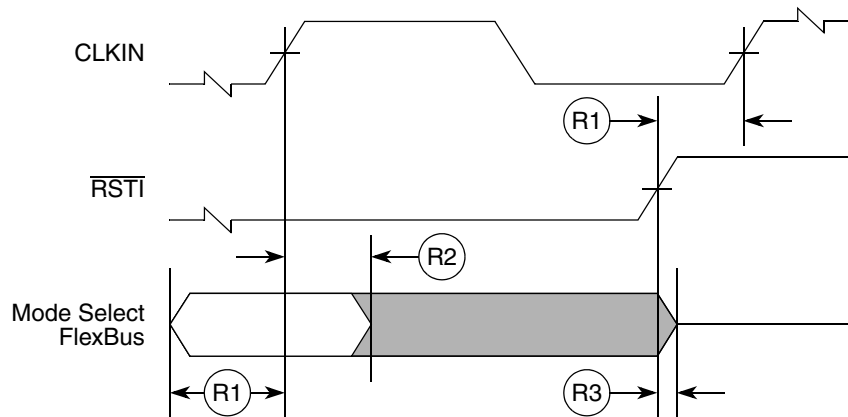
Table 9 lists specifications for the reset timing parameters shown in Figure 10

Table 9. Reset Timing Specifications

| Num | Characteristic | 50 MHz CLKIN | | Units |
|-----------------|--|--------------|-----|--------------|
| | | Min | Max | |
| R1 ¹ | Valid to CLKIN (setup) | 8 | — | ns |
| R2 | CLKIN to invalid (hold) | 1.0 | — | ns |
| R3 | $\overline{\text{RSTI}}$ to invalid (hold) | 1.0 | — | ns |
| | $\overline{\text{RSTI}}$ pulse duration | 5 | — | CLKIN cycles |

¹ $\overline{\text{RSTI}}$ and FlexBus data lines are synchronized internally. Setup and hold times must be met only if recognition on a particular clock is required.

Figure 10 shows reset timing for the values in Table 9.



NOTE:

Mode selects are registered on the rising clock edge before the cycle in which $\overline{\text{RSTI}}$ is recognized as being negated.

Figure 10. Reset Timing

8 FlexBus

A multi-function external bus interface called FlexBus is provided on the MCF5482 with basic functionality to interface to slave-only devices up to a maximum bus frequency of 66 MHz. It can be directly connected to asynchronous or synchronous devices such as external boot ROMs, flash memories, gate-array logic, or other simple target (slave) devices with little or no additional circuitry. For asynchronous devices, a simple chip-select based interface can be used. The FlexBus interface has six general purpose chip-selects ($\overline{\text{FBCS}}[5:0]$). Chip-select $\overline{\text{FBCS0}}$ can be dedicated to boot ROM access and can be programmed to be byte (8 bits), word (16 bits), or longword (32 bits) wide. Control signal timing is compatible with common ROM / flash memories.

8.1 FlexBus AC Timing Characteristics

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the system clock.

Table 10. FlexBus AC Timing Specifications

| Num | Characteristic | Min | Max | Unit | Notes |
|-----|---|-----|-----|------|-----------------|
| | Frequency of Operation | 25 | 50 | Mhz | ¹ |
| FB1 | Clock Period (CLKIN) | 20 | 40 | ns | ² |
| FB2 | Address, Data, and Control Output Valid (AD[31:0], $\overline{\text{FBCS}}[5:0]$, R/W, ALE, TSIZ[1:0], $\overline{\text{BE}}/\overline{\text{BWE}}[3:0]$, $\overline{\text{OE}}$, and $\overline{\text{TBST}}$) | — | 7.0 | ns | ³ |
| FB3 | Address, Data, and Control Output Hold ((AD[31:0], $\overline{\text{FBCS}}[5:0]$, R/W, ALE, TSIZ[1:0], $\overline{\text{BE}}/\overline{\text{BWE}}[3:0]$, $\overline{\text{OE}}$, and $\overline{\text{TBST}}$) | 1 | — | ns | ^{3, 4} |
| FB4 | Data Input Setup | 3.5 | — | ns | |
| FB5 | Data Input Hold | 0 | — | ns | |
| FB6 | Transfer Acknowledge ($\overline{\text{TA}}$) Input Setup | 4 | — | ns | |
| FB7 | Transfer Acknowledge ($\overline{\text{TA}}$) Input Hold | 0 | — | ns | |
| FB8 | Address Output Valid (PCIAD[31:0]) | — | 7.0 | ns | ⁵ |
| FB9 | Address Output Hold (PCIAD[31:0]) | 0 | — | ns | ⁵ |

¹ The frequency of operation is the same as the PCI frequency of operation. The MCF548X supports a single external reference clock (CLKIN). This signal defines the frequency of operation for FlexBus and PCI.

² Max cycle rate is determined by CLKIN and how the user has the system PLL configured.

³ Timing for chip selects only applies to the $\overline{\text{FBCS}}[5:0]$ signals. Please see [Section 9.2, “DDR SDRAM AC Timing Characteristics”](#) for $\overline{\text{SDCS}}[3:0]$ timing.

⁴ The FlexBus supports programming an extension of the address hold. Please consult the MCF548X specification manual for more information.

⁵ These specs are used when the PCIAD[31:0] signals are configured as 32-bit, non-muxed FlexBus address signals.

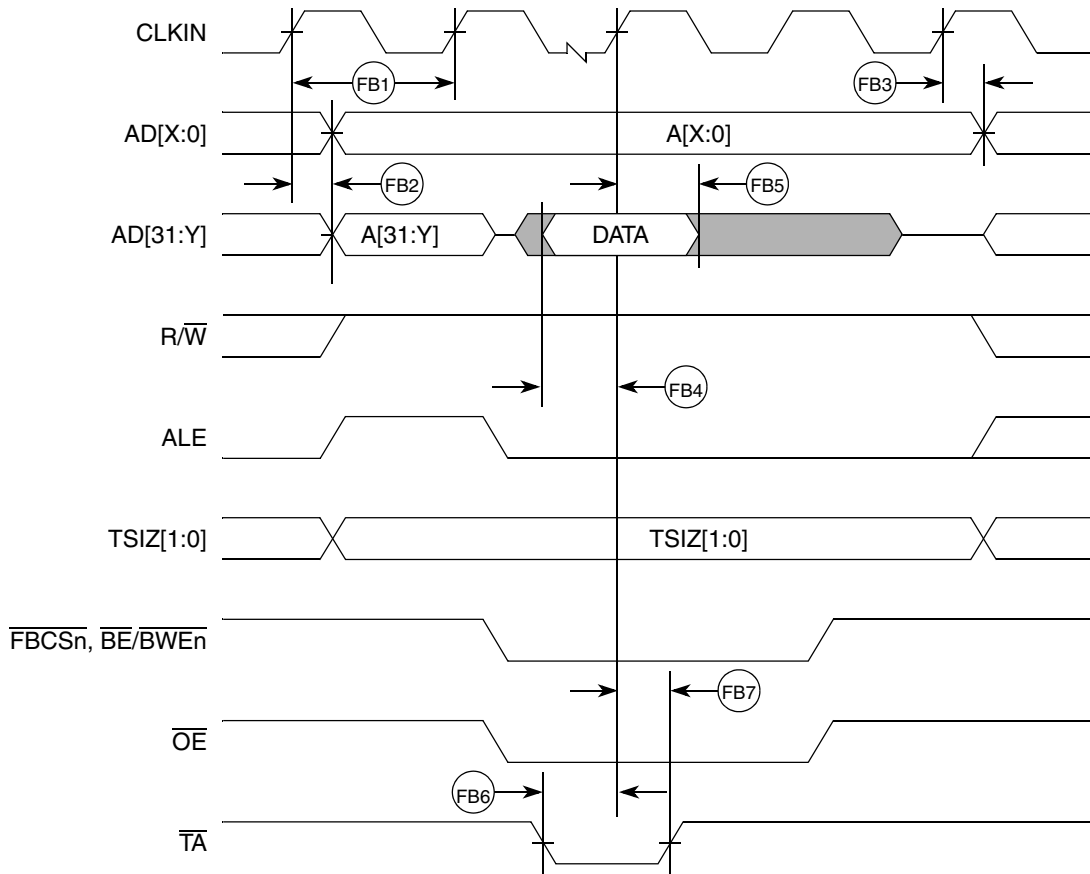


Figure 11. FlexBus Read Timing

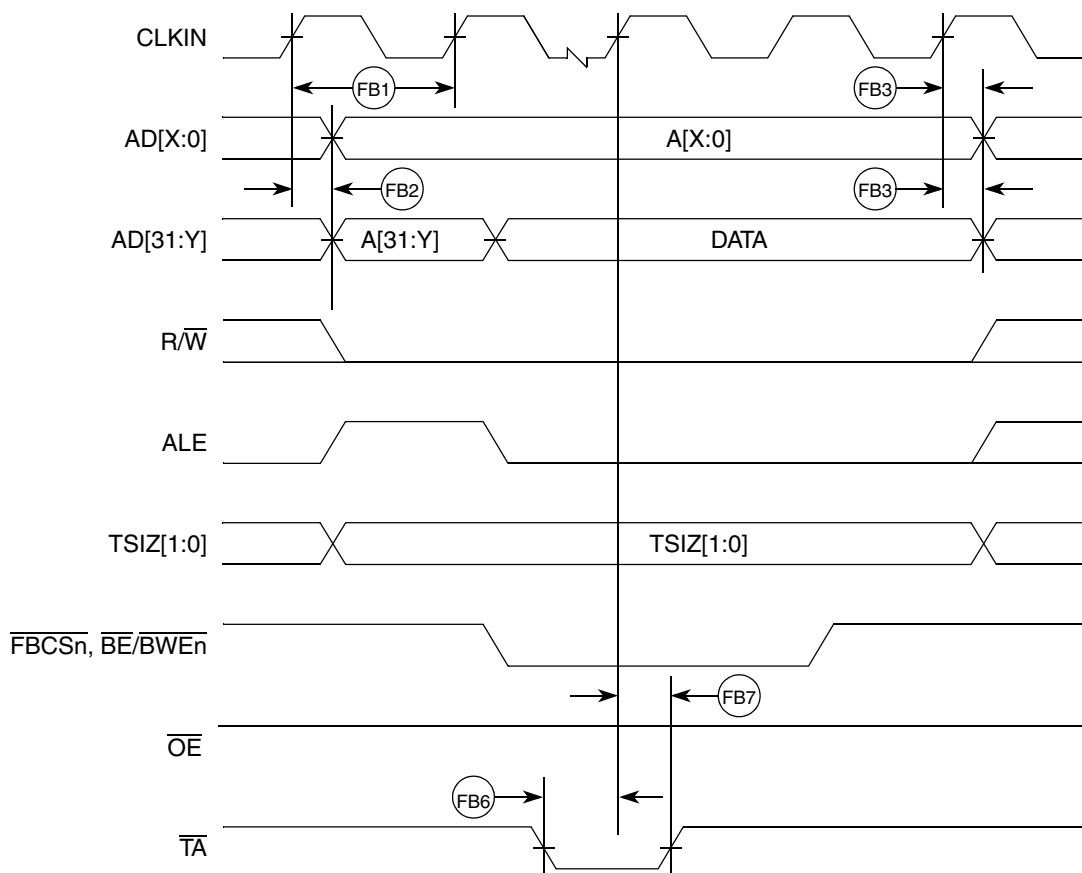


Figure 12. FlexBus Write Timing

9 SDRAM Bus

The SDRAM controller supports accesses to main SDRAM memory from any internal master. It supports standard SDRAM or double data rate (DDR) SDRAM, but it does not support both at the same time. The SDRAM controller uses SSTL2 and SSTL3 I/O drivers. Both SSTL drive modes are programmable for Class I or Class II drive strength.

9.1 SDR SDRAM AC Timing Characteristics

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the memory bus clock, when operating in SDR mode on write cycles and relative to SDR_DQS on read cycles. The MCF548x SDRAM controller is a DDR controller that has an SDR mode. Because it is designed to support DDR, a DQS pulse must be supplied to the MCF548x for each data beat of an SDR read. The MCF548x accomplishes this by asserting a signal called SDR_DQS during read cycles. Care must be taken during board design to adhere to the following guidelines and specs with regard to the SDR_DQS signal and its usage.

Table 11. SDR Timing Specifications

| Symbol | Characteristic | Min | Max | Unit | Notes |
|--------|---|--|---|-------|-------|
| | Frequency of Operation | 0 | 133 | Mhz | 1 |
| SD1 | Clock Period (t_{CK}) | 7.52 | 12 | ns | 2 |
| SD2 | Clock Skew (t_{SK}) | | TBD | | |
| SD3 | Pulse Width High (t_{CKH}) | 0.45 | 0.55 | SDCLK | 3 |
| SD4 | Pulse Width Low (t_{CKL}) | 0.45 | 0.55 | SDCLK | 4 |
| SD5 | Address, CKE, CAS, RAS, WE, BA, CS - Output Valid (t_{CMV}) | | $0.5 \times \text{SDCLK} + 1.0\text{ns}$ | ns | |
| SD6 | Address, CKE, CAS, RAS, WE, BA, CS - Output Hold (t_{CMH}) | 2.0 | | ns | |
| SD7 | SDRDQS Output Valid (t_{DQSOV}) | | Self timed | ns | 5 |
| SD8 | SDDQS[3:0] input setup relative to SDCLK ($t_{DQSI S}$) | $0.25 \times \text{SDCLK}$ | $0.40 \times \text{SDCLK}$ | ns | 6 |
| SD9 | SDDQS[3:0] input hold relative to SDCLK (t_{DQSIH}) | Does not apply. 0.5 SDCLK fixed width. | | | 7 |
| SD10 | Data Input Setup relative to SDCLK (reference only) (t_{DIS}) | $0.25 \times \text{SDCLK}$ | | ns | 8 |
| SD11 | Data Input Hold relative to SDCLK (reference only) (t_{DIH}) | 1.0 | | ns | |
| SD12 | Data and Data Mask Output Valid (t_{DV}) | | $0.75 \times \text{SDCLK} + 0.500\text{ns}$ | ns | |
| SD13 | Data and Data Mask Output Hold (t_{DH}) | 1.5 | | ns | |

¹ The frequency of operation is 2x or 4x the CLKIN frequency of operation. The MCF548X supports a single external reference clock (CLKIN). This signal defines the frequency of operation for FlexBus and PCI, but SDRAM clock operates at the same frequency as the internal bus clock. Please see the PLL chapter of the *MCF548X Reference Manual* for more information on setting the SDRAM clock rate.

² SDCLK is one SDRAM clock in (ns).

³ Pulse width high plus pulse width low cannot exceed min and max clock period.

⁴ Pulse width high plus pulse width low cannot exceed min and max clock period.

⁵ SDR_DQS is designed to pulse 0.25 clock before the rising edge of the memory clock. This is a guideline only. Subtle variation from this guideline is expected. SDR_DQS only pulses during a read cycle and one pulse occurs for each data beat.

⁶ SDR_DQS is designed to pulse 0.25 clock before the rising edge of the memory clock. This spec is a guideline only. Subtle variation from this guideline is expected. SDR_DQS only pulses during a read cycle and one pulse occurs for each data beat.

⁷ The SDR_DQS pulse is designed to be 0.5 clock in width. The timing of the rising edge is most important. The falling edge does not affect the memory controller.

⁸ Because a read cycle in SDR mode uses the DQS circuit within the MCF548X, it is most critical that the data valid window be centered 1/4 clk after the rising edge of DQS. Ensuring that this happens results in successful SDR reads. The input setup spec is provided as guidance.

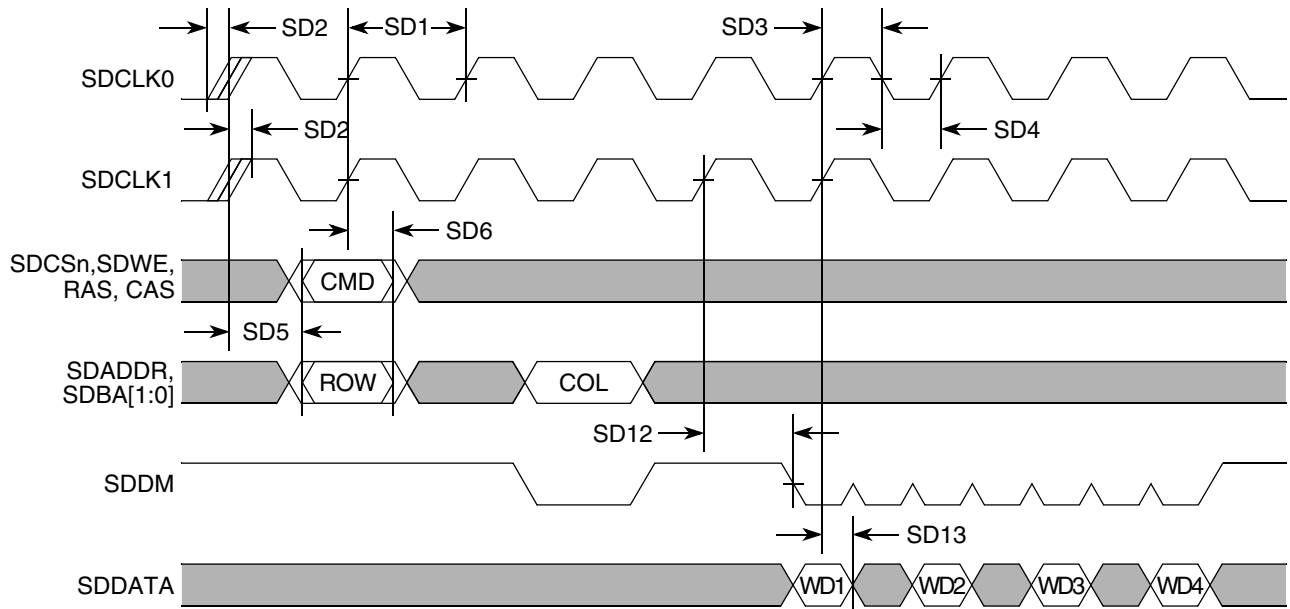
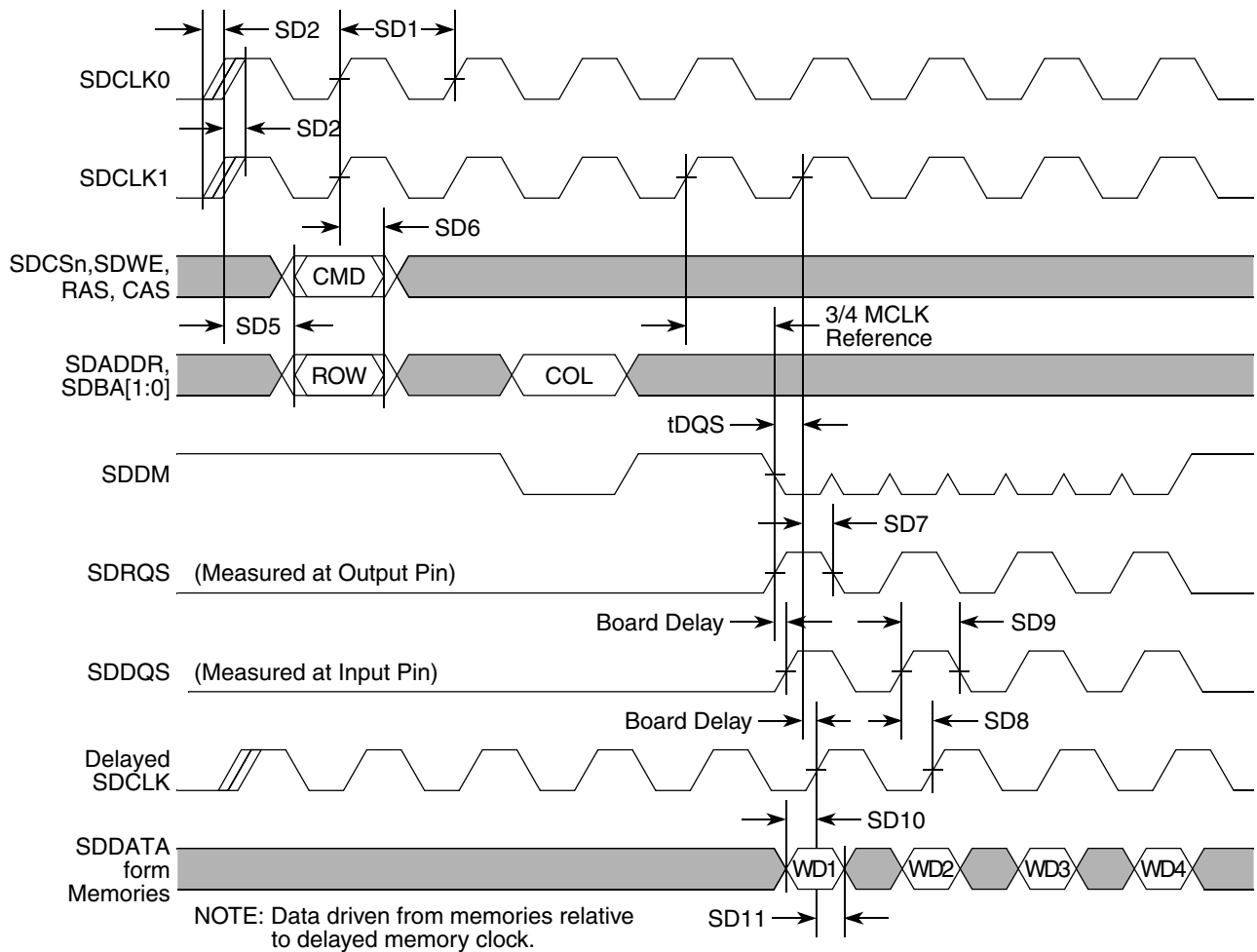


Figure 13. SDR Write Timing



NOTE: Data driven from memories relative to delayed memory clock.

Figure 14. SDR Read Timing

9.2 DDR SDRAM AC Timing Characteristics

When using the DDR SDRAM controller, the following timing numbers must be followed to properly latch or drive data onto the memory bus. All timing numbers are relative to the four DQS byte lanes.

Table 12 shows the DDR clock crossover specifications.

Table 12. DDR Clock Crossover Specifications

| Symbol | Characteristic | Min | Max | Unit |
|-----------|--|------|--------------|------|
| V_{MP} | Clock output mid-point voltage | 1.05 | 1.45 | V |
| V_{OUT} | Clock output voltage level | -0.3 | SD_VDD + 0.3 | V |
| V_{ID} | Clock output differential voltage (peak to peak swing) | 0.7 | SD_VDD + 0.6 | V |
| V_{IX} | Clock crossing point voltage ¹ | 1.05 | 1.45 | V |

¹ The clock crossover voltage is only guaranteed when using the highest drive strength option for the SDCLK[1:0] and SDCLK[1:0] signals.

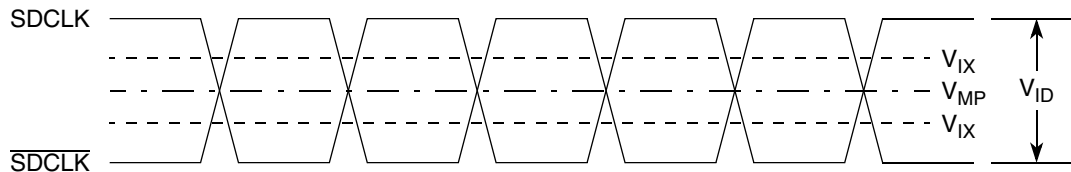


Figure 15. DDR Clock Timing Diagram

Table 13. DDR Timing Specifications

| Symbol | Characteristic | Min | Max | Unit | Notes |
|--------|---|---|--|-------|--------|
| | Frequency of Operation | 50 ¹ | 133 | MHz | 2 |
| DD1 | Clock Period (t_{CK}) | 7.52 | 12 | ns | 3 |
| DD2 | Pulse Width High (t_{CKH}) | 0.45 | 0.55 | SDCLK | 4 |
| DD3 | Pulse Width Low (t_{CKL}) | 0.45 | 0.55 | SDCLK | 5 |
| DD4 | Address, SDCKE, \overline{CAS} , \overline{RAS} , \overline{WE} , SDBA, \overline{SDCS} —Output Valid (t_{CMV}) | — | $0.5 \times \text{SDCLK} + 1.0 \text{ ns}$ | ns | 6 |
| DD5 | Address, SDCKE, \overline{CAS} , \overline{RAS} , \overline{WE} , SDBA, \overline{SDCS} —Output Hold (t_{CMH}) | 2.0 | — | ns | |
| DD6 | Write Command to first DQS Latching Transition (t_{DQSS}) | — | 1.25 | SDCLK | |
| DD7 | Data and Data Mask Output Setup (DQ→DQS) Relative to DQS (DDR Write Mode) (t_{QS}) | 1.0 | — | ns | 7 8 |
| DD8 | Data and Data Mask Output Hold (DQS→DQ) Relative to DQS (DDR Write Mode) (t_{QH}) | 1.0 | — | ns | 9 |
| DD9 | Input Data Skew Relative to DQS (Input Setup) (t_{IS}) | | 1 | ns | 10 |
| DD10 | Input Data Hold Relative to DQS (t_{IH}) | $0.25 \times \text{SDCLK} + 0.5 \text{ ns}$ | — | ns | 11 |
| DD11 | DQS falling edge to SDCLK rising (output setup time) (t_{DSS}) | 0.5 | — | ns | |
| DD12 | DQS falling edge from SDCLK rising (output hold time) (t_{DSH}) | 0.5 | — | ns | |

Table 13. DDR Timing Specifications (continued)

| Symbol | Characteristic | Min | Max | Unit | Notes |
|--------|---|------|-----|-------|-------|
| DD13 | DQS input read preamble width (t_{RPRE}) | 0.9 | 1.1 | SDCLK | |
| DD14 | DQS input read postamble width (t_{RPST}) | 0.4 | 0.6 | SDCLK | |
| DD15 | DQS output write preamble width (t_{WPRE}) | 0.25 | — | SDCLK | |
| DD16 | DQS output write postamble width (t_{WPST}) | 0.4 | 0.6 | SDCLK | |

¹ DDR memories typically have a minimum speed specification of 83 MHz. Check memory component specifications to verify.

² The frequency of operation is 2x or 4x the CLKIN frequency of operation. The MCF548X supports a single external reference clock (CLKIN). This signal defines the frequency of operation for FlexBus and PCI, but SDRAM clock operates at the same frequency as the internal bus clock. Please see the reset configuration signals description in the “Signal Descriptions” chapter within the *MCF548x Reference Manual*.

³ SDCLK is one memory clock in (ns).

⁴ Pulse width high plus pulse width low cannot exceed max clock period.

⁵ Pulse width high plus pulse width low cannot exceed max clock period.

⁶ Command output valid should be 1/2 the memory bus clock (SDCLK) plus some minor adjustments for process, temperature, and voltage variations.

⁷ This specification relates to the required input setup time of today's DDR memories. SDDATA[31:24] is relative to SDDQS3, SDDATA[23:16] is relative to SDDQS2, SDDATA[15:8] is relative to SDDQS1, and SDDATA[7:0] is relative SDDQS0.

⁸ The first data beat is valid before the first rising edge of SDDQS and after the SDDQS write preamble. The remaining data beats is valid for each subsequent SDDQS edge.

⁹ This specification relates to the required hold time of today's DDR memories. SDDATA[31:24] is relative to SDDQS3, SDDATA[23:16] is relative to SDDQS2, SDDATA[15:8] is relative to SDDQS1, and SDDATA[7:0] is relative SDDQS0.

¹⁰ Data input skew is derived from each SDDQS clock edge. It begins with a SDDQS transition and ends when the last data line becomes valid. This input skew must include DDR memory output skew and system level board skew (due to routing or other factors).

¹¹ Data input hold is derived from each SDDQS clock edge. It begins with a SDDQS transition and ends when the first data line becomes invalid.

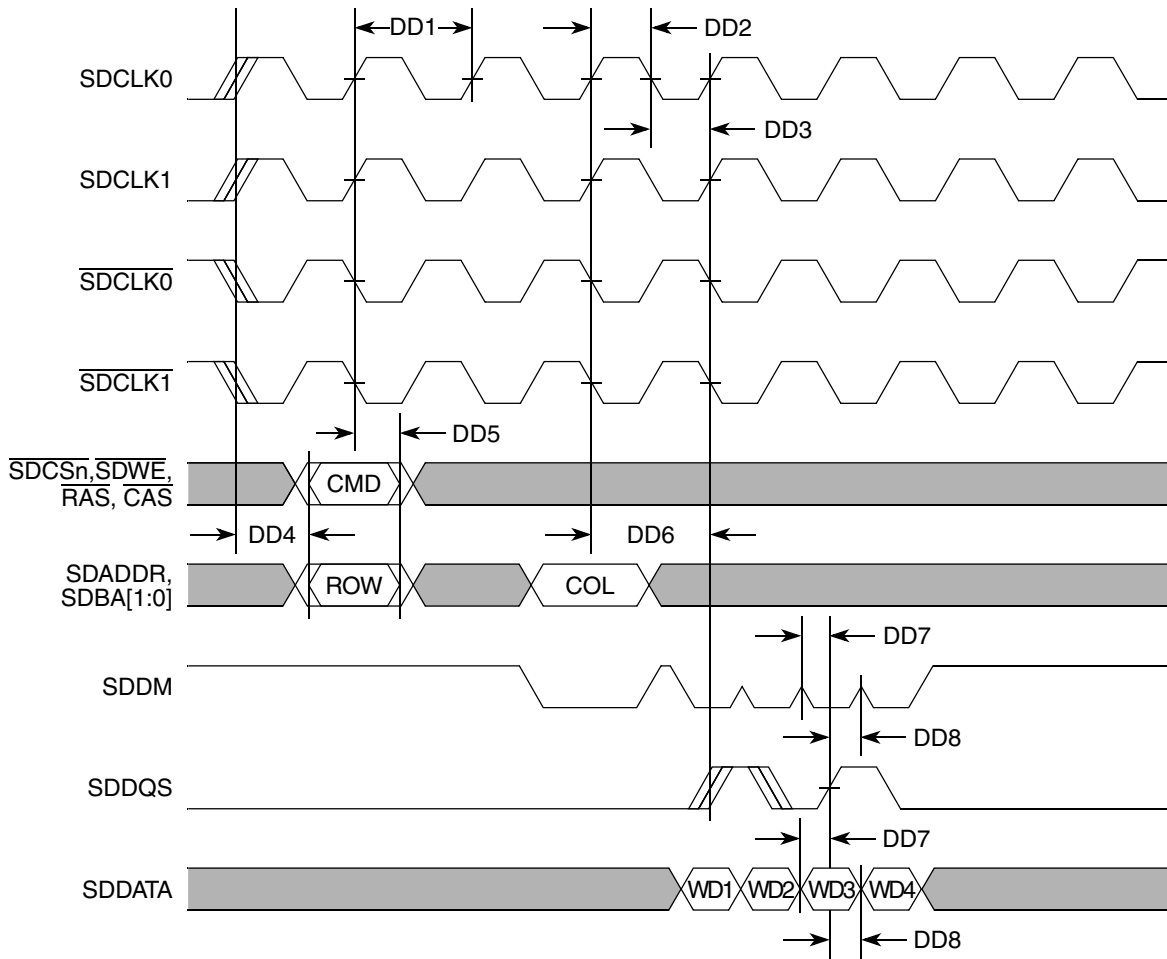


Figure 16. DDR Write Timing

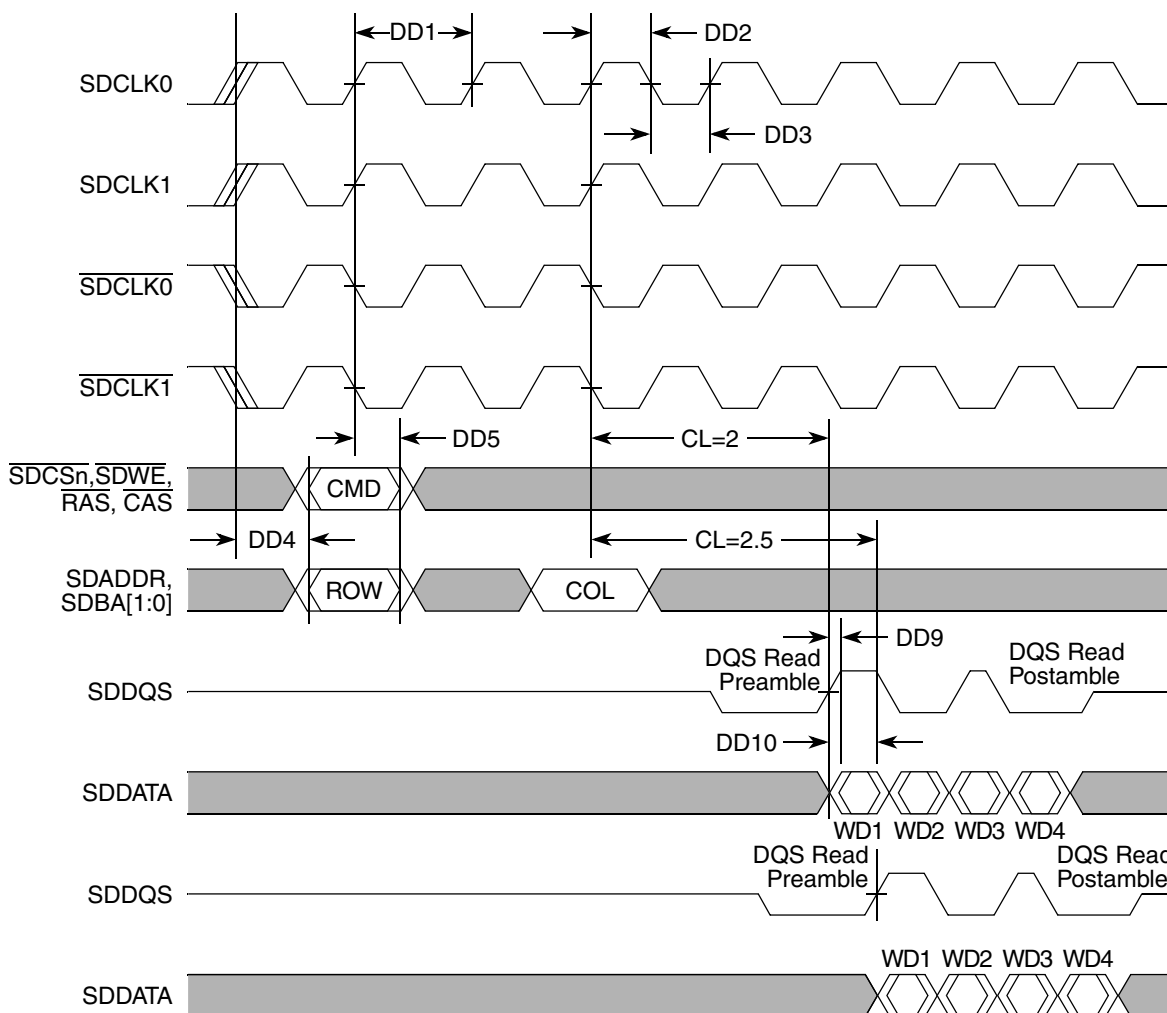


Figure 17. DDR Read Timing

10 PCI Bus

The PCI bus on the MCF548x is PCI 2.2 compliant. The following timing numbers are mostly from the PCI 2.2 spec. Please refer to the PCI 2.2 spec for a more detailed timing analysis.

Table 14. PCI Timing Specifications

| Num | Characteristic | Min | Max | Unit | Notes |
|-----|---|-----|------|------|-------|
| | Frequency of Operation | 25 | 50 | MHz | 1 |
| P1 | Clock Period (t_{CK}) | 20 | 40 | ns | 2 |
| P2 | Address, Data, and Command ($33 < \text{PCI} \leq 50 \text{ Mhz}$)—Input Setup (t_{IS}) | 3.0 | — | ns | |
| P3 | Address, Data, and Command ($0 < \text{PCI} \leq 33 \text{ Mhz}$)—Input Setup (t_{IS}) | 7.0 | — | ns | |
| P4 | Address, Data, and Command ($33\text{--}50 \text{ Mhz}$)—Output Valid (t_{DV}) | — | 6.0 | ns | 3 |
| P5 | Address, Data, and Command ($0\text{--}33 \text{ Mhz}$) - Output Valid (t_{DV}) | — | 11.0 | ns | |
| P6 | PCI signals ($0\text{--}50 \text{ Mhz}$) - Output Hold (t_{DH}) | 0 | — | ns | 4 |

Table 14. PCI Timing Specifications (continued)

| Num | Characteristic | Min | Max | Unit | Notes |
|-----|---|-----|-----|------|-------|
| P7 | PCI signals (0–50 Mhz) - Input Hold (t_{IH}) | 0 | — | ns | 5 |
| P8 | PCI REQ/GNT ($33 < \text{PCI} \leq 50\text{Mhz}$) - Output valid (t_{DV}) | — | 6 | ns | 6 |
| P9 | PCI REQ/GNT ($0 < \text{PCI} \leq 33\text{Mhz}$) - Output valid (t_{DV}) | — | 12 | ns | |
| P10 | PCI REQ/GNT ($33 < \text{PCI} \leq 50\text{Mhz}$) - Input Setup (t_{IS}) | — | 5 | ns | |
| P11 | PCI REQ ($0 < \text{PCI} \leq 33\text{Mhz}$) - Input Setup (t_{IS}) | 12 | — | ns | |
| P12 | PCI GNT ($0 < \text{PCI} \leq 33\text{Mhz}$) - Input Setup (t_{IS}) | 10 | — | ns | |

¹ Please see the reset configuration signals description in the “Signal Descriptions” chapter within the *MCF548x Reference Manual*. Also specific guidelines may need to be followed when operating the system PLL below certain frequencies.

² Max cycle rate is determined by CLKIN and how the user has the system PLL configured.

³ All signals defined as PCI based signals. Does not include PTP (point-to-point) signals.

⁴ PCI 2.2 spec does not require an output hold time. Although the MCF548X may provide a slight amount of hold, it is not required or guaranteed.

⁵ PCI 2.2 spec requires zero input hold.

⁶ These signals are defined at PTP (Point-to-point) in the PCI 2.2 spec.

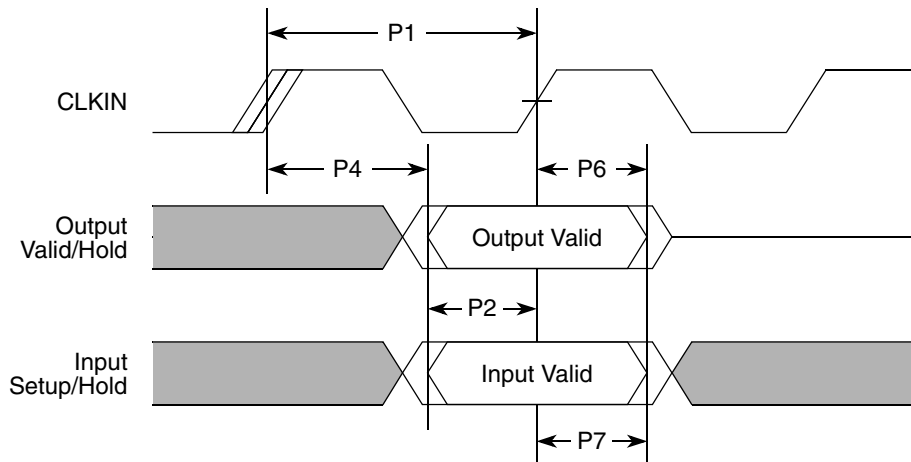


Figure 18. PCI Timing

11 Fast Ethernet AC Timing Specifications

11.1 MII/7-WIRE Interface Timing Specs

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the EMAC_10_100 I/O signals.

The following timing specs meet the requirements for MII and 7-Wire style interfaces for a range of transceiver devices. If this interface is to be used with a specific transceiver device the timing specs may be altered to match that specific transceiver.

Table 15. MII Receive Signal Timing

| Num | Characteristic | Min | Max | Unit |
|-----|-------------------------------------|-----|-----|--------------|
| M1 | RXD[3:0], RXDV, RXER to RXCLK setup | 5 | — | ns |
| M2 | RXCLK to RXD[3:0], RXDV, RXER hold | 5 | — | ns |
| M3 | RXCLK pulse width high | 35% | 65% | RXCLK period |
| M4 | RXCLK pulse width low | 35% | 65% | RXCLK period |

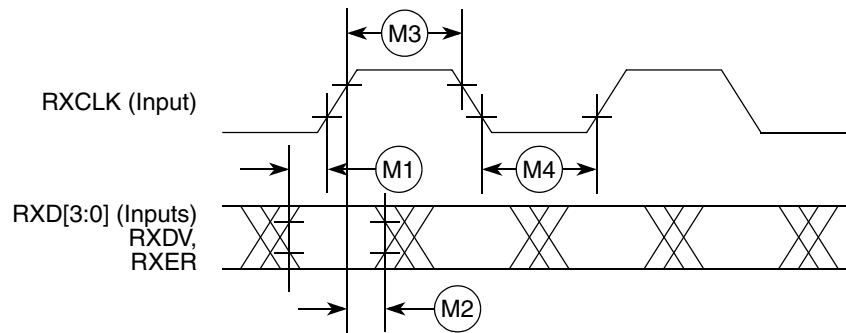


Figure 19. MII Receive Signal Timing Diagram

11.2 MII Transmit Signal Timing

Table 16. MII Transmit Signal Timing

| Num | Characteristic | Min | Max | Unit |
|-----|---------------------------------------|-----|-----|--------------|
| M5 | TXCLK to TXD[3:0], TXEN, TXER invalid | 0 | — | ns |
| M6 | TXCLK to TXD[3:0], TXEN, TXER valid | — | 25 | ns |
| M7 | TXCLK pulse width high | 35% | 65% | TXCLK period |
| M8 | TXCLK pulse width low | 35% | 65% | TXCLK period |

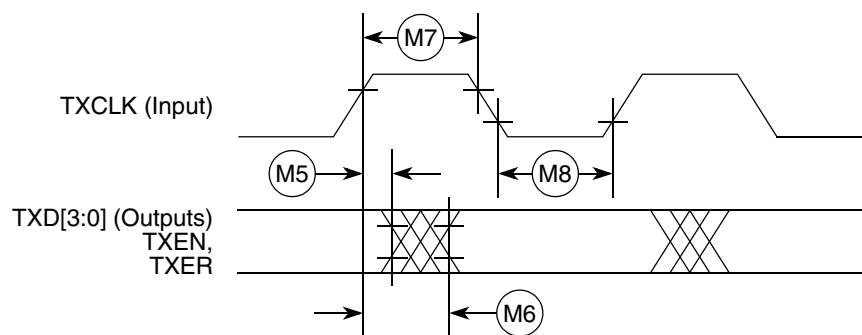


Figure 20. MII Transmit Signal Timing Diagram

11.3 MII Async Inputs Signal Timing (CRS, COL)

Table 17. MII Transmit Signal Timing

| Num | Characteristic | Min | Max | Unit |
|-----|------------------------------|-----|-----|---------------|
| M9 | CRS, COL minimum pulse width | 1.5 | — | TX_CLK period |

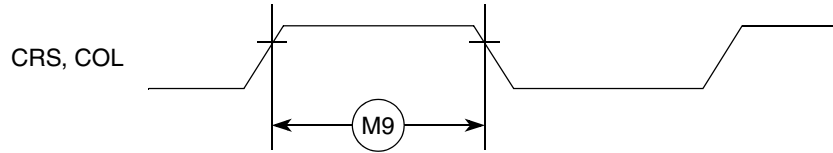


Figure 21. MII Async Inputs Timing Diagram

11.4 MII Serial Management Channel Timing (MDIO, MDC)

Table 18. MII Serial Management Channel Signal Timing

| Num | Characteristic | Min | Max | Unit |
|-----|--|-----|-----|------------|
| M10 | MDC falling edge to MDIO output invalid (min prop delay) | 0 | — | ns |
| M11 | MDC falling edge to MDIO output valid (max prop delay) | — | 25 | ns |
| M12 | MDIO (input) to MDC rising edge setup | 10 | — | ns |
| M13 | MDIO (input) to MDC rising edge hold | 0 | — | ns |
| M14 | MDC pulse width high | 40% | 60% | MDC period |
| M15 | MDC pulse width low | 40% | 60% | MDC period |

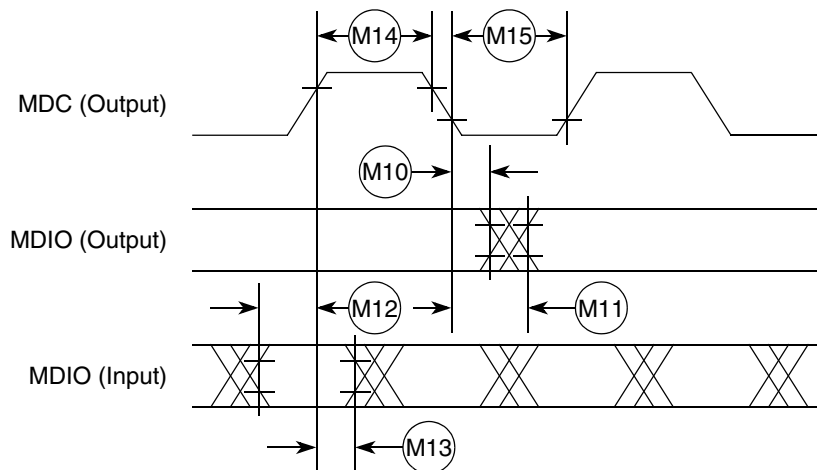


Figure 22. MII Serial Management Channel Timing Diagram

12 General Timing Specifications

Table 19 lists timing specifications for the GPIO, PSC, FlexCAN, \overline{DREQ} , \overline{DACK} , and external interrupts.

Table 19. General AC Timing Specifications

| Name | Characteristic | Min | Max | Unit |
|------|--|-----|-----|--------|
| G1 | CLKIN high to signal output valid | — | 2 | PSTCLK |
| G2 | CLKIN high to signal invalid (output hold) | 0 | — | ns |
| G3 | Signal input pulse width | 2 | — | PSTCLK |

13 I²C Input/Output Timing Specifications

Table 20 lists specifications for the I²C input timing parameters shown in Figure 23.

Table 20. I²C Input Timing Specifications between SCL and SDA

| Num | Characteristic | Min | Max | Units |
|-----|--|-----|-----|------------|
| I1 | Start condition hold time | 2 | — | Bus clocks |
| I2 | Clock low period | 8 | — | Bus clocks |
| I3 | SCL/SDA rise time ($V_{IL} = 0.5\text{ V}$ to $V_{IH} = 2.4\text{ V}$) | — | 1 | mS |
| I4 | Data hold time | 0 | — | ns |
| I5 | SCL/SDA fall time ($V_{IH} = 2.4\text{ V}$ to $V_{IL} = 0.5\text{ V}$) | — | 1 | mS |
| I6 | Clock high time | 4 | — | Bus clocks |
| I7 | Data setup time | 0 | — | ns |
| I8 | Start condition setup time (for repeated start condition only) | 2 | — | Bus clocks |
| I9 | Stop condition setup time | 2 | — | Bus clocks |

Table 21 lists specifications for the I²C output timing parameters shown in Figure 23.

Table 21. I²C Output Timing Specifications between SCL and SDA

| Num | Characteristic | Min | Max | Units |
|-----------------|--|-----|-----|---------------|
| I1 ¹ | Start condition hold time | 6 | — | Bus clocks |
| I2 ¹ | Clock low period | 10 | — | Bus clocks |
| I3 ² | SCL/SDA rise time ($V_{IL} = 0.5\text{ V}$ to $V_{IH} = 2.4\text{ V}$) | — | — | μS |
| I4 ¹ | Data hold time | 7 | — | Bus clocks |
| I5 ³ | SCL/SDA fall time ($V_{IH} = 2.4\text{ V}$ to $V_{IL} = 0.5\text{ V}$) | — | 3 | ns |
| I6 ¹ | Clock high time | 10 | — | Bus clocks |
| I7 ¹ | Data setup time | 2 | — | Bus clocks |
| I8 ¹ | Start condition setup time (for repeated start condition only) | 20 | — | Bus clocks |
| I9 ¹ | Stop condition setup time | 10 | — | Bus clocks |

JTAG and Boundary Scan Timing

- ¹ Output numbers depend on the value programmed into the IFDR; an IFDR programmed with the maximum frequency (IFDR = 0x20) results in minimum output timings as shown in Table 21. The I²C interface is designed to scale the actual data transition time to move it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed into the IFDR; however, the numbers given in Table 21 are minimum values.
- ² Because SCL and SDA are open-collector-type outputs, which the processor can only actively drive low, the time SCL or SDA take to reach a high level depends on external signal capacitance and pull-up resistor values.
- ³ Specified at a nominal 50-pF load.

Figure 23 shows timing for the values in Table 20 and Table 21.

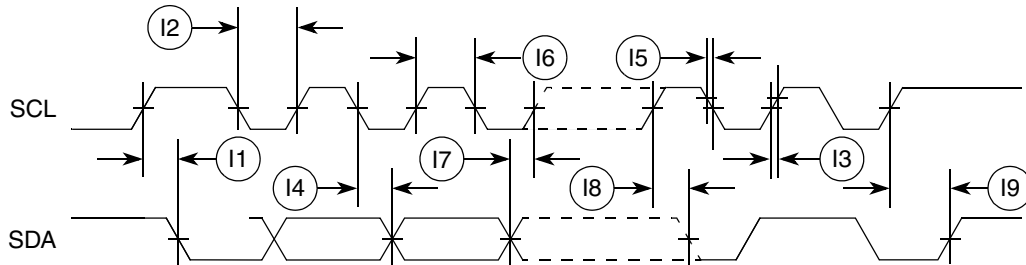


Figure 23. I²C Input/Output Timings

14 JTAG and Boundary Scan Timing

Table 22. JTAG and Boundary Scan Timing

| Num | Characteristics ¹ | Symbol | Min | Max | Unit |
|-----|--|--------------|-------|------|----------|
| J1 | TCLK Frequency of Operation | f_{JCYC} | DC | 10 | MHz |
| J2 | TCLK Cycle Period | t_{JCYC} | 2 | — | t_{CK} |
| J3 | TCLK Clock Pulse Width | t_{JCW} | 15.15 | — | ns |
| J4 | TCLK Rise and Fall Times | t_{JCRF} | 0.0 | 3.0 | ns |
| J5 | Boundary Scan Input Data Setup Time to TCLK Rise | t_{BSDST} | 5.0 | — | ns |
| J6 | Boundary Scan Input Data Hold Time after TCLK Rise | t_{BSDHT} | 24.0 | — | ns |
| J7 | TCLK Low to Boundary Scan Output Data Valid | t_{BSDV} | 0.0 | 15.0 | ns |
| J8 | TCLK Low to Boundary Scan Output High Z | t_{BSDZ} | 0.0 | 15.0 | ns |
| J9 | TMS, TDI Input Data Setup Time to TCLK Rise | t_{TAPBST} | 5.0 | — | ns |
| J10 | TMS, TDI Input Data Hold Time after TCLK Rise | t_{TAPBHT} | 10.0 | — | ns |
| J11 | TCLK Low to TDO Data Valid | t_{TDODV} | 0.0 | 20.0 | ns |
| J12 | TCLK Low to TDO High Z | t_{TDODZ} | 0.0 | 15.0 | ns |
| J13 | \overline{TRST} Assert Time | t_{TRSTAT} | 100.0 | — | ns |
| J14 | \overline{TRST} Setup Time (Negation) to TCLK High | t_{TRSTST} | 10.0 | — | ns |

¹ MTMOD is expected to be a static signal. Hence, it is not associated with any timing

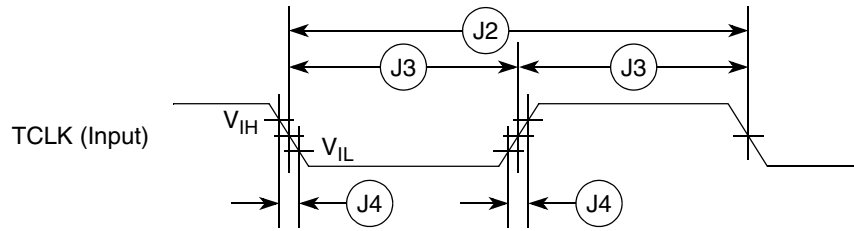


Figure 24. Test Clock Input Timing

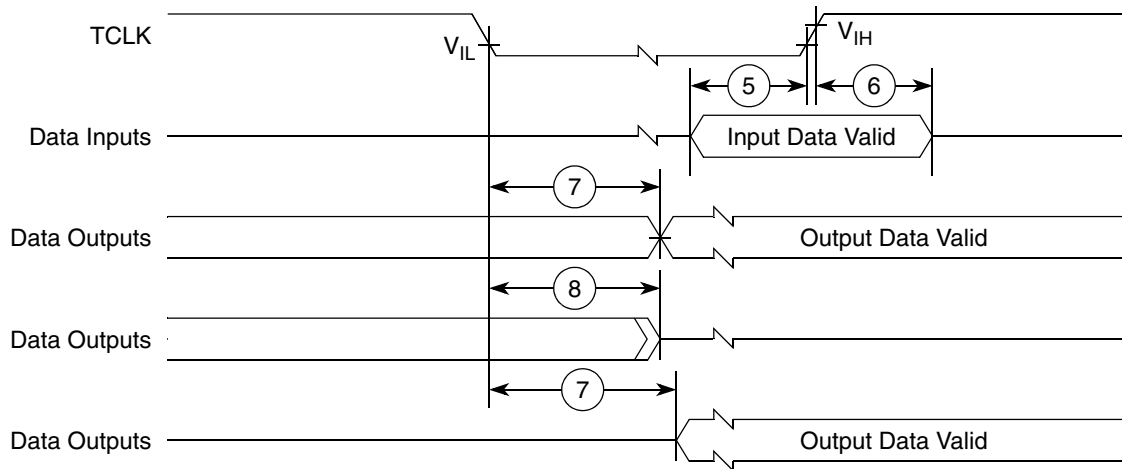


Figure 25. Boundary Scan (JTAG) Timing

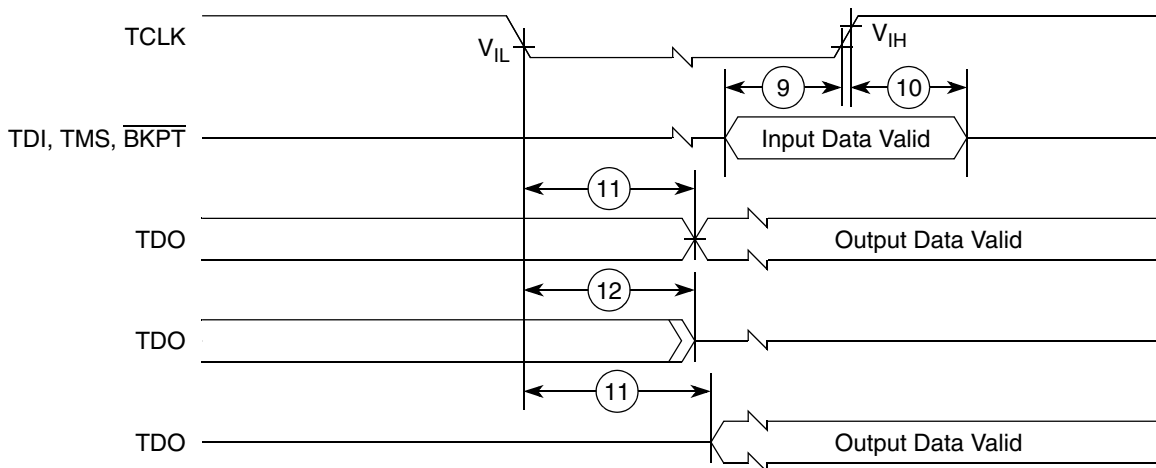


Figure 26. Test Access Port Timing

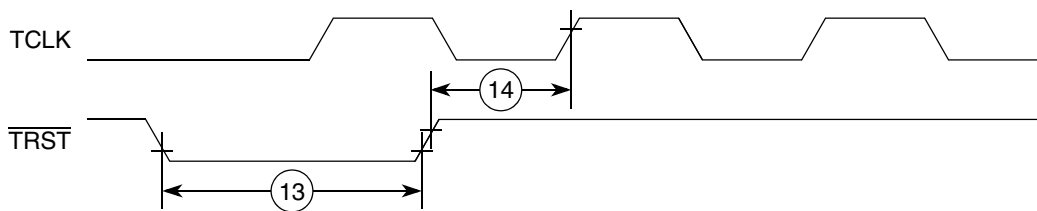


Figure 27. TRST Timing Debug AC Timing Specifications

JTAG and Boundary Scan Timing

Table 23 lists specifications for the debug AC timing parameters shown in Figure 29.

Table 23. Debug AC Timing Specifications

| Num | Characteristic | 50 MHz | | Units |
|-----------------|--------------------------|--------|-----|---------|
| | | Min | Max | |
| D1 | PSTDDATA to PSTCLK setup | 4.5 | — | ns |
| D2 | PSTCLK to PSTDDATA hold | 4.5 | — | ns |
| D3 | DSI-to-DSCLK setup | 1 | — | PSTCLKs |
| D4 ¹ | DSCLK-to-DSO hold | 4 | — | PSTCLKs |
| D5 | DSCLK cycle time | 5 | — | PSTCLKs |

¹ DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of CLKOUT.

Figure 28 shows real-time trace timing for the values in Table 23.

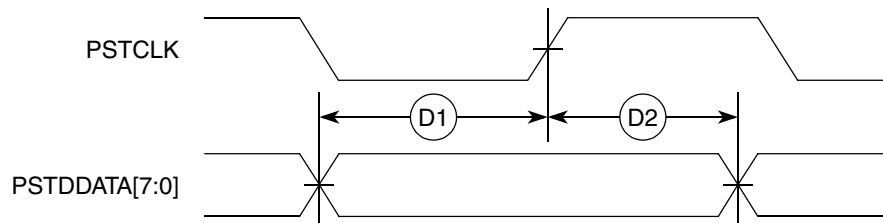


Figure 28. Real-Time Trace AC Timing

Figure 29 shows BDM serial port AC timing for the values in Table 23.

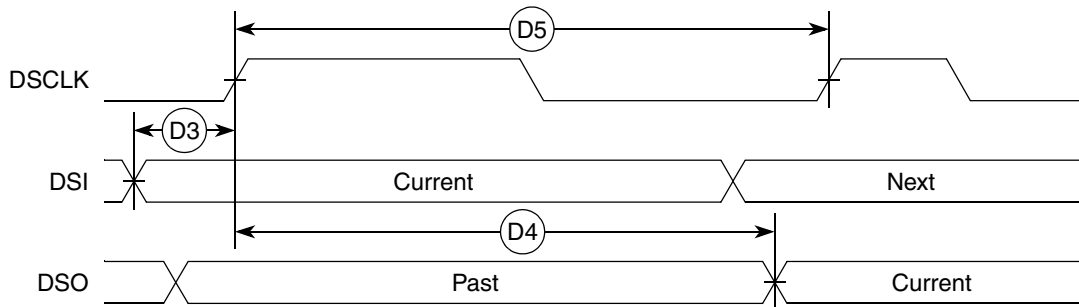


Figure 29. BDM Serial Port AC Timing

15 DSPI Electrical Specifications

Table 24 lists DSPI timings.

Table 24. DSPI Modules AC Timing Specifications

| Name | Characteristic | Min | Max | Unit |
|------|---|---------|-----------|------|
| DS1 | DSPI_CS[3:0] to DSPI_CLK | 1 × tck | 510 × tck | ns |
| DS2 | DSPI_CLK high to DSPI_DOUT valid. | — | 12 | ns |
| DS3 | DSPI_CLK high to DSPI_DOUT invalid. (Output hold) | 2 | — | ns |
| DS4 | DSPI_DIN to DSPI_CLK (Input setup) | 10 | — | ns |
| DS5 | DSPI_DIN to DSPI_CLK (Input hold) | 10 | — | ns |

The values in Table 24 correspond to Figure 30.

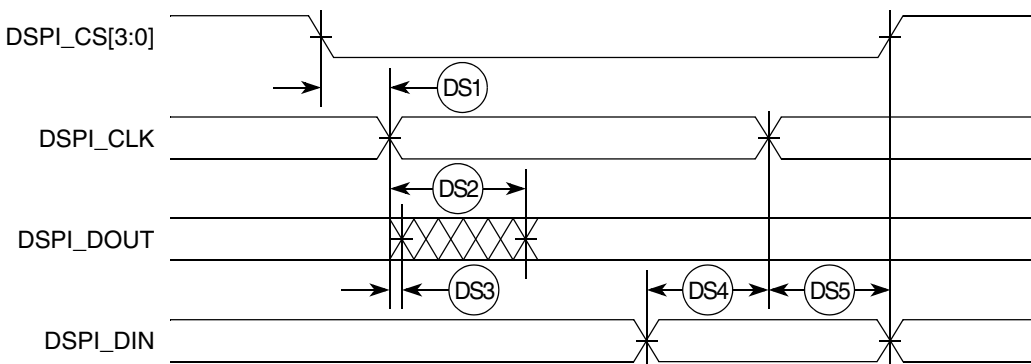


Figure 30. DSPI Timing

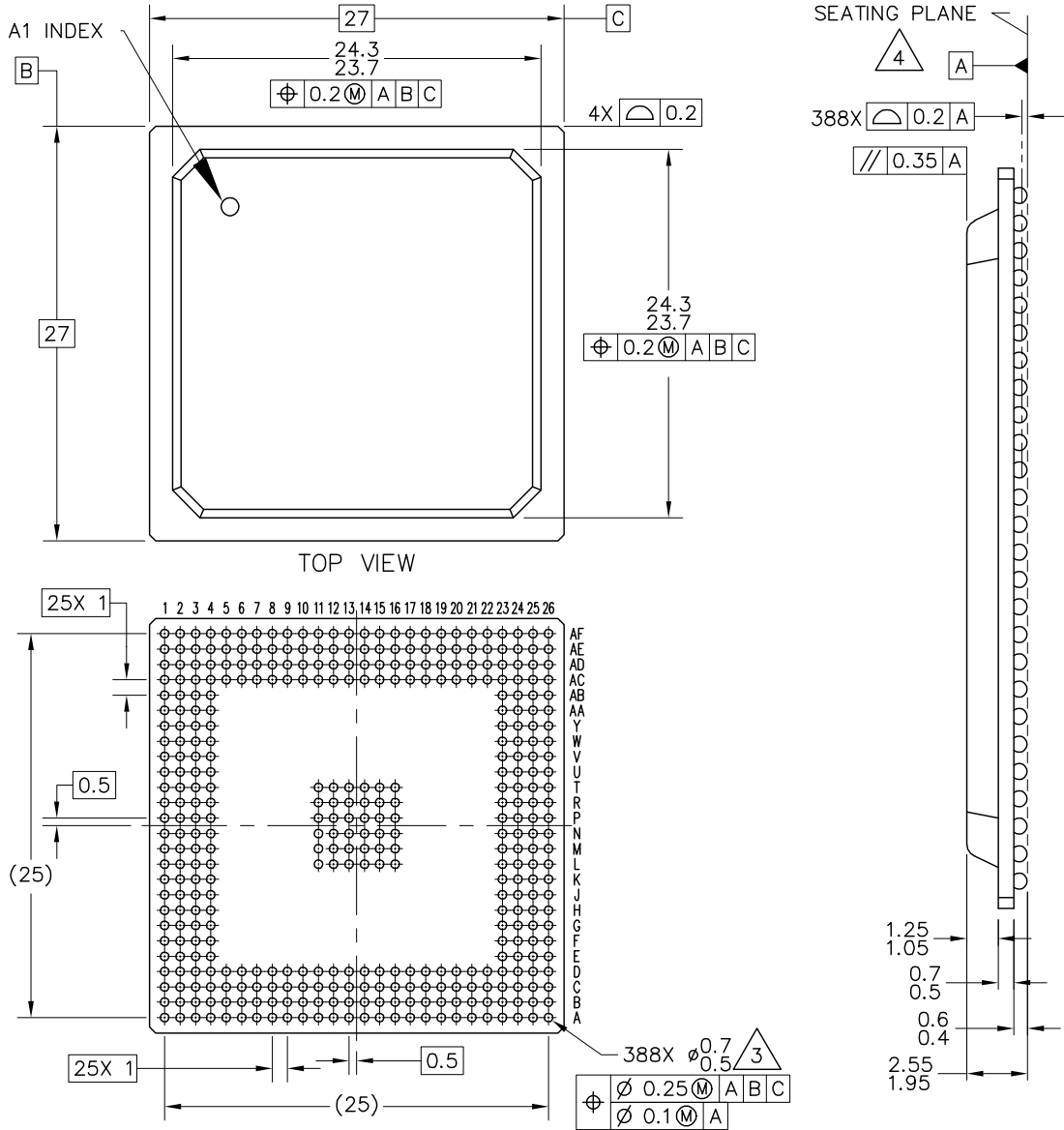
16 Timer Module AC Timing Specifications

Table 25 lists timer module AC timings.

Table 25. Timer Module AC Timing Specifications

| Name | Characteristic | 0–50 MHz | | Unit |
|------|---------------------------------------|----------|-----|--------|
| | | Min | Max | |
| T1 | TIN0 / TIN1 / TIN2 / TIN3 cycle time | 3 | — | PSTCLK |
| T2 | TIN0 / TIN1 / TIN2 / TIN3 pulse width | 1 | — | PSTCLK |

17 Case Drawing



| | | | | | |
|--|--|------------------------------|--|---|--|
| © FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED. | | MECHANICAL OUTLINE | | SIDE VIEW PRINT VERSION NOT TO SCALE | |
| TITLE: 388 I/O, PBGA 27 X 27 PKG, 1 MM PITCH (OMPAC) | | DOCUMENT NO: 98ARS23880W | | REV: C | |
| | | CASE NUMBER: 1164-02 | | 25 JAN 2007 | |
| | | STANDARD: JEDEC MS-034 AAL-1 | | | |

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PACKAGE CODES:
 5254 - 2 LAYER SUBSTRATE PACKAGE
 5367 - 4 LAYER SUBSTRATE PACKAGE

| | | | |
|---|------------------------------|----------------------------|--|
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| | CASE NUMBER: 1164-02 | 25 JAN 2007 | |
| | STANDARD: JEDEC MS-034 AAL-1 | | |

Figure 31. 388-pin BGA Case Outline

18 Revision History

| Revision Number | Date | Substantive Changes |
|-----------------|-------------------|--|
| 2.2 | August 29, 2005 | Table 7 : Changed C1 minimum spec from 15.15 ns to 20 ns and maximum spec from 33.3 ns to 40 ns. |
| 2.3 | August 30, 2005 | Table 22 : Changed J11 maximum from 15 ns to 20 ns. |
| 2.4 | December 14, 2005 | <p>Table 9: Changed heading maximum from 66 MHz to 50 MHz.</p> <p>Table 10: Changed frequency of operation maximum from 66 MHz to 50 MHz and corresponding FB1 minimum from 15.15 ns to 20 ns.</p> <p>Table 10: Changed FB1 maximum from 33.33 ns to 40 ns.</p> <p>Table 14: Changed frequency of operation maximum from 66 MHz to 50 MHz and corresponding FB1 minimum from 15.15 ns to 20 ns.</p> <p>Table 14: Changed FB1 maximum from 33.33 ns to 40 ns.</p> <p>Table 14: Changed various entry descriptions from “(33 < PCI ≤ 66 Mhz)” to (33 < PCI ≤ 50 Mhz)</p> <p>Table 23: Changed heading maximum from 66 MHz to 50 MHz.</p> <p>Table 25: Changed heading maximum from 66 MHz to 50 MHz.</p> |
| 3 | February 20, 2007 | <p>Table 4: Updated DC electrical specifications, V_{IL} and V_{IH}.</p> <p>Table 6: Changed FlexBus output load from 20pF to 30pF.</p> <p>Added Section 4.3, “General USB Layout Guidelines.”</p> |
| 4 | December 4, 2007 | <p>Figure 2: Changed resistor value from 10W to 10Ω</p> <p>Figure 3: Changed note 1 in from “IVDD should not exceed EVDD, SD VDD or PLL VDD by more than 0.4V...” to “IVDD should not exceed EVDD or SD VDD by more than 0.4V...”</p> <p>Table 3: Updated thermal information for θ_{JMA}, θ_{JB}, and θ_{JC}</p> <p>Table 4: Added input leakage current spec.</p> <p>Table 6: Added footnote regarding pads having balanced source & sink current.</p> <p>Table 9: Added \overline{RSTI} pulse duration spec.</p> <p>Added features list, pinout drawing, block diagram, and case outline.</p> |



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