Freescale Technology Forum

Design Innovation.

Nov 05, 2008

QorIQ™ P1 and P2 Platforms: Multicore for Low-End Networking Applications

PN109

Tiger Chun
Technical Marketing Manager, Asia Networking GTM

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What Are We Announcing?

- Freescale is advancing the move to **embedded multicore** architectures with its new **QorIQ™** communications platforms.
- QorIQ platforms are the **next-generation evolution** of Freescale PowerQUICC® communications processors – and compatible stepping stones to multicore.

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- QorIQ platforms suit applications from the networked home to the service-rich enterprise to the expanding mobile network. They are competitively **very high-performance at very low power consumption** for any given application space.
- Freescale has the **long-term, deep ecosystem** engagements necessary for streamlining the migration to multicore architectures.

The New Platforms and Products

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Five levels of platforms targeting different performance and application capabilities – all built on 45nm process technology

QorIQ P1 Platform
QorIQ P2 Platform
QorIQ P3 Platform
QorIQ P4 Platform
QorIQ P5 Platform

June 2007 Disclosure

QorIQ™ P4 Platform: P4080 8-core processor with CoreNet™ fabric

- Includes Hybrid Simulation Environment from Virtutech

QorIQ P1 & P2 platforms: Pin-compatible processors

- P1020 – dual core
- P1010 – single core
- P1011 – single core
- P2020 – dual core
- P2010 – single core

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QorIQ™ Platform Levels

PLATFORMS / PRODUCTS	DESCRIPTION	APPLICATION EXAMPLES
QorIQ P5 **PRODUCTS:** **To be announced**	**Highest-performing embedded processors**	 Service Provider Routers  Network Admission Control  Storage Networks
QorIQ P4 **PRODUCTS:** **P4080**	**Tap the full potential of multicore with this "many-core" platform**	 Metro Carrier Edge Router  IMS Controller  Radio Network Control  Serving Node Router (GSN)
QorIQ P3 **PRODUCTS:** **To be announced**	**Your first step into true multicore performance**	 Converged Media Gateway  SSL, IPSec, Firewall  Access Gateway
QorIQ P2 **PRODUCTS:** **P2020** **P2010**	**Unprecedented performance per watt in this highly integrated platform**	 Unified Threat Management  VoIP Carrier-Class Media Gateway  Wireless Media Gateway  Basestation
QorIQ P1 **PRODUCTS:** **P1020** **P1011** **P1010**	**A highly integrated, cost-effective, low power platform**	 Integrated Services Router  Network Attached Storage  Home Media Hub

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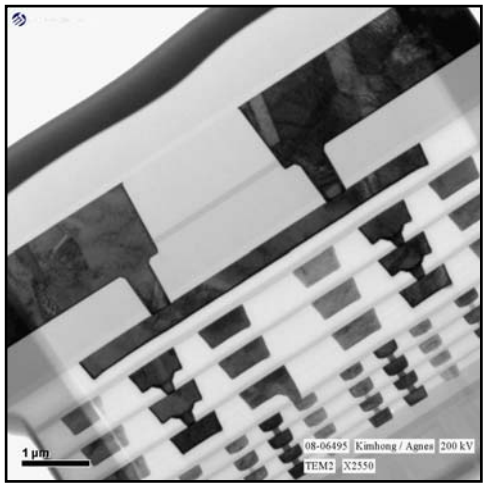
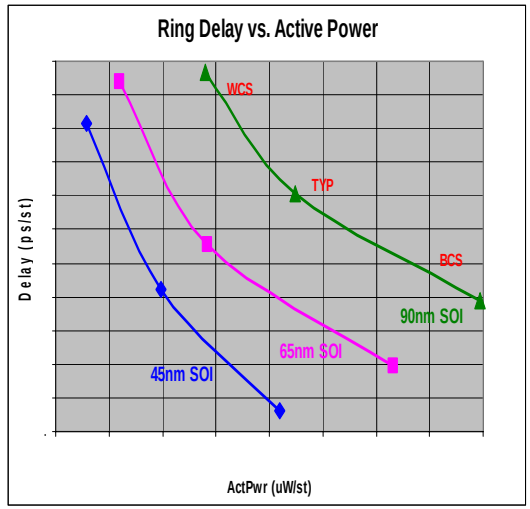
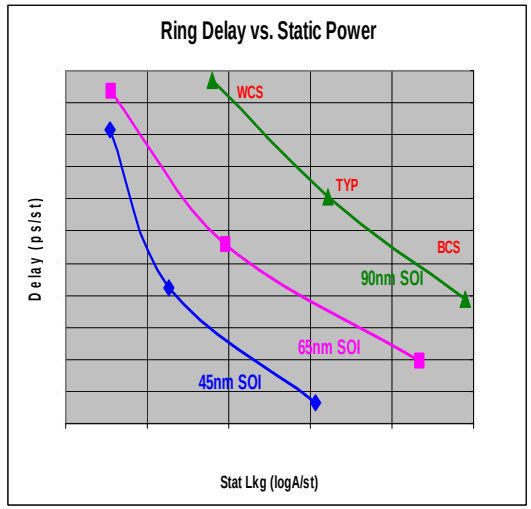
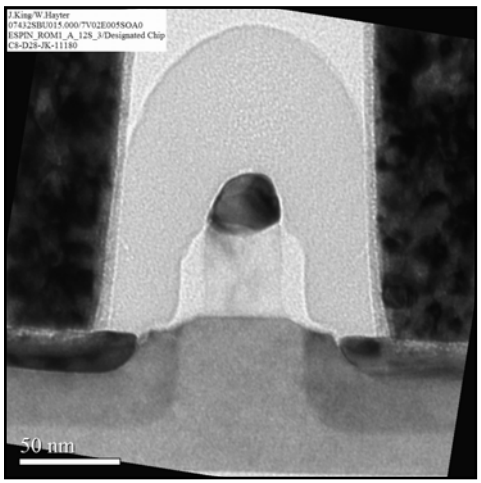
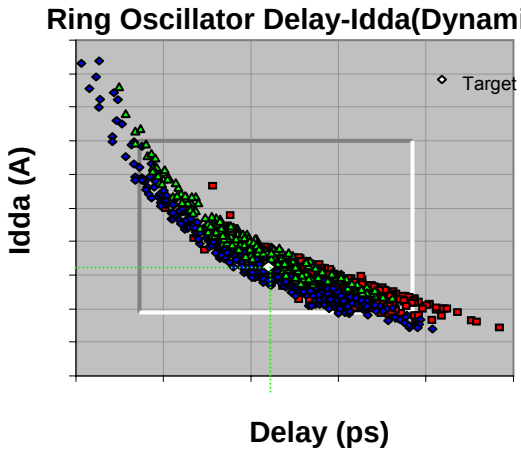
45nm SOI Advantage











45nm SOI Delivers Its Promise

- Active & Static Power Improvement
- Delivered frequency performance
- Scaling for unparalleled packaged performance-power ratio

And retains its strong SER reliability advantage vs. bulk!

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Target Applications

- **Networking (switches and routers)**
  - Line card controller
  - Mid-range line card control plane
  - Low-end line card combined control and data plane
  - Shelf controller
  - Business gateway
  - Multiservice router
  - Wireless access points

- **Telecom**
  - AMC card
  - Controller on ATCA Carrier Card
  - Channel and control card for NodeB, BTS, WCDMA, 4G LTE, WiMax
  - General-purpose compute blade

- **Industrial**
  - Robotics
  - Test/measurement Networking/telecom
  - Multifunction printer
  - Single board computers
  - Industrial applications

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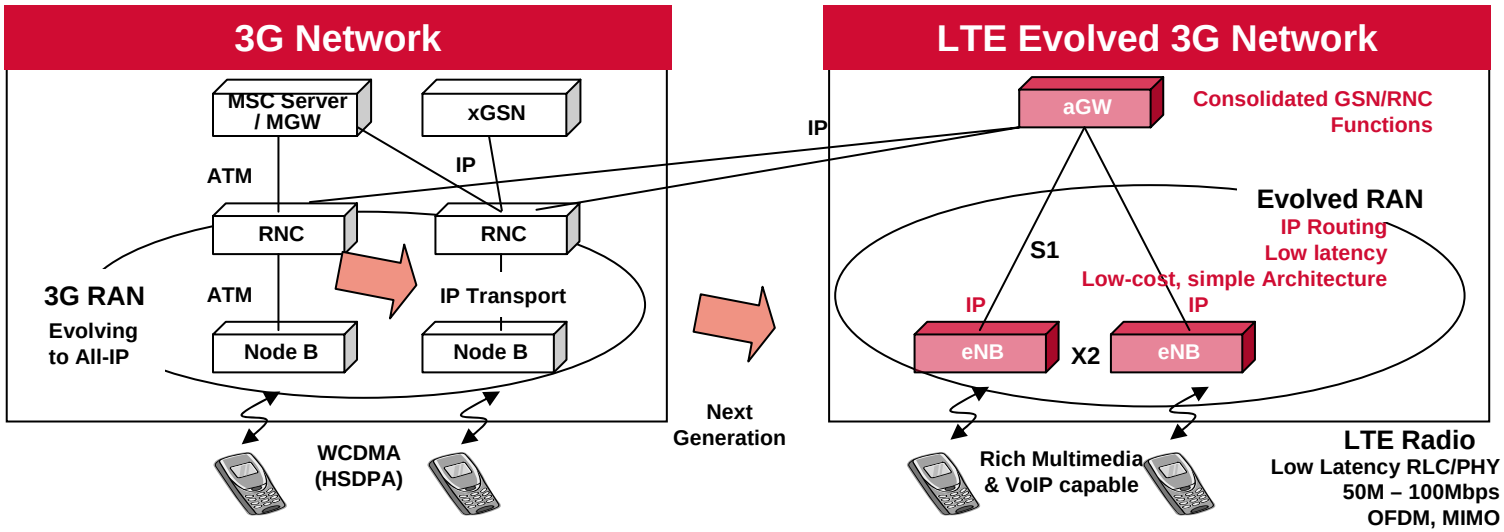
Improved Architectures Enabled



	Existing 3G	LTE Requirement	Impact on Processor
User data-rate (Per Sector)	~300kbps – 14Mbps	> 100Mb/s	Increased processing
Latency	50ms (Rel6) – web browse	10ms (Rel8) – VoIP, gaming	Integration
Hierarchies	Three	Two – lower latency, cost	Higher processing densities in same power budget
Protocols in NodeB (Non-L1)	Control, Scheduler	Radio Bearer, Control, Radio Admission Control, Dynamic Scheduler, Inter Cell Radio Resource Management, Connection Mobility Control, NodeB Measurement, Configuration & Provision, RRC, PDCP, RLC, MAC	Intelligence required

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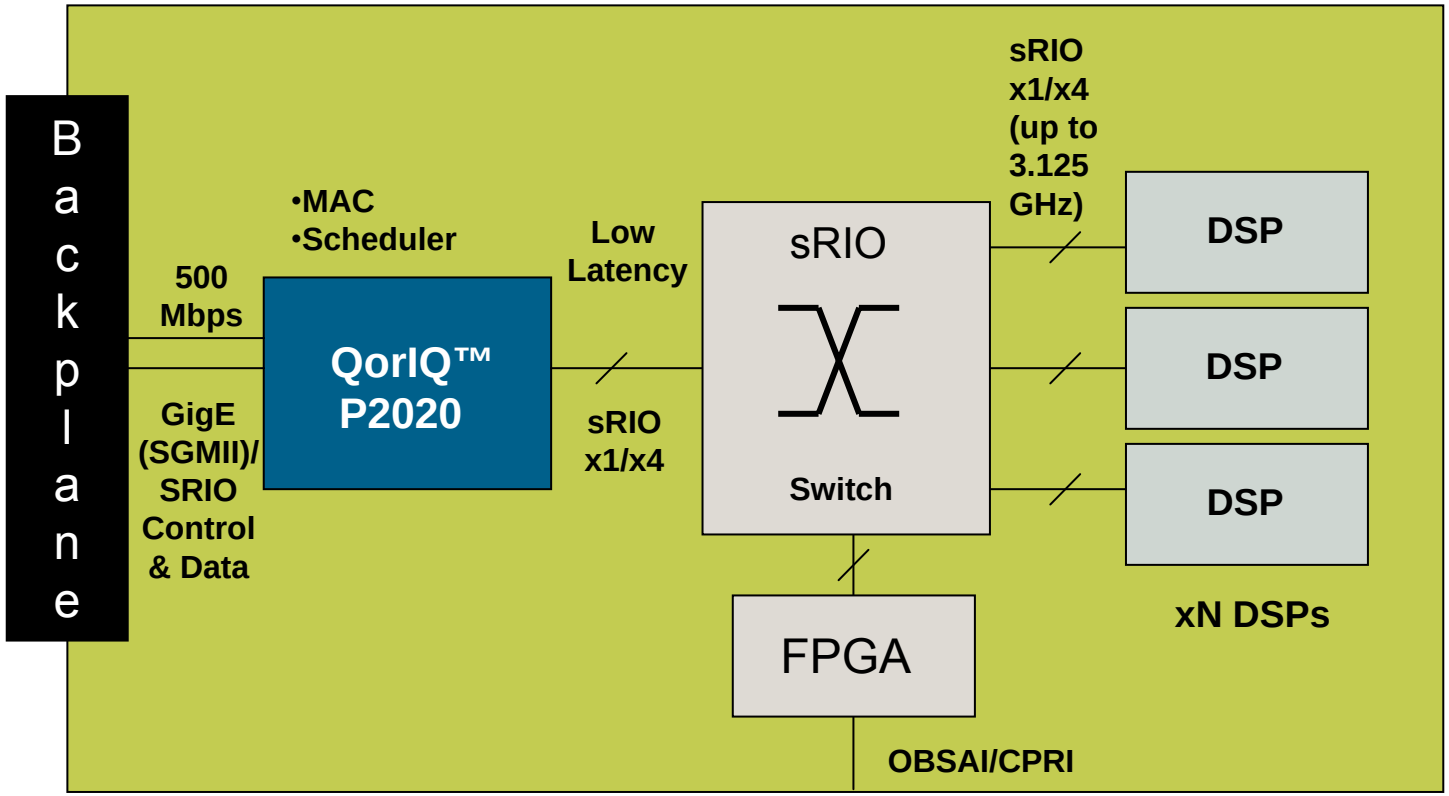
LTE / WiMAX Baseband Applications



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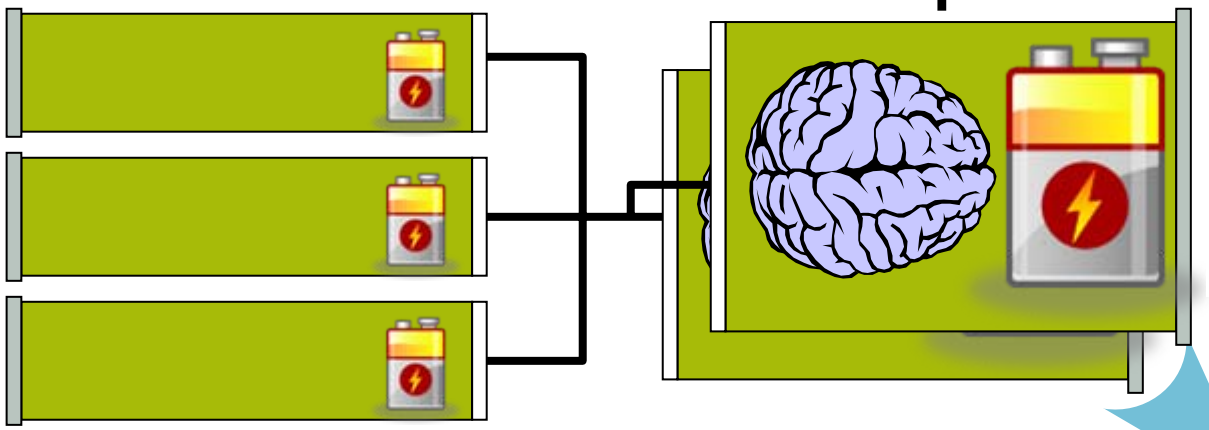
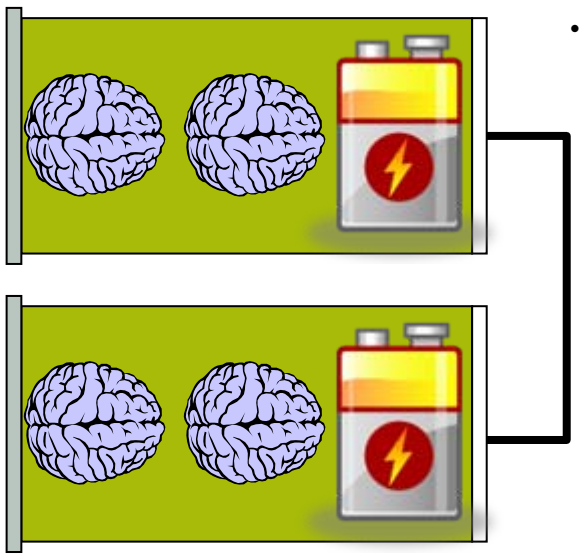
Improved Architectures Enabled



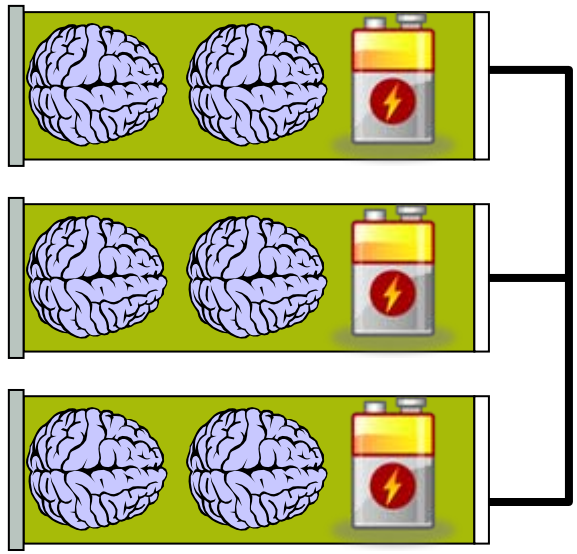
- Centralized Intelligence
  - Dumb line cards
  - All traffic processed on big blade
  - Redundancy implemented on blade

Architectures with existing processors



- Distributed
  - Intelligent line cards
  - Can implement local switching
  - May not need centralized resource
  - Redundancy on line card with two cores
  - Greater scalability

Improved architecture



Reduced power enables higher density

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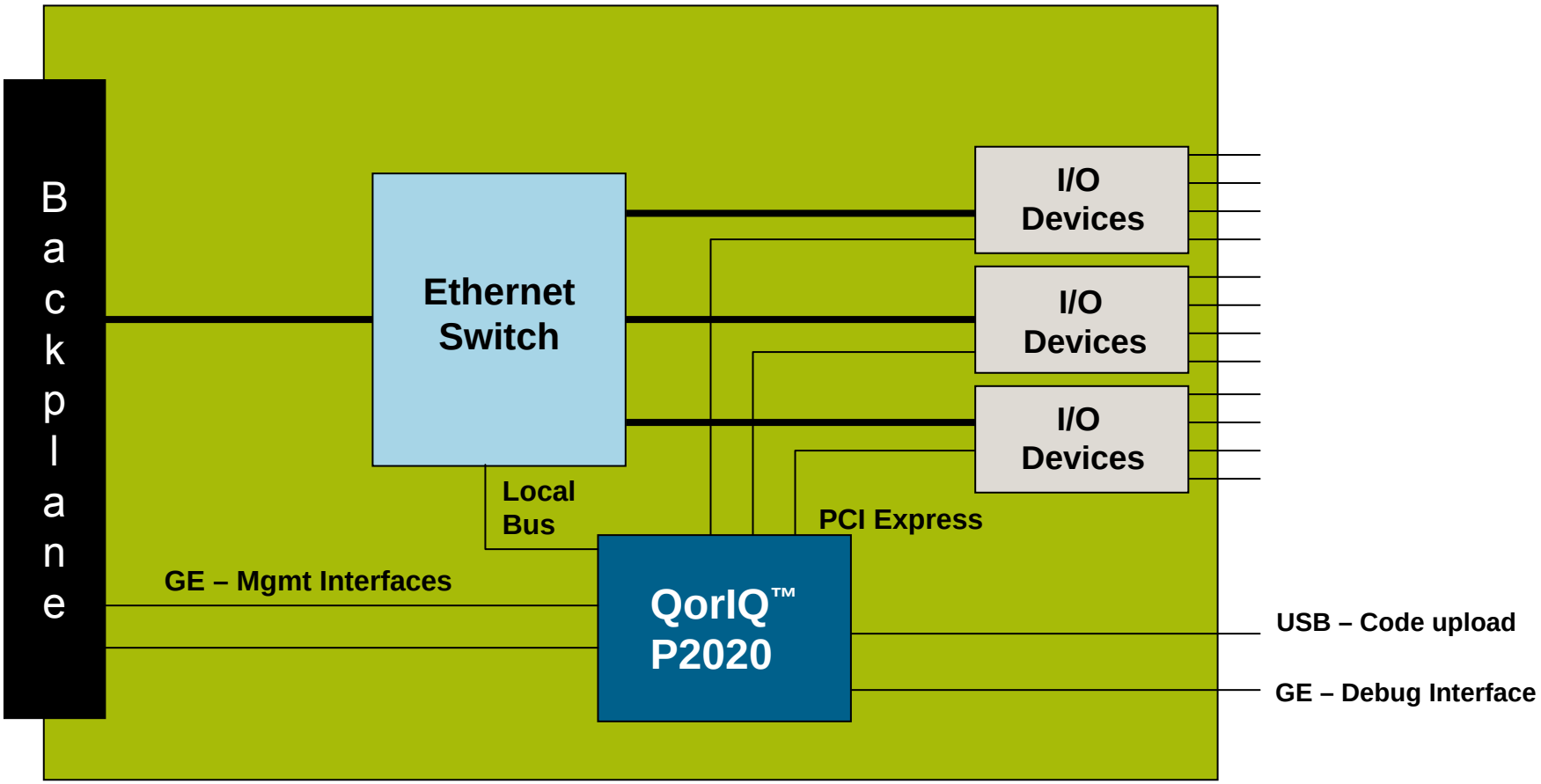
Linecard Control Plane



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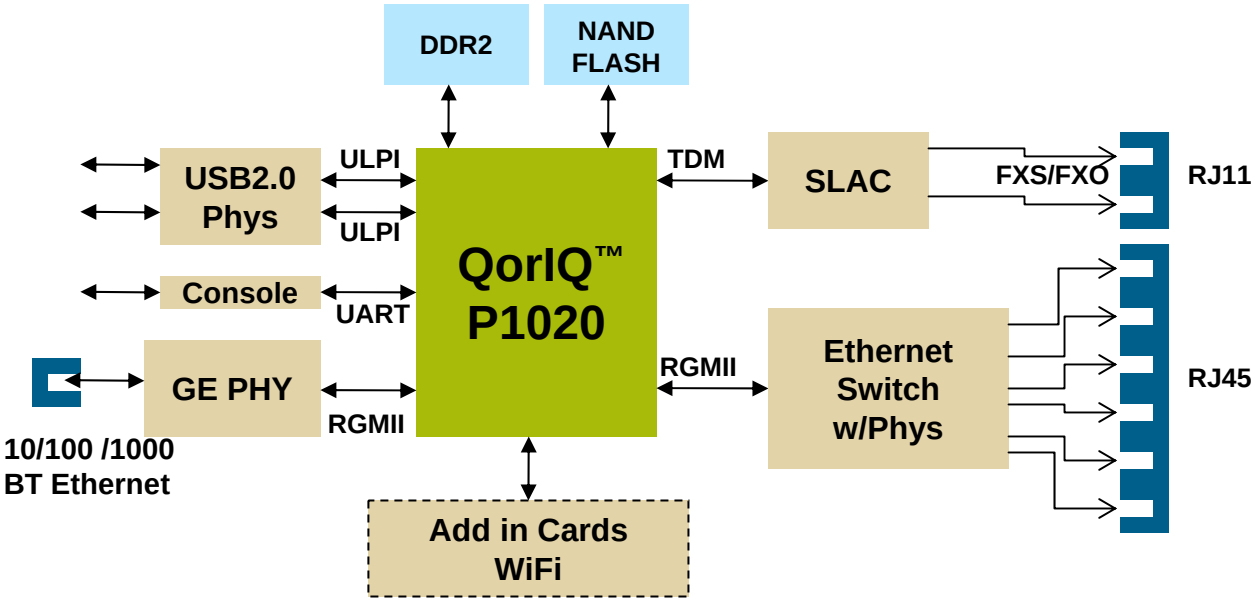
SMB / Branch Office Router



Features

- Dual-core AMP support
- 1-core for services/applications
- High-performance routing
- Security
  - NAPT/Firewall
  - Encrypted VPN
- Wireless 802.11N with option card
- VoIP through SIP Proxy and TDM
  - SIP phones
  - Analog phones
  - PSTN fail over (life line)

Challenges

- Scalability in performance and cost to support different number of users
- Low power
  - Simplify thermal design
  - Fanless design for higher reliability
- Flexibility to enable multiple product derivatives
  - Enhance 10/100/1000 Ethernet, USB, TDM, PCI-Exp, DDR2/3 support

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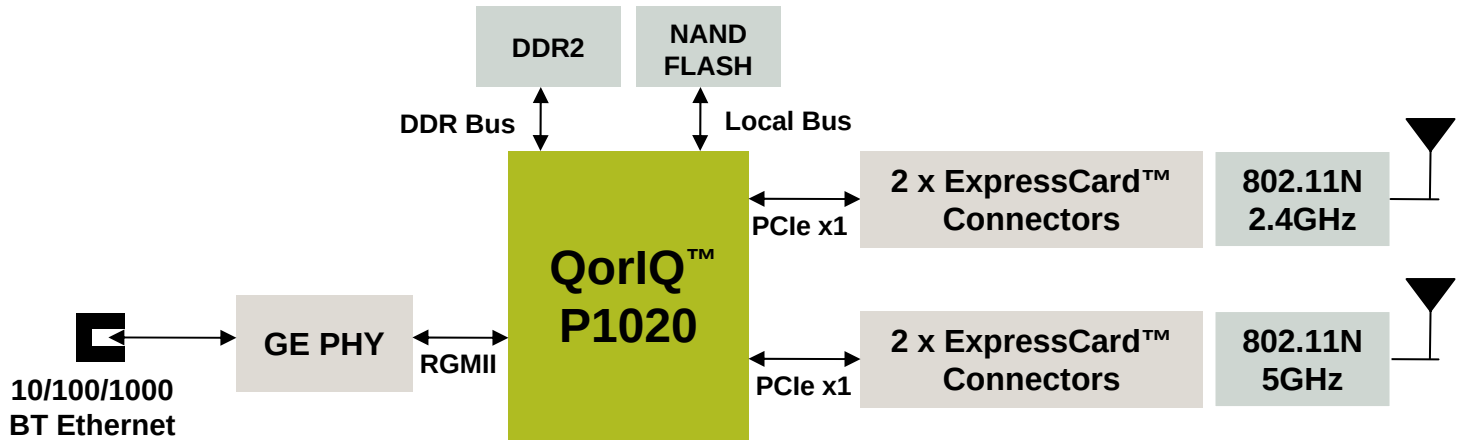
Enterprise WLAN Access Point



Challenges

- Power
  - IEEE802.3af Power over Ethernet standard limits
- Performance
  - IEEE802.11n
  - Trend towards increased throughput with more radios (4 x 4)
- Quality of Service
  - Support for VoIP over WiFi.

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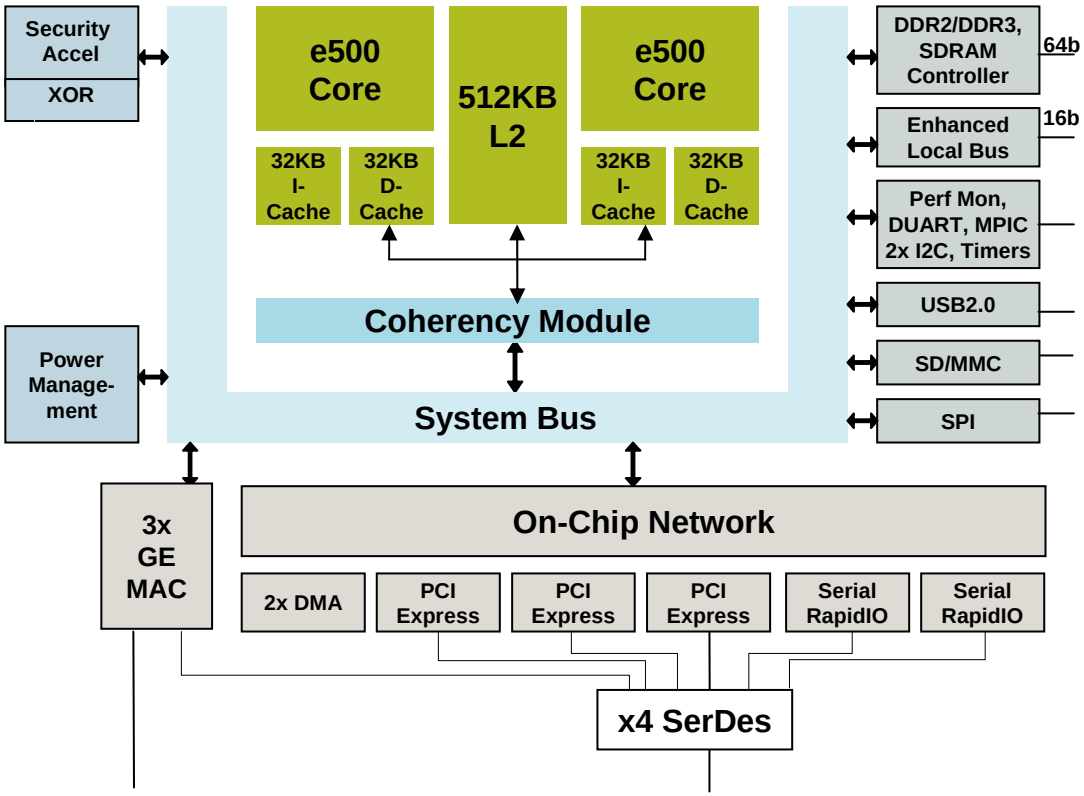
Dual-core P2020 Block Diagram



- **Dual e500 Power Architecture™ core**
  - 800 - 1200 MHz
  - 512KB Frontside L2 cache w/ECC, HW cache coherent
  - 36 bit physical addressing, DP-FPU
- **System Unit**
  - 64/32b DDR2/DDR3 with ECC
  - Integrated SEC 3.1 Security Engine
  - Open-PIC Interrupt Controller, Perf Mon, 2x I2C, Timers, 16 GPIO's, DUART
  - 16-bit Enhanced Local Bus supports booting from NAND Flash
  - One USB 2.0 Host Controller with ULPI interface
  - SPI controller supporting booting from SPI serial Flash
  - SD/MMC card controller supporting booting from Flash cards
  - Three 10/100/1000 Ethernet Controllers (eTSEC) w/ Jumbo Frame support, SGMII interface
    - Enhanced features: Parser/Filer, QOS, IP-Checksum Offload, Lossless Flow Control
    - IEEE 1588v2 support
  - Two Serial Rapid I/O Controllers with integrated message unit operating up to 3.125GHz
  - Three PCI Express 1.0a Controllers operating at 2.5GHz
- **Process & Package**
  - 45nm SOI, 0C to 125C Tj with -40C to 125C Tj option
  - 689-pin TePBGAII

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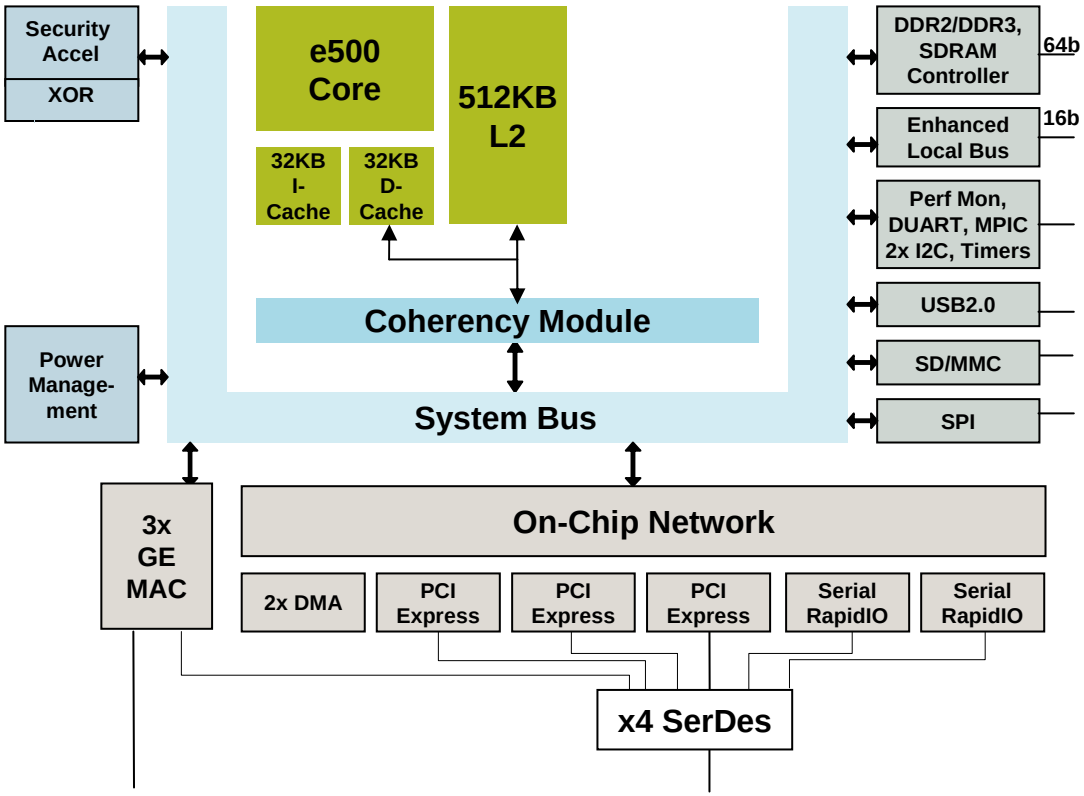
Single-Core P2010 Block Diagram



- **e500 Power Architecture™ core**
  - 800 – 1200 MHz
  - 512KB Frontside L2 cache w/ECC, HW cache coherent
  - 36 bit physical addressing, DP-FPU
- **System Unit**
  - 64/32b DDR2/DDR3 with ECC
  - Integrated SEC 3.1 Security Engine
  - Open-PIC Interrupt Controller, Perf Mon, 2x I2C, Timers, 16 GPIO's, DUART
  - 16-bit Enhanced Local Bus supports booting from NAND Flash
  - One USB 2.0 Host Controller with ULPI interface
  - SPI controller supporting booting from SPI serial Flash
  - SD/MMC card controller supporting booting from Flash cards
  - Three 10/100/1000 Ethernet Controllers (eTSEC) w/ Jumbo Frame support, SGMII interface
    - Enhanced features: Parser/Filer, QOS, IP-Checksum Offload, Lossless Flow Control
    - IEEE 1588v2 support
  - Two Serial Rapid I/O Controllers with integrated message unit operating up to 3.125GHz
  - Three PCI Express 1.0a Controllers operating at 2.5GHz
- **Process & Package**
  - 45nm SOI, 0C to 125C Tj with -40C to 125C Tj option
  - 689-pin TePBGAII

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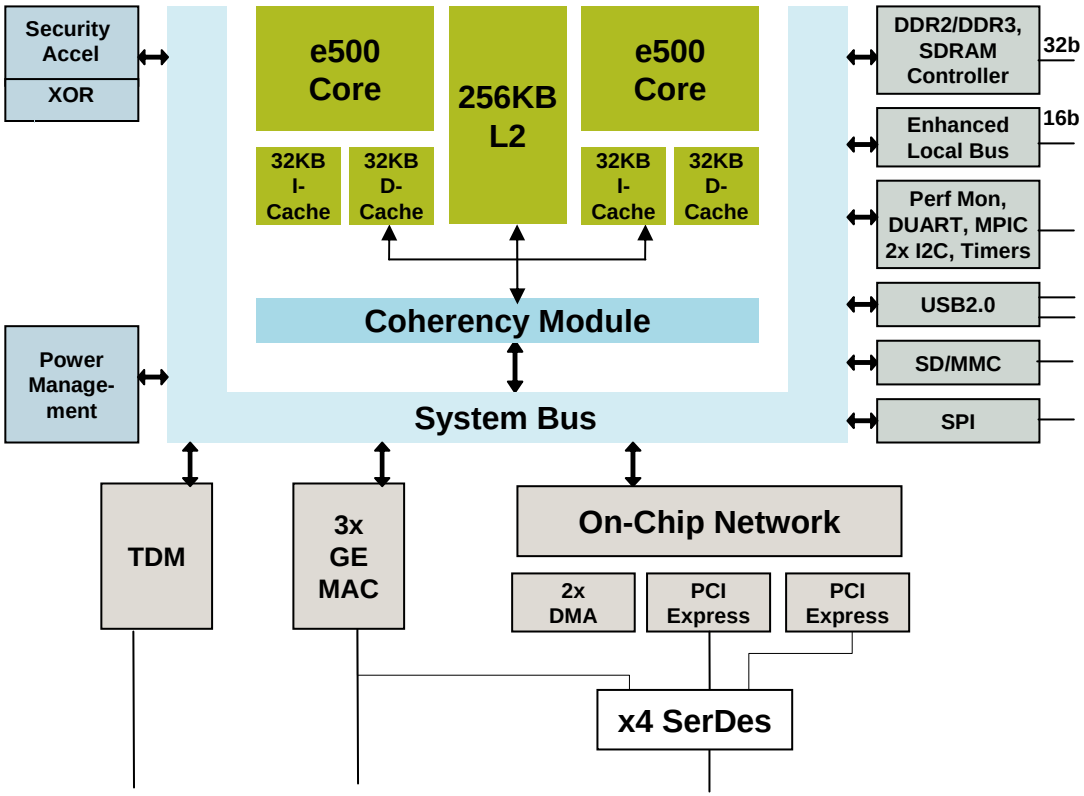
Dual-Core P1020 Block Diagram



- **Dual e500 Power Architecture™ core**
  - 533 – 800 MHz
  - 256KB Frontside L2 cache w/ECC, HW cache coherent
  - 36 bit physical addressing, DP-FPU
- **System Unit**
  - 32-bit DDR2/DDR3 with ECC
  - Integrated SEC 3.1 Security Engine
  - Open-PIC Interrupt Controller, Perf Mon, 2x I2C, Timers, 16 GPIO's, DUART
  - 16-bit Enhanced Local Bus supports booting from NAND Flash
  - Two USB 2.0Controllers Host/Device support
  - SPI controller supporting booting from SPI serial Flash
  - SD/MMC card controller supporting booting from Flash cards
  - TDM interface
  - Three 10/100/1000 Ethernet Controllers (eTSEC) w/ Jumbo Frame support, SGMII interface
    - Enhanced features: Parser/Filer, QOS, IP-Checksum Offload, Lossless Flow Control
    - IEEE1588v2 Support
  - Two PCI Express 1.0a Controllers operating at 2.5GHz
  - Power Management
- **Process & Package**
  - 45nm SOI, 0C to 125C Tj with -40C to 125C Tj option
  - 689-pin TePBGAII

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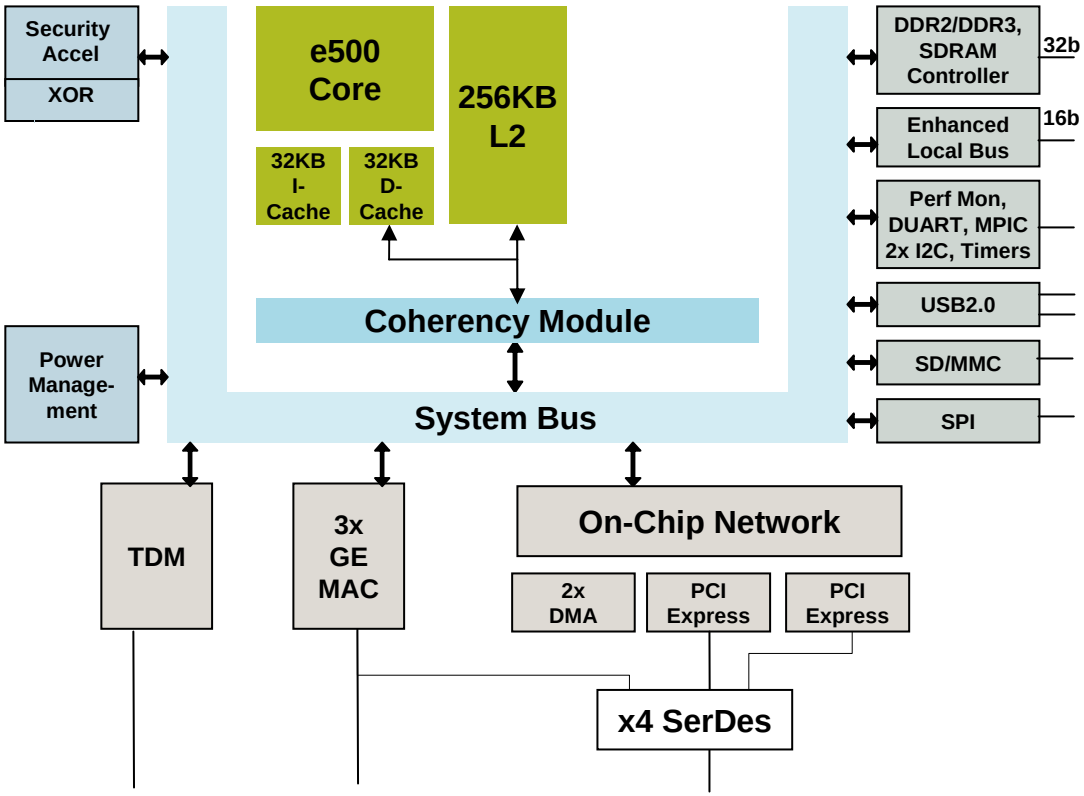
Single-Core P1011 Block Diagram



- **e500 Power Architecture™ core**
  - 533 – 800 MHz
  - 256KB Frontside L2 cache w/ECC, HW cache coherent
  - 36 bit physical addressing, DP-FPU
- **System Unit**
  - 32-bit DDR2/DDR3 with ECC
  - Integrated SEC 3.1 Security Engine
  - Open-PIC Interrupt Controller, Perf Mon, 2x I2C, Timers, 16 GPIO's, DUART
  - 16-bit Enhanced Local Bus supports booting from NAND Flash
  - Two USB 2.0 Controllers Host/Device support
  - SPI controller supporting booting from SPI serial Flash
  - SD/MMC card controller supporting booting from Flash cards
  - TDM Interface
  - Three 10/100/1000 Ethernet Controllers (eTSEC) w/ Jumbo Frame support, SGMII interface
    - Enhanced features: Parser/Filer, QOS, IP-Checksum Offload, Lossless Flow Control
    - IEEE1588v2 Support
  - Two PCI Express 1.0a Controllers operating at 2.5Gbps
  - Power Management
- **Process & Package**
  - 45nm SOI, 0C to 125C Tj with -40C to 125C Tj option
  - 689-pin TePBGAII

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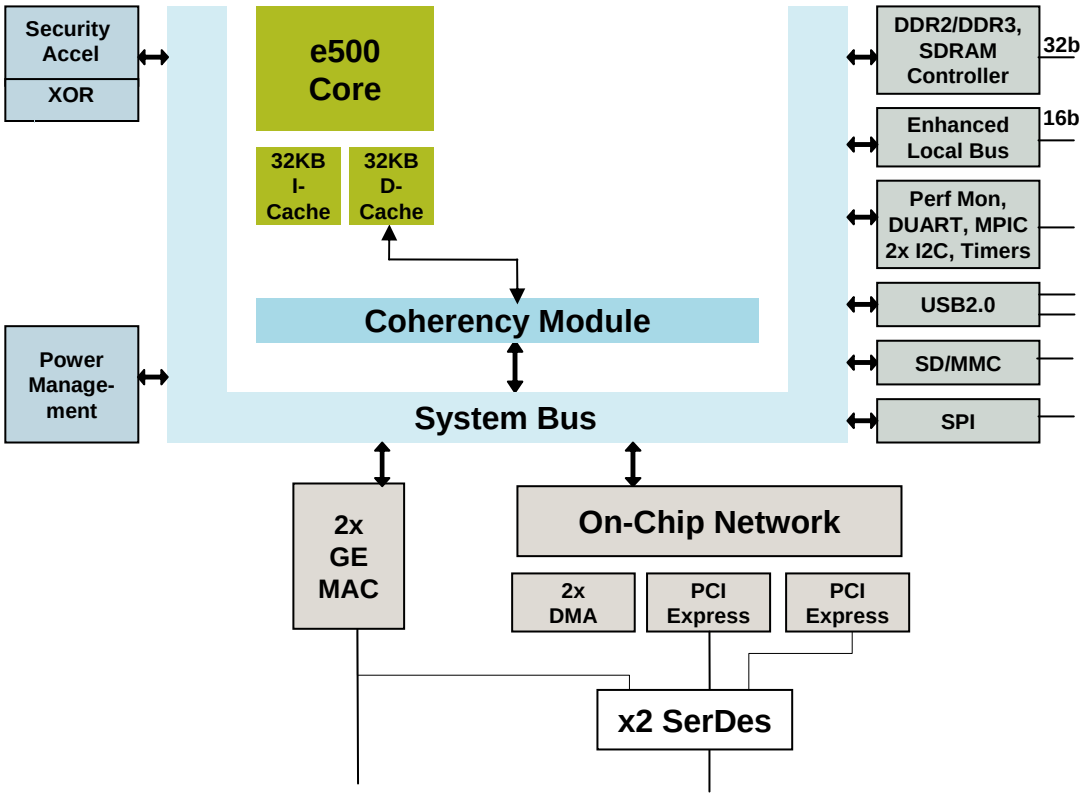
Single-Core P1010 Block Diagram



- **e500 Power Architecture™ core**
  - 400 – 667 MHz
  - 36 bit physical addressing, DP-FPU
- **System Unit**
  - 32-bit DDR2/DDR3 with ECC
  - Integrated SEC 3.1 Security Engine
  - Open-PIC Interrupt Controller, Perf Mon, 2x I2C, Timers, 16 GPIO's, DUART
  - 16-bit Enhanced Local Bus supports booting from NAND Flash
  - Two USB 2.0 Host Controllers
  - SPI controller supporting booting from SPI serial Flash
  - SD/MMC card controller supporting booting from Flash cards
  - Two 10/100/1000 Ethernet Controllers (eTSEC) w/ Jumbo Frame support, SGMII interface
    - Enhanced features: Parser/Filer, QOS, IP-Checksum Offload, Lossless Flow Control
    - IEEE1588v2 Support
  - Two PCI Express 1.0a Controllers operating up to 2.5GHz
  - Power Management
- **Process & Package**
  - 45nm SOI, 0C to 125C Tj with -40C to 125C Tj option
  - 689-pin TePBGAII

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QorIQ™ P1 and P2 Series Comparison

	P1010	P1011	P1020	P2010	P2020
CPU	e500 Up to **667MHz** 32K I/D	e500 Up to **800MHz** 32K I/D	Dual e500 Up to **800MHz** 32K I/D	e500 Up to **1200MHz** 32K I/D	Dual e500 Up to **1200MHz** 32K I/D
L2 Cache	-	**256KB**	**256KB**	**512KB**	**512KB**
DDR I/F Type/Width	DDR2/3 32-bit	DDR2/3 32-bit	DDR2/3 32-bit	DDR2/3 32/64-bit	DDR2/3 32/64-bit
10/100/1000 Ethernet (with IEEE1588v2)	2 with SGMII	3 w/(2) SGMII	3 w/(2) SGMII	3 w/(2) SGMII	3 w/(2) SGMII
TDM	-	Yes	Yes	-	-
PCI-Exp 1.0a	2 controllers w/ 2 SERDES	2 controllers w/ 4 SERDES	2 controllers w/ 4 SERDES	3 controllers w/ 4 SERDES	3 controllers w/ 4 SERDES
sRIO 1.2	-	-	-	2 x1 or 1 x4	2 x1 or 1 x4
USB2.0	2	2	2	1	1
Memory Card	SD/MMC	SD/MMC	SD/MMC	SD/MMC	SD/MMC
Other interfaces	SPI, 2xI2C, DUART	SPI, 2xI2C, DUART	SPI, 2xI2C, DUART	SPI, 2xI2C, DUART	SPI, 2xI2C, DUART
Accelerators	SEC3.1	SEC3.1	SEC3.1	SEC3.1	SEC3.1
Package	689 Te PBGAII	689 Te PBGAII	689 Te PBGAII	689 Te PBGAII	689 Te PBGAII

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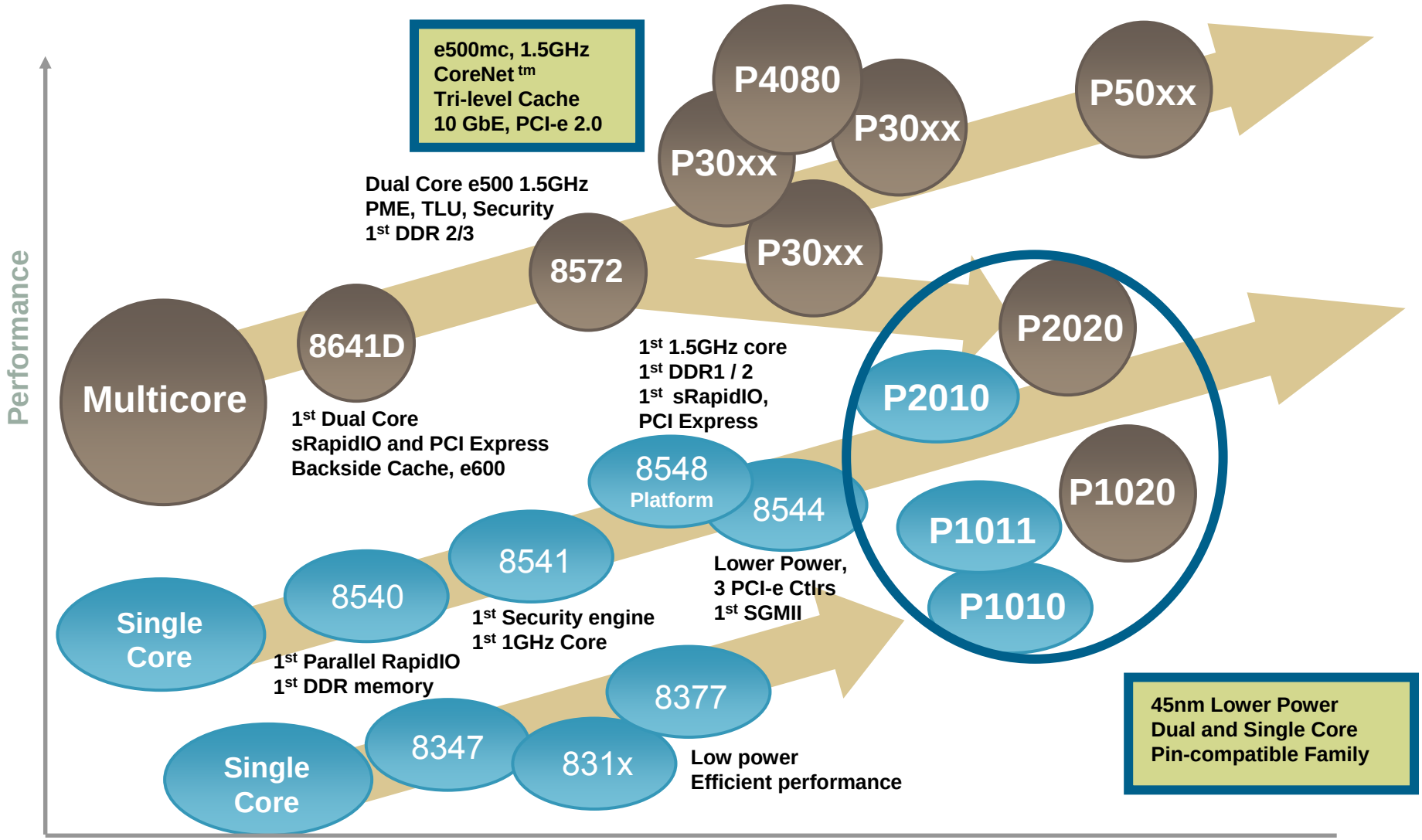
PowerQUICC Migration to QorIQ™ Platforms



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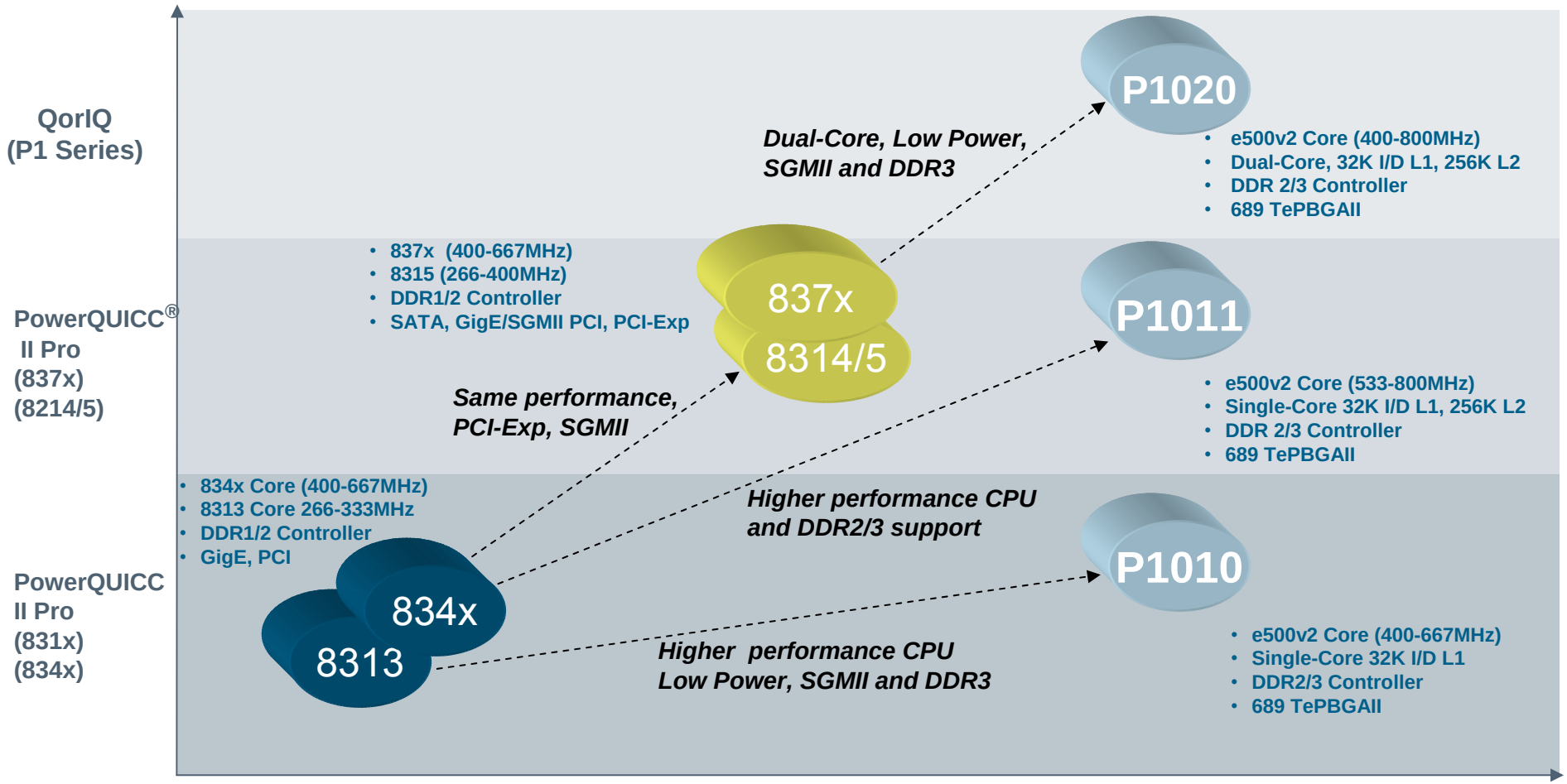
QorIQ™ P1 Migration Scenarios



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QorIQ™ P1 and PowerQUICC® II / PowerQUICC II Pro

	PowerQUICC I (MPC8xx)	PowerQUICC II (MPC82xx)	PowerQUICC II Pro (MPC83xx)	QorIQ (P1 Series)
CPU	50-133MHz	166-450MHz	266-667MHz	**400-800MHz**
DMIPS	66-175	318-864	505-1280	**920-3680**
Floating Point Support	All-handled in SW using exception mechanism	All	All (8323/21 FPU handled in SW using exception mechanism)	**Single precision embedded floating point. SPE**
Caches	Up to 16KB/8KB	16K/16K	Up to 32K/32K	**I/D 32K/32K L1, 256K L2**
Memory	SDRAM	SDRAM	DDR1/2	**DDR2/3**
Local Bus	No	Yes	Yes	**Yes (enhanced Local Bus)**
PCI Bus Options	-	PCI-All (Hip4 process)	PCI-All, PCI Express 8315/14, 837x	**PCI Express**
Security Engine	885, 875	8248, 8272	All E Versions	**All E Versions**
Communications Processor	All	All, except 8241/45/40	832x, 836x Only QE	**P1023 / P1013**
Ethernet	10/100 All (10 Mbps on 850/823/860)	10/100	10/100/1000 (10/100 on 832x)	**10/100/1000**
SATA	-	-	8315, 8379, 8377	**-**
ATM	88x/862/859/857/855/850	All except 8250/8248/8247/8270	8323/836x	
USB	885/880/875/870/850	8248/47, 827x	High Speed (except 832X, 836x)	**High Speed USB 2.0**
Packaging	256/357 PBGA	352/480 TBGA, 357/516 PBGA	516/620/668/689 PBGA, 672/740 TBGA	**689 TePBGAII**

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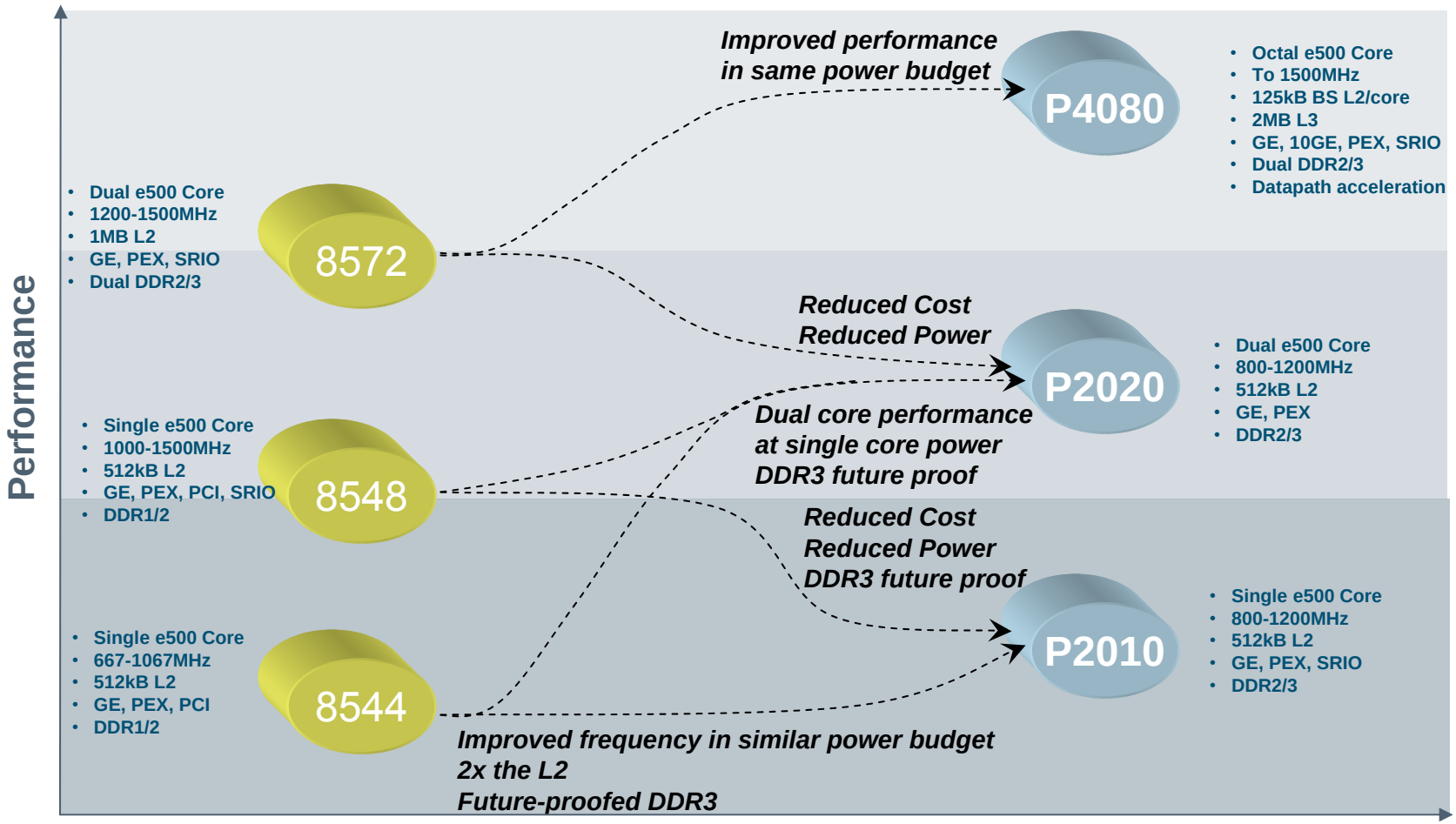
QorIQ™ P2 Migration Scenarios



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QorIQ™ P2 and PowerQUICC III

	MPC8544	P2010	MPC8548	P2020	MPC8572
CPU	e500 667 – 1067MHz 32K I/D	e500 800 - 1200MHz 32K I/D	e500 1000 - 1333MHz 32K I/D	Dual e500 800 to 1200MHz 32K I/D	Dual e500 1200 to 1500MHz 32K I/D
L2 Cache	256kB	512KB	512kB	512KB	1MB
DDR I/F Type/Width	DDR1/2, 64b	DDR2/3, 64-bit	DDR1/2, 64b	DDR2/3, 32/64-bit	Dual DDR2/3, 64b
10/100/1000 Ethernet	2 w/ all SGMII	3 w/ 2 SGMII	4	3 w/ 2 SGMII	4 w/ all SGMII + 10/100
PCI	32b PCI +3 PCIe controllers w/ 9 SerDes	3 PCIe controllers w/ 4 SerDes	64b PCI-X and PCIe w/ 8 SerDes	3 PCIe controllers w/ 4 SerDes	2 PCIe controllers w/ 8 SerDes
sRIO 1.2	-	2 x1 or 1 x4	1 x4	2 x1 or 1 x4	1 x4 or 1 x1
USB2.0	-	1	-	1	-
Local bus controller	32b	16b	32b	16b	32b
Memory Card	-	SD/MMC	-	SD/MMC	-
Other interfaces	DUART, 2xI2C	DUART, 2xI2C, SPI	DUART, 2xI2C	DUART, 2xI2C, SPI	DUART, 2xI2C
Accelerators	SEC2.1	SEC3.1	SEC 3.0	SEC3.1	SEC 3.0, PME, TLU
Package	783 FC-PBGA	689 Te PBGAII	783 FC-CBGA and FC-PBGA	689 Te PBGAII	1023 FC-PBGA

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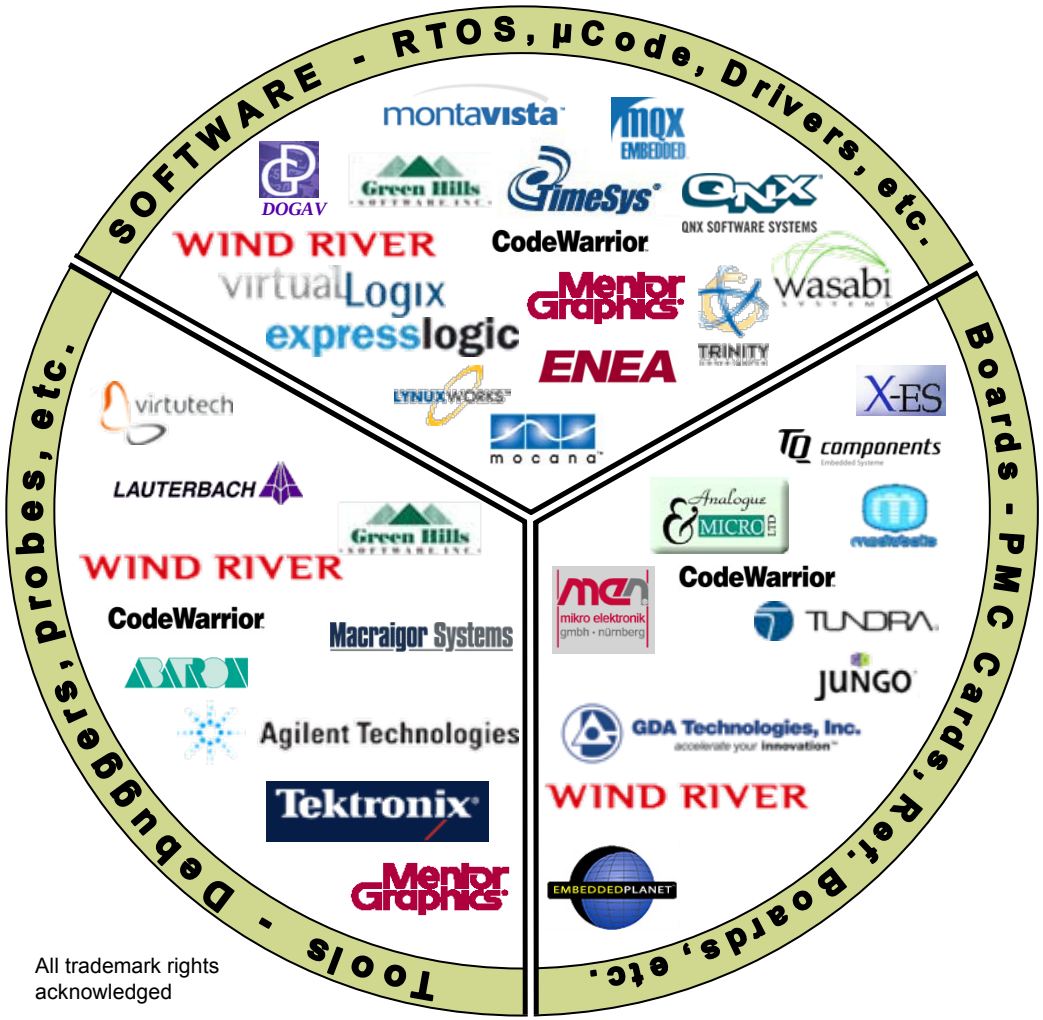
Leading Embedded Ecosystem



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- **Pre-silicon**
  - Functional simulation
  - I/O simulation
  - Power simulation
- **Software**
  - Operating systems
  - Application stacks
  - Protocol acceleration
  - Development services
- **Board offerings**
  - Custom off the shelf
  - Standard product
  - Various form factors
  - Integration design services
- **Development**
  - Integrated development environments
  - Debuggers
  - Compilers
  - Probes

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QorIQ™ P1 and P2 Series Summary

Features	Benefits
Best in class ecosystem	Faster time to market
Migration path	Improved performance/watt/$ migrating from PowerQUICC II, PowerQUICC II Pro, and PowerQUICC III
High performance e500 2.4MIPS/MHz Power Architecture™ core	High efficiency and frequency cores means fewer cores to get the job done
Best-in-class power	Enables fanless, “green” and low cost designs, improves reliability
Integrated Ethernet, TDM, USB, SD Flash controller, IEEE1588, PCI-Express, Serial Rapid IO	Flexibility to address a wide range of applications and reduced system cost
6x performance range in a single package	Common hardware platform to enable wide range of system performance
Dual and single cores	Move to dual core at your own pace without hardware changes

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Related Session Resources

Session Location – Online Literature Library

http://www.freescale.com/webapp/sps/site/homepage.jsp?nodeId=052577903644CB

Sessions

Session ID	Title

Demos

Pedestal ID	Demo Title

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