Freescale Technology Forum

Design Innovation.

November 2008

Hands-on Workshop: An Introduction to Freescale Segment LCD Solutions

PZ114

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Basis on Liquid Crystal Display Technologies

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Segment LCD Products Everywhere

Watch

Clock

Calculator

Disk

Appliances

Remote Controller

Thermal Stat

Portable One Time Token

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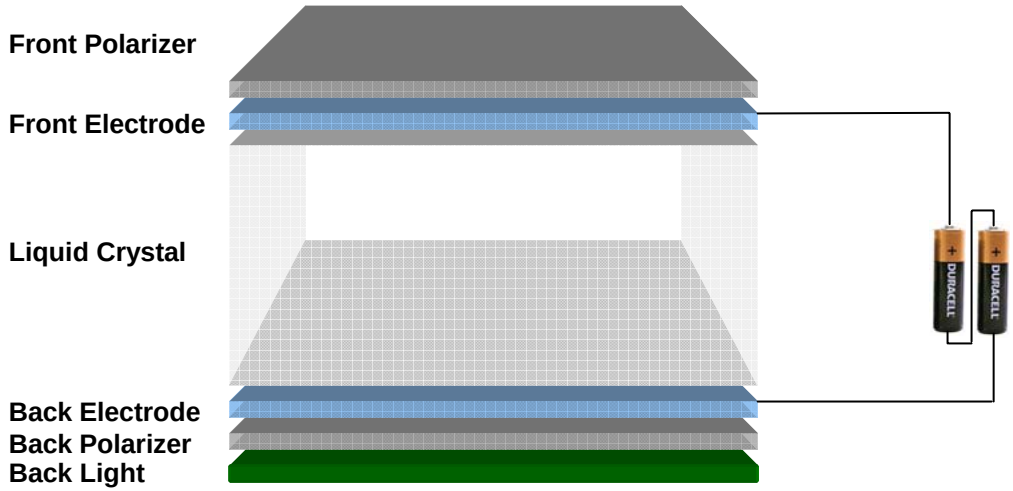
Basics of LCD Operation

- The twisted nematic (TN) – The most common LCD
  - Sandwich Construction
    - Front Polarizer
    - Front Electrode
    - Liquid Crystal
    - Back Electrode
    - Back Polarizer
    - Back Light



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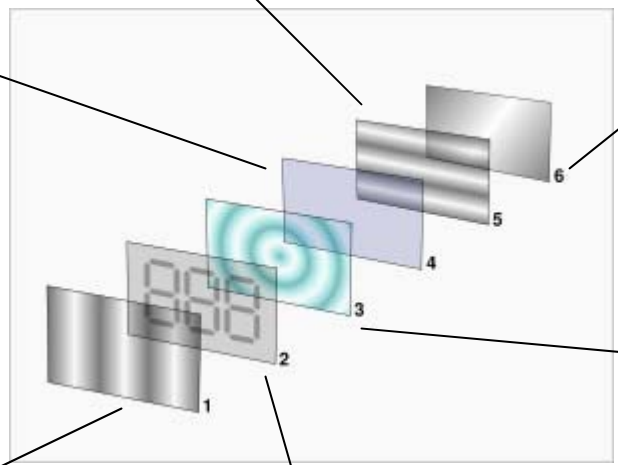
Reflective twisted nematic LCD

Glass substrate with common electrode film (ITO) with horizontal ridges to line up with the horizontal filter

Polarizing filter film with a horizontal axis to block/pass light

Reflective surface to send light back to viewer. (In a backlit LCD, this layer is replaced with a light source.)



Twisted nematic liquid crystal

Polarizing filter film with a vertical axis to polarize light as it enters

Polarizing filter film with a vertical axis to polarize light as it enters Glass substrate with ITO electrodes. The shapes of these electrodes will determine the shapes that will appear when the LCD is turned ON. Vertical ridges etched on the surface are smooth

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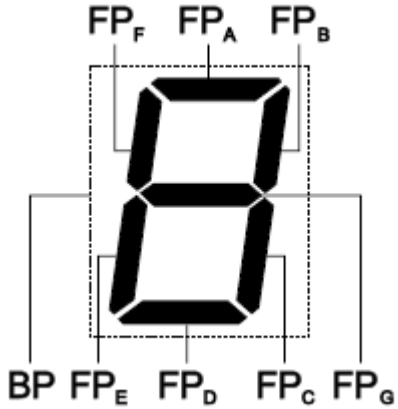
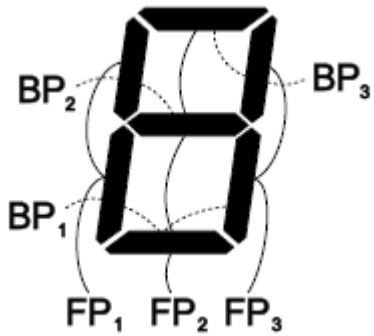
Display Segments

- Static Display
  - One backplane electrode for all segments
  - One front plane electrode for each segment
- Dynamic Display
  - Matrix organization
    - Multi back plane time-division shared by all front plane
    - Multi front plane time-division shared by all back plane
- Dynamic VS Static
  - Dynamic display needs less driving terminals
  - Static has better optical properties



A typical 7-segment static display



A typical 3 front plane and 3 back plane dynamic display

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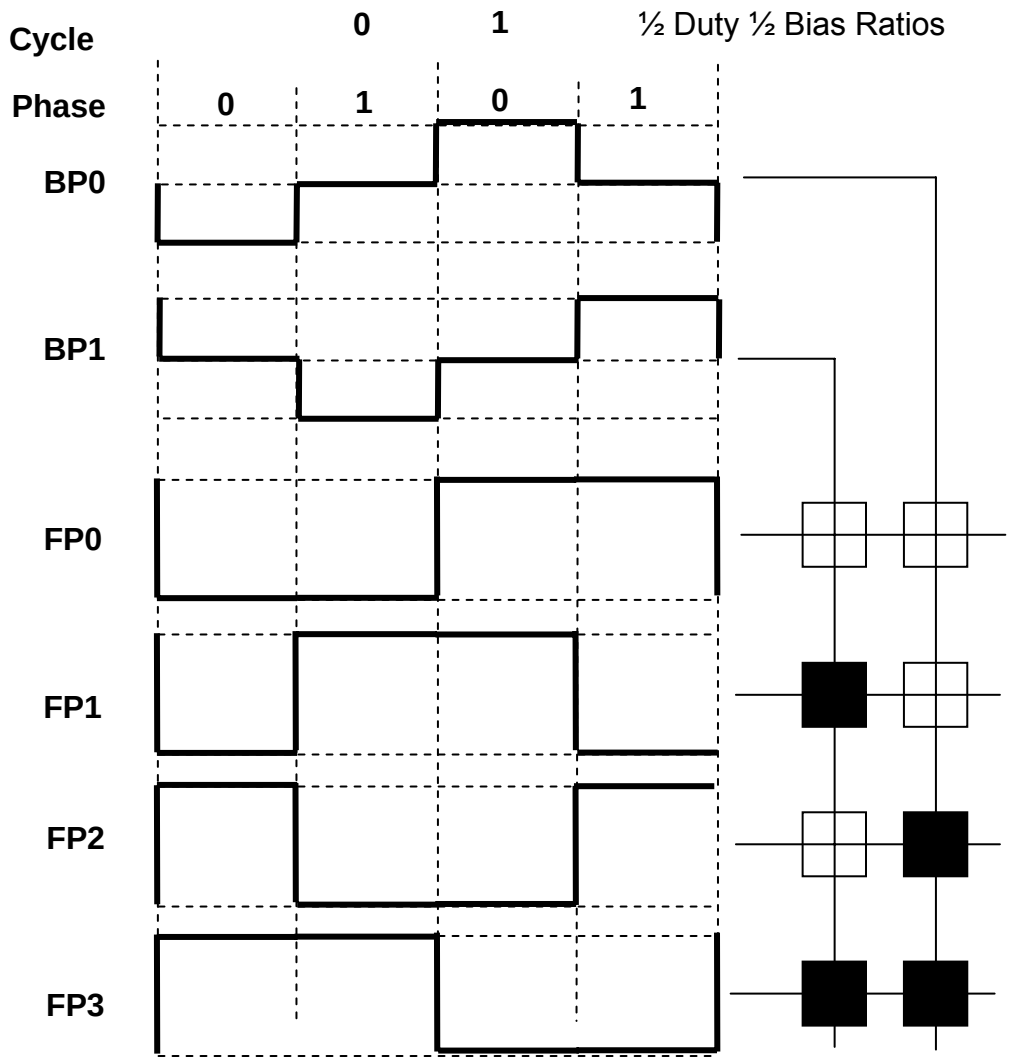
Dynamic Segment Display

- Duty – Time Component
  - the number of phases of the refresh cycle
  - Mostly, duty cycle equal to back plane number
  - Most used duty cycle 4x mode
- Bias – Voltage Component
  - The voltage across the LCD cell during the inactive phases
  - Most used bias 1/3 mode



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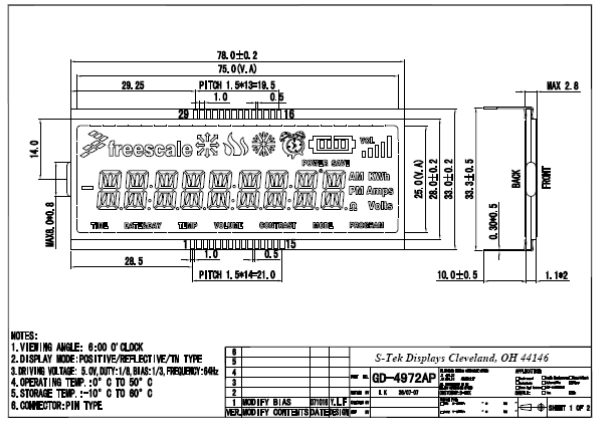
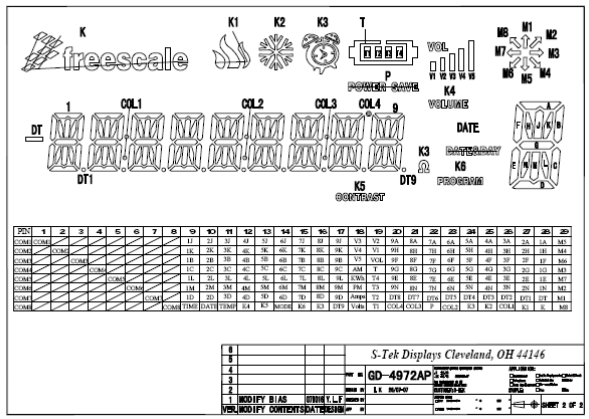
Order LCD Glass

- Dimension
- Segment Definition
  - Front plane mapping
  - Back plane mapping
- Parameters
  - Viewing Angle:
    - 12:00, 3:00, 6:00, 9:00 O'Clock
  - Display Mode
    - TN, STN, ...
    - POSITIVE/NEGATIVE
    - REFELECT/TRANSMISSIVE/
  - Operating Voltage
    - 3V, 5V, ...
  - Duty cycle and Bias
  - Operating Frequency
- Others
  - Operating/Storage Temperature
  - Connector





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Freescale Segment LCD MCU Family

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Freescale Segment LCD MCU Family

- MC9S08LL16 – Low-voltage ultra-low-power LCD Microcontroller
  - Operating Voltage 1.8V – 3.6V
  - Enabled by Flexis Technologies
  - Up to 8×24 or 4×28 LCD segments
- MC9RS08LA8 – Cost-effective Low-power LCD Microcontroller
  - Operating Voltage 2.7V – 5.5V
  - Enabled by RS08 CPU core
  - Up to 8×21 or 4×25 LCD segments
- MC9RS08LE4 – Lowest-end Low-power LCD Microcontroller
  - Operating Voltage 2.7V – 5.5V
  - Enabled by RS08 CPU core
  - Up to 8×14 or 4×18 LCD segments
  - Packaged in 28-pin SOIC

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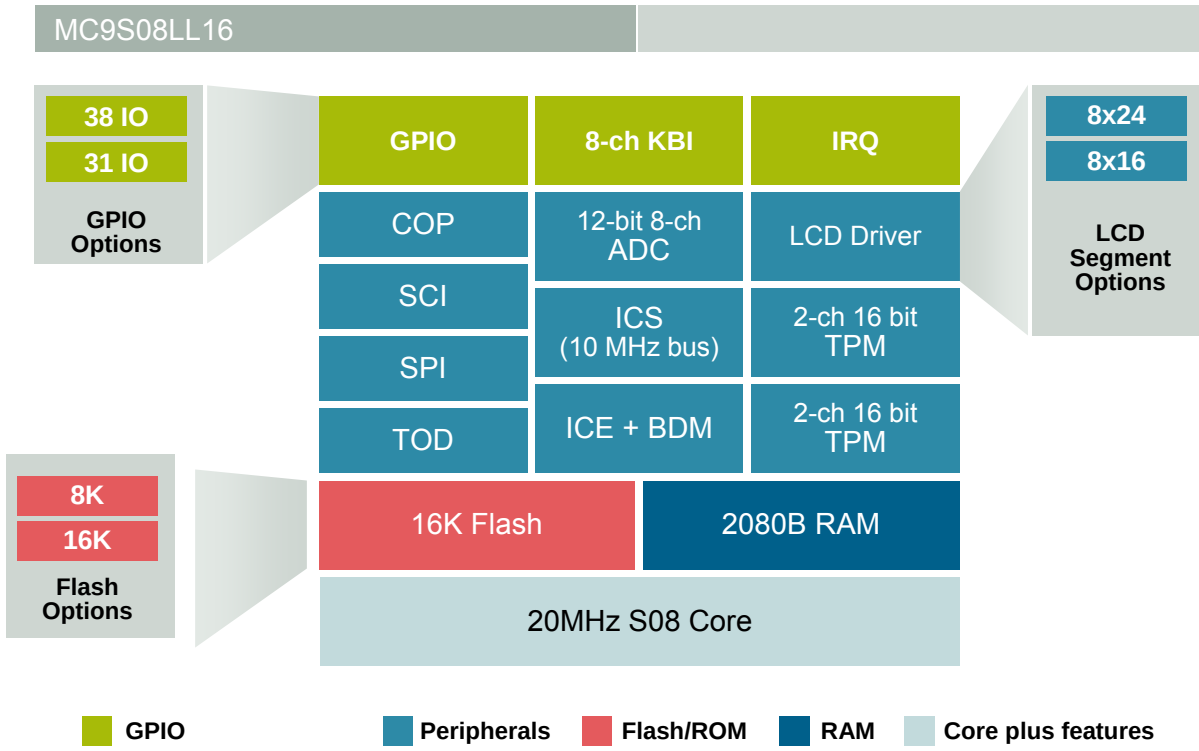
MC9S08LL16 Features

- Voltage Range
  - 1.8V ~ 3.6V
- Core & BUS
  - 20MHz S08 Core
  - 10MHz BUS
- LCD Driver
  - 8x24 in 64-pin
  - 8x14 in 48-pin
- Peripherals
  - 2x 2-ch 16-bit TPM
  - 1x TOD
  - 1x 12-bit 8-ch ADC
  - Communications
    - SCI
    - SPI
    - IIC
- Package
  - 64-pin LQFP
  - 48-pin QFN & LQFP



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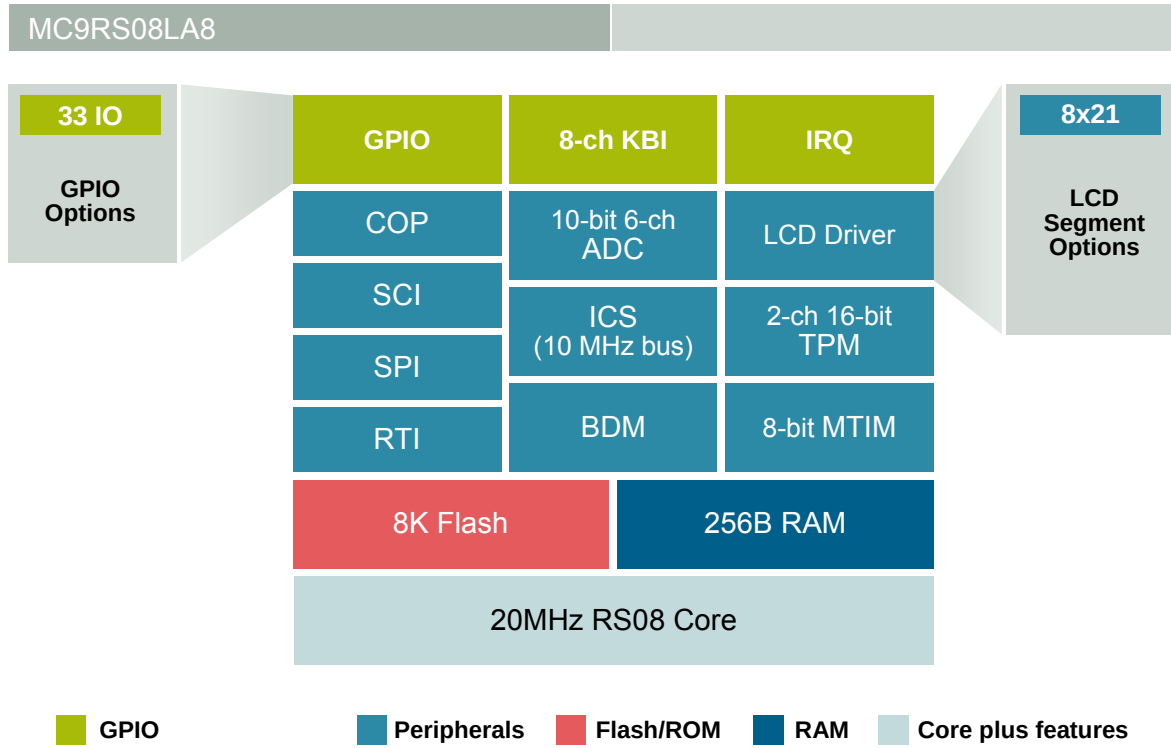
MC9RS08LA8 Features

- Voltage Range
  - 2.7V ~ 5.5V
- Core & BUS
  - 20MHz RS08 Core
  - 10MHz BUS
- LCD Driver
  - 8 x 21
- Peripherals
  - 1 x 2-ch 16-bit TPM
  - 1 x 8-bit MTIM
  - 1 x RTI
  - 1 x 10-bit 6-ch ADC
  - Communications
    - SCI
    - SPI
    - IIC
- Package
  - 48-pin QFN & LQFP



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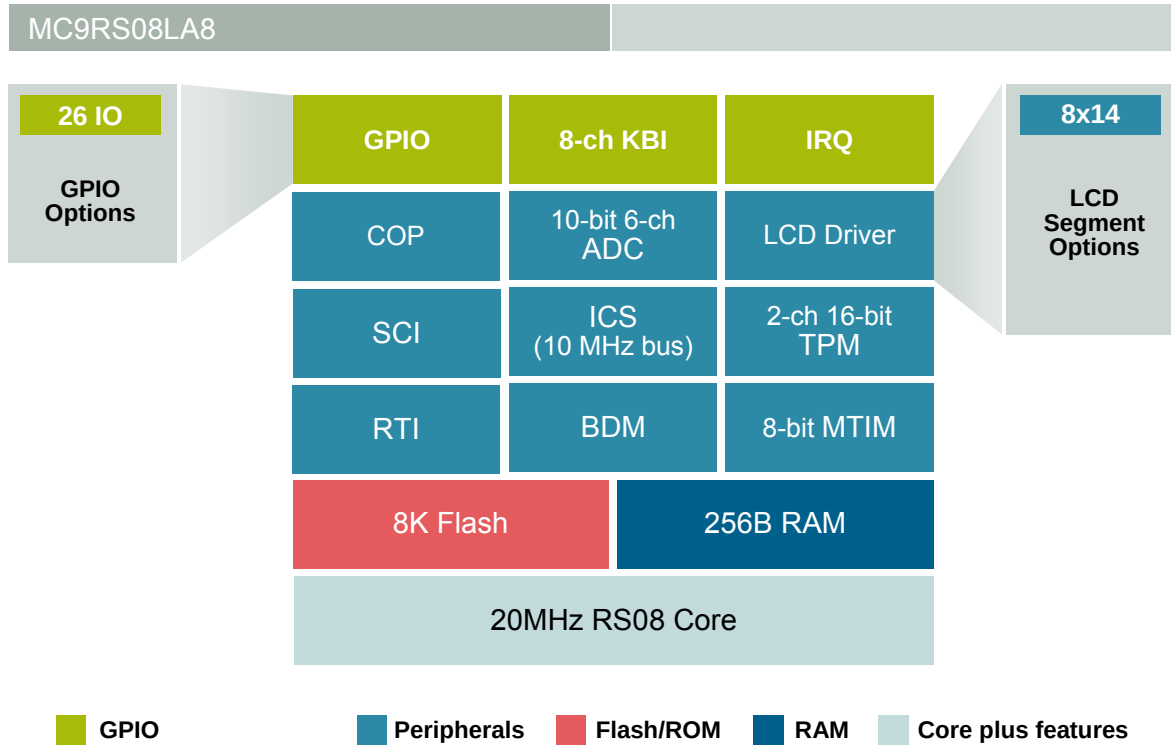
MC9RS08LE4 Features

- Voltage Range
  - 2.7V ~ 5.5V
- Core & BUS
  - 20MHz RS08 Core
  - 10MHz BUS
- LCD Driver
  - 8 x 14
- Peripherals
  - 2 x 2-ch 16-bit TPM
  - 1 x RTI
  - 1 x 10-bit 8-ch ADC
  - Communications
    - SCI
- Package
  - 28-pin SOIC



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Freescale LCD MCU Family

		MC9S08LL16	MC9RS08LA8	MC9RS08LE4
Operating Voltage		1.8V – 3.6V	2.7V – 5.5V	2.7V – 5.5V
CPU		S08@20MHz	RS08@20MHz	RS08@20MHz
BUS		10MHz	10MHz	10MHz
Memory on-chip	*FLASH*	16KB	8KB	4KB
	RAM	2080B	256B	256B
Timers		2 × 2-ch 16-bit TPM	1 × 2-ch 16-bit TPM 1 × 8-bit MTIM	2 × 2-ch 16-bit TPM
Real-Time Clock		TOD	RTI	RTI
Comms.	*SCI*	YES	YES	YES
	SPI	YES	N/A	N/A
	IIC	YES	N/A	N/A
ADC		8-ch 12-bit	6-ch 10-bit	8-ch 10-bit
ACMP		YES	YES	N/A
LCD Driver	*Segments*	8 × 24 = 192 4 × 28 = 112	8 × 21 = 168 4 × 25 = 100	8 × 14 = 112 4 × 18 = 72
	Charge Pump	YES	YES	NO
	Resister Network	YES	YES	YES
	VLCD pin	YES	NO	NO
	VCAP1 VCAP2 Vll1 VLL2Vll3	YES	YES	NO
GPIO		38	33	26
Packages		64-pin 48-pin	48-pin	28-pin

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Introduction to Freescale LCD Driver

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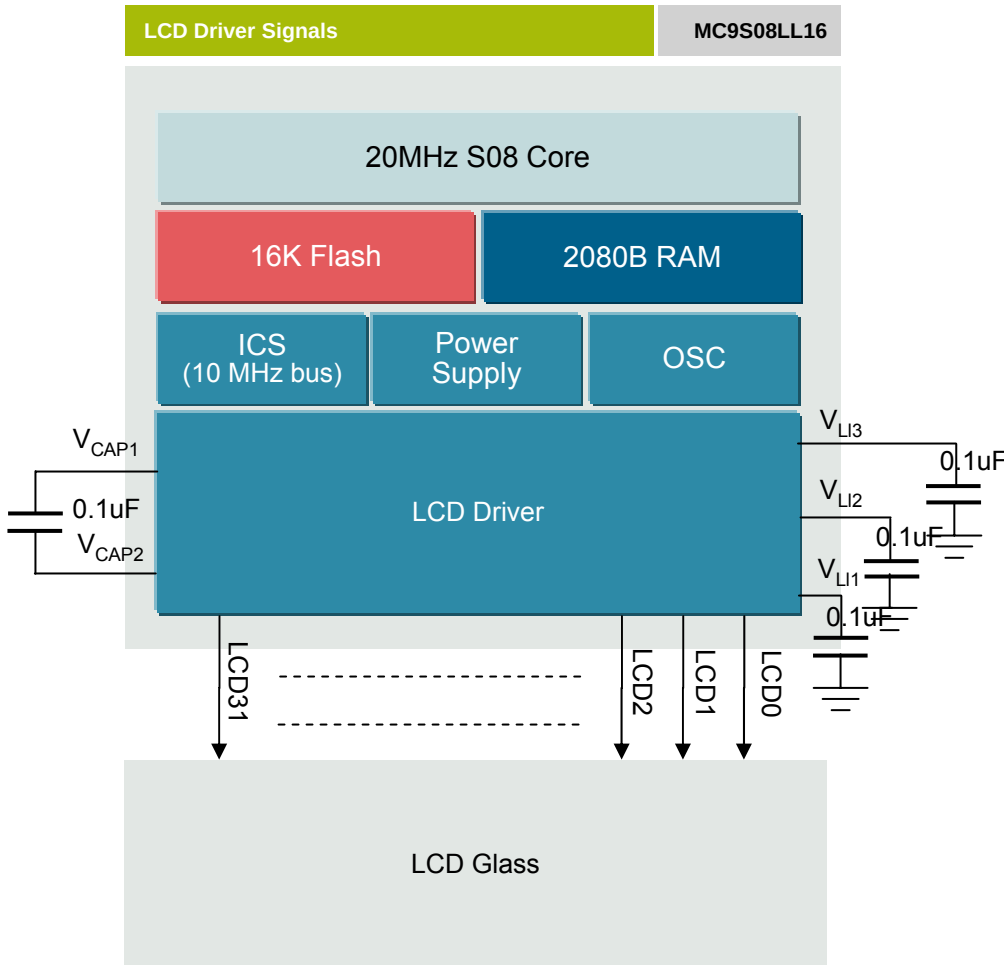
LCD Driver Signals

- LCD FP/BP Pins
  - LCD driver pins
  - All pins can operate as FP or BP
  - Up to 8 Back plane driver pins
- V_{LCD} Pins
  - LCD supply voltage
  - Available on LL16 only
- LCD Bias Pins
  - V_{LL3} = Full LCD driving voltage
  - V_{LL2} = 2/3 LCD driving voltage
  - V_{LL1} = 1/3 LCD driving voltage
  - Available on LL16 and LA8 only
- LCD Charge Pump Pins
  - V_{CAP1} and V_{CAP2}
  - Available on LL16 and LA8 only



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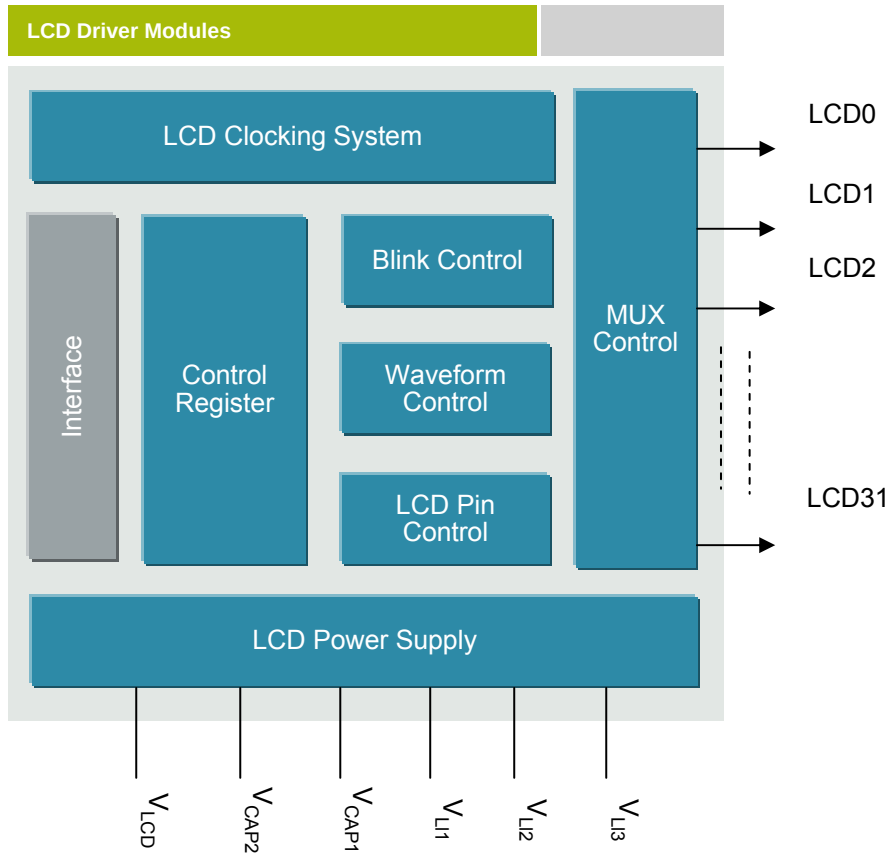
LCD Driver Architecture

- LCD Clocking Control
  - Providing Clock reference to generate LCD waveform and light charge pump
- LCD Power Control
  - Providing Power Supply to LCD waveform
- LCD Pin Control
  - Enable / Disable LCD Pins
  - Enable / Disable LCD Backplane Pins
- Waveform Control
  - Generate LCD waveforms on each LCD driver pin
- Blink Control
  - Control LCD Blink mode and frequency
- MUX Control
  - Mapping LCD waveforms on LCD pins
- Control Registers and Interface
  - Interfacing CPU and contains all configuration information



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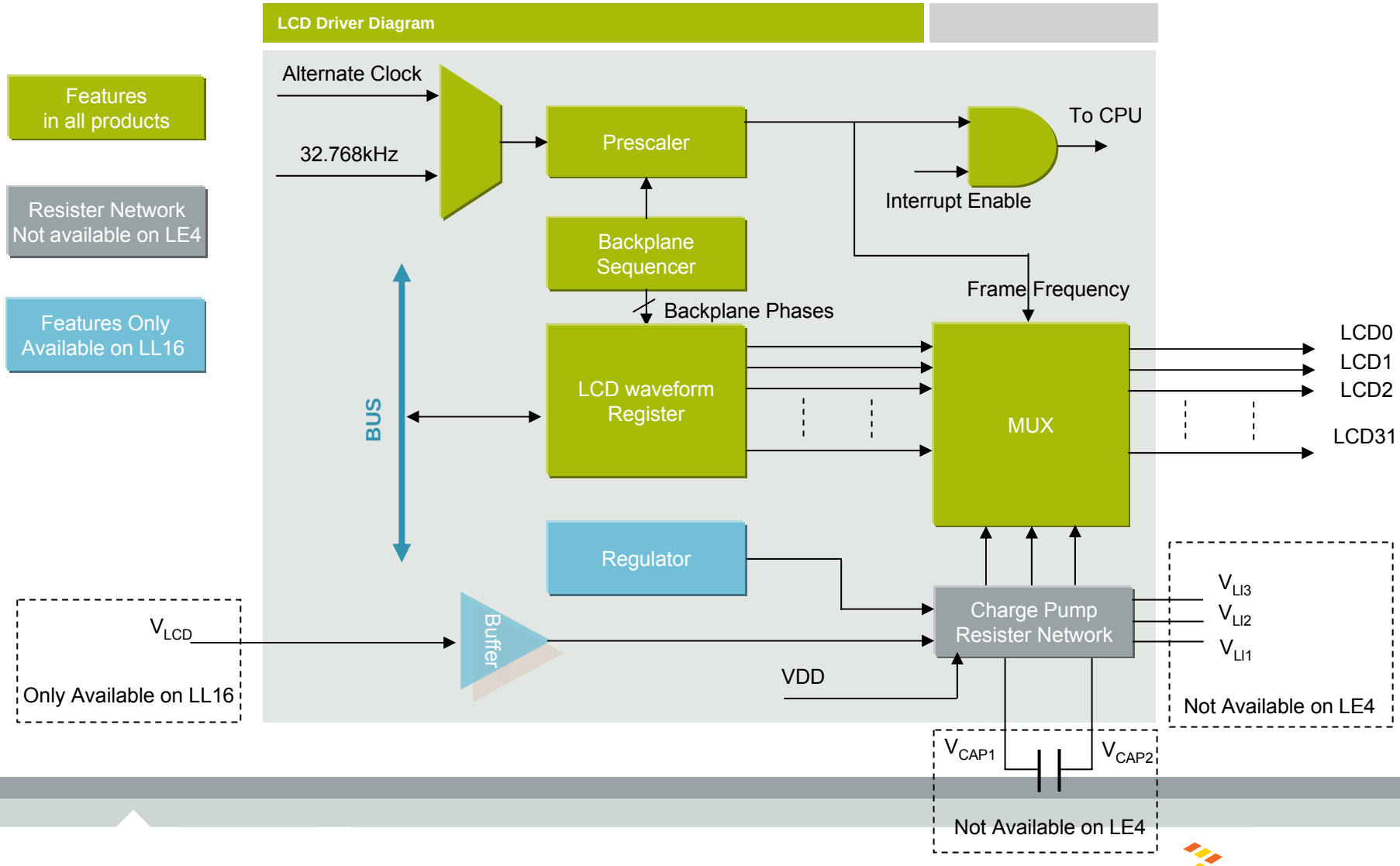
LCD Driver Diagram



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LCD Driver Register Definition

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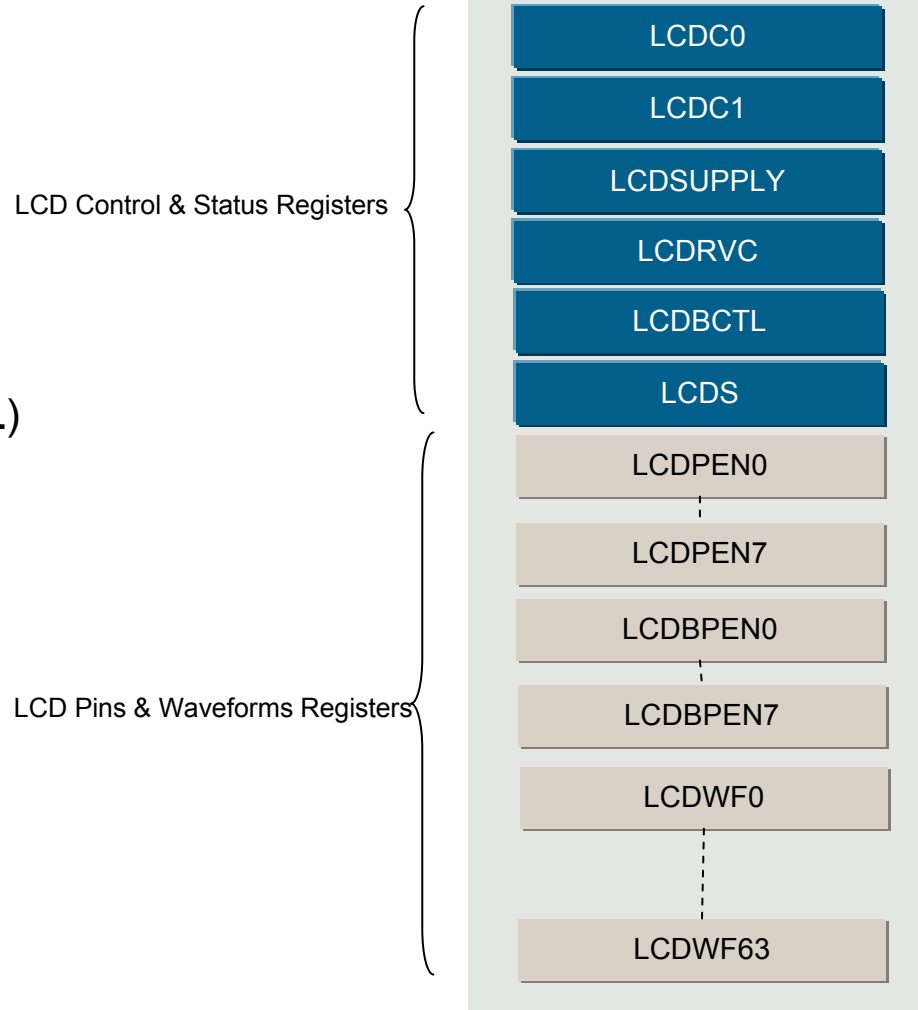
LCD Control Registers

- LCD Control & Status Registers
  - LCD Control Register 0 (**LCDC0**)
  - LCD Control Register 1 (**LCDC1**)
  - LCD Voltage Supply Register (**LCD SUPPLY**)
  - LCD Regulated Voltage Control Register (**LCDRVC**)
  - LCD Blink Control Register (**LCDBCTL**)
  - LCD Status Register (**LCDS**)
- LCD Pins & Waveforms Registers
  - LCD Pin Enable Registers (**LCDPEN0 – LCDPEN7**)
  - LCD Backplane Pin Enable Registers (**LCDBPEN0 – LCDBPEN7**)
  - LCD Waveform Registers (**LCDWF0 – LCDWF63**)



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LCD Control & Status Registers

	Name		7	6	5	4	3	2	1	0
LCD Control Register 0	LCDC0	R	LCDEN	SOURCE	LCLK2	LCLK1	LCLK0	DUTY2	DUTY1	DUTY0
		W								
LCD Control Register 1	LCDC1	R	LCDIEN	0	0	0	0	FCDEN	LCDWAI	LCDSTP
		W								
LCD Voltage Supply Register	LCDCSUPPLY	R	CPSEL	HREFSEL	LADJ1	LADJ0	0	BBYPASS	VSUPPLY1	VSUPPLY0
		W								
LCD Regulated Voltage Control Register	LCDRVC	R	RVEN	0	0	0	RVTRIM3	RVTRIM2	RVTRIM1	RVTRIM0
		W								
LCD Blink Control Register	LCDBCTL	R	BLINK	ALT	BLANK		BMODE	BRATE2	BRATE1	BRATE0
		W								
LCD Status Register	LCDS	R	LCDIF	0	0	0	0	0	0	0
		W								

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LCD Control Register 0 (LCDC0)

LCD Control Register 0 (LCDC0)

	7	6	5	4	3	2	1	0
R W	LCDEN	SOURCE	LCLK2	LCLK1	LCLK0	DUTY2	DUTY1	DUTY0
Reset	0	0	0	0	0	0	1	1

7 LCDEN **LCD Driver Enable** — LCDEN starts LCD-module-waveform generator.

6 SOURCE **LCD Clock Source Select** — To select clock source as the basis for LCD clock

5:3 LCLK **LCD Prescaler** — To use a clock divider to generate LCD waveform frame frequency. Detail

2:9 DUTY **LCD Duty Select** — To select the duty cycle of LCD module

LCD Control Register 1 (LCDC1)

LCD Control Register 1 (LCDC1)

	7	6	5	4	3	2	1	0
R W	LCDIEN					FCDEN	LCDWAI	LCDSTP
Reset	0	0	0	0	0	1	0	0

7 LCDIEN **LCD Module Frame Frequency Driver Enable** — Enables an LCD interrupt event that coincides with the LCD module frame frequency.

2 FCDEN **Full Complementary Drive Enable** — To allow GPIO that are shared with LCD pins to operate as full complementary if the other conditions necessary have been met

1 LCDWAI **LCD Module Driver and Charge Pump in Wait Mode** — To allow the LCD driver and charge pump to continue running during wait mode

0 LCDSTP **LCD Module Driver and Charge Pump in Stop Mode** — To allow the LCD driver and charge pump to continue running during stop mode

LCD Voltage Supply Register (LCDSUPPLY)

LCD Voltage Supply Register (LCDSUPPLY)

	7	6	5	4	3	2	1	0
R W	CPSEL	HREFSEL	LADJ1	LADJ0		BBYPASS	VSUPPLY1	VSUPPLY0
Reset	0	0	0	0	0	1	0	0

7 SPSEL **Charge Pump or Resistor Bias Select** —To select LCD module charge pump or a resistor network to supply the LCD voltages V_{LL1}, V_{LL2}, and V_{LL3}.

6 HREFSEL **High Reference Select** — To select reference bias divider

5:4 LADJ **LCD Module Load Adjust** — To configure the LCD module to handle different LCD glass capacitance

2 BBYPASS **Op Amp Control** — To determine whether the internal LCD op amp buffer is bypassed

1:0 VSUPPLY **Voltage Supply Control** — To configure LCD module power supply

LCD Regulated Voltage Control Register (LCDRVC)

LCD Regulated Voltage Control Register (LCDRVC)

	7	6	5	4	3	2	1	0
R W	RVEN				RVTRIM3	RVTRIM2	RVTRIM1	RVTRIM0
Reset	0	0	0	0	0	0	0	0

7 RVEN **Regulated Voltage Enable** —To enable internal voltage regulator

3:0 RVTRIM **Regulated Voltage Trim** — To adjust the regulated input

LCD Blink Control Register (LCDBCTL)

LCD Blink Control Register (LCDBCTL)

	7	6	5	4	3	2	1	0
R W	BLINK	ALT	BLANK		BMODE	BRATE2	BRATE1	BRATE0
Reset	0	0	0	0	0	0	0	0

7 BLINK **Blink Command** —To start LCD module blinking

6 ALT **Alternate Display Mode** —To start Alternate display mode for 4 backplanes or less configurations

5 BLANK **Blink Display Mode** —To start Blank display mode

3 BMODE **Blink Display Mode** —To select the blink mode displayed during the blink period

2:0 BRATE **Blink-Rate Configuration** —To select frequency at which the LCD display blinks

LCD Status Register (LCDS)

LCD Status Register (LCDS)

	7	6	5	4	3	2	1	0
R W	LCDIF							
Reset	0	0	0	0	0	0	0	0

7 LCDIF **LCD Interrupt Flag Command** —To indicate an interrupt condition occurred

LCD Pins and Waveforms Registers

LCD Pin Enable Register

Name		7	6	5	4	3	2	1	0
LCDPEN	R	PEN_{N+7}	PEN_{N+6}	PEN_{N+5}	PEN_{N+4}	PEN_{N+3}	PEN_{N+2}	PEN_{N+1}	PEN_{N}
	W								

LCD Back Pin Enable Register

Name		7	6	5	4	3	2	1	0
LCDBPEN	R	$BPEN_{N+7}$	$BPEN_{N+6}$	$BPEN_{N+5}$	$BPEN_{N+4}$	$BPEN_{N+3}$	$BPEN_{N+2}$	$BPEN_{N+1}$	$BPEN_{N}$
	W								

LCD Waveform Register

Name		7	6	5	4	3	2	1	0
LCDWF	R	BPHLCD	BPGLCD	BPFLCD	BPELCD	BPDLCD	BPCLCD	BPBLCD	BPALCD
	W								

LCD Pin Enable Register (LCDPEN)

LCD Pin Enable Register (LCDPEN)

	7	6	5	4	3	2	1	0
R W	PEN_{N+7}	PEN_{N+6}	PEN_{N+5}	PEN_{N+4}	PEN_{N+3}	PEN_{N+2}	PEN_{N+1}	PEN_{N}
Reset	0	0	0	0	0	0	0	0

7:0 PEN **LCD Pin Enable** —To enable LCD pin for LCD operation

LCD Backplane Pin Enable Register (LCDBPEN)

LCD Backplane Pin Enable Register (LCDBPEN)

	7	6	5	4	3	2	1	0
R W	$BPEN_{N+7}$	$BPEN_{N+6}$	$BPEN_{N+5}$	$BPEN_{N+4}$	$BPEN_{N+3}$	$BPEN_{N+2}$	$BPEN_{N+1}$	$BPEN_{N}$
Reset	0	0	0	0	0	0	0	0

7:0 BPEN **LCD Backplane Pin Enable** —To enable LCD pin as front plane or backplane for LCD operation

LCD Waveform Register (LCDWF)

LCD Waveform Register (LCDWF)

	7	6	5	4	3	2	1	0
R W	BPHLCDx	BPGLCDx	BPFLCDx	BPELCDx	BPDLCDx	BPCLCDx	BPBLCDx	BPALCDx
Reset	0	0	0	0	0	0	0	0

7:0 BP[y]LCD[x]

Segmemt-on-Frontplane Operation

– switch on/off state if this pin is configured as front plane at phase Y

Segment-on-Backplane Operation

– switch on/off state if this pin is configured as back plane at phase X

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Operate LCD Driver

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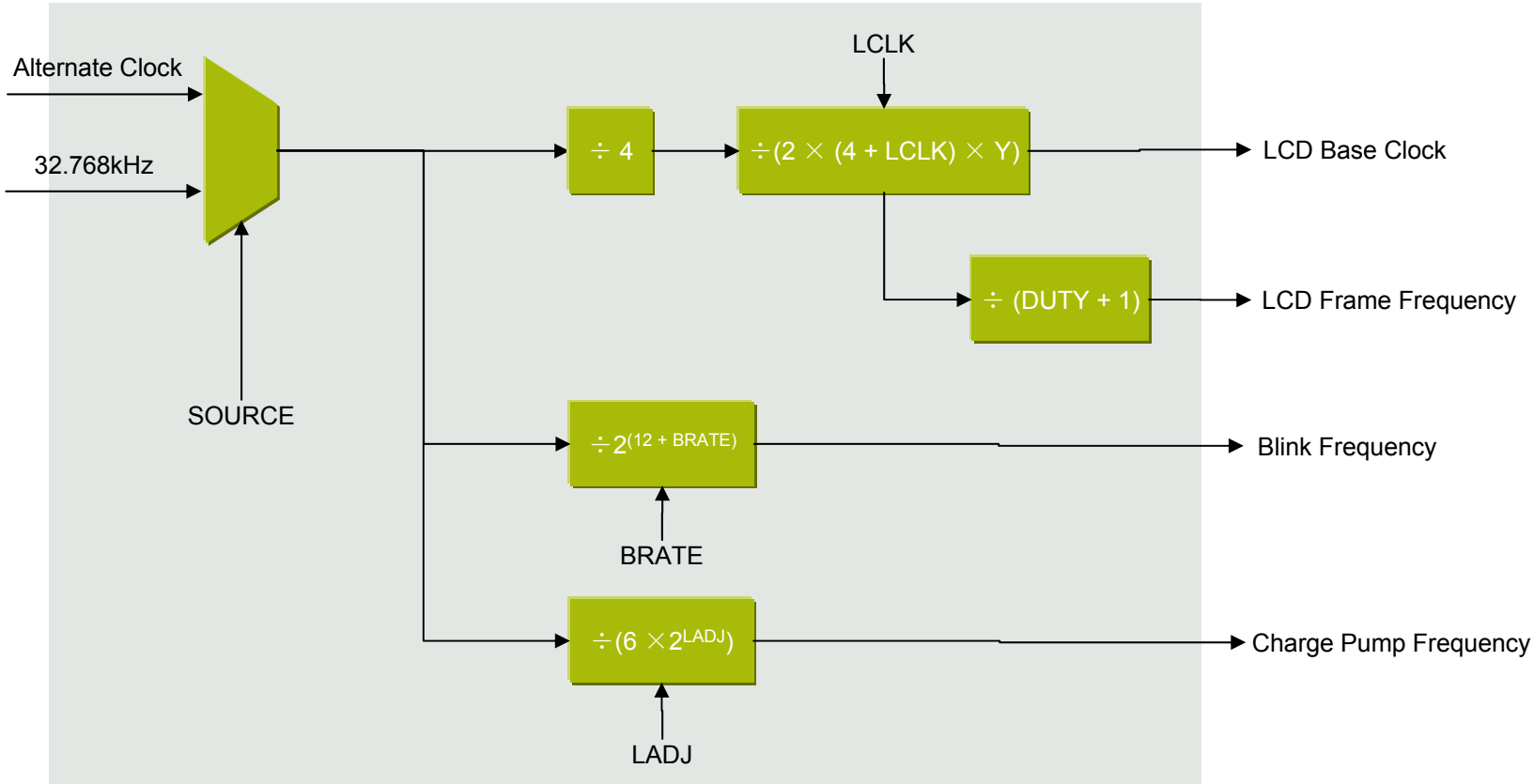
Operate LCD Driver

- Select LCD Clock Source
  - Select Internal or External Clock Reference
- Select LCD Power Supply
  - Select Internal or External Power Supply
  - Select Bias Voltage Generator
- Set LCD Duty Cycle and Bias
  - Select Correct Duty Cycle
  - 1/3 Bias
- Enable LCD Pin and Set Waveform
  - Enable LCD Pin
  - Enable LCD Backplane Pin
  - Set Wave form
- Special effects
  - Blink

Select LCD Clock Source

- LCD Clock Input
  - Optimized to operate using a 32.768kHz clock input
- LCD Clock Distribution
  - LCD Base Clock – To generate each Backplane phase
  - LCD Frame Frequency – To generate each Frame Timing (28 ~ 58Hz preferred)
  - LCD Charge Pump Clock – To generate bias voltages via charge pump
  - Blink Frequency

LCD Clock Distribution



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LCD Module Frame Frequency Calculation

Duty Cycle		1/1	1/2	1/3	1/4	1/5	1/6	1/7	1/8
Y		16	8	5	4	3	3	2	2
LCLK	0	64	64	68.3	64	68.3	56.9	73.1	64
	1	51.2	51.2	54.6	51.2	54.6	45.5	58.5	51.2
	2	42.7	42.7	45.5	42.7	45.5	37.9	48.8	42.7
	3	36.6	36.6	39	36.6	39	32.5	41.8	36.6
	4	32	32	34.1	32	34.1	28.4	36.6	32
	5	28.4	28.4	30.3	28.4	30.3	25.3	32.5	28.4
	6	25.6	25.6	27.3	25.6	27.3	22.8	29.3	25.6
	7	23.3	23.3	24.8	23.3	24.8	20.7	26.6	23.3

LCD input Frequency ~ 32.768kHz

28Hz <= Frame Frequency <= 58Hz

Frame Frequency < 28Hz
Or Frame Frequency > 58Hz

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LCD Module Frame Frequency Calculation

Duty Cycle		1/1	1/2	1/3	1/4	1/5	1/6	1/7	1/8
Y		16	8	5	4	3	3	2	2
LCLK	0	76.3	76.3	81.4	76.3	81.4	67.8	87.2	76.3
	1	61	61	65.1	61	65.1	54.3	69.8	61
	2	50.9	50.9	54.3	50.9	54.3	45.2	58.1	50.9
	3	43.6	43.6	46.5	43.6	46.5	38.8	49.8	43.6
	4	38.1	38.1	40.7	38.1	40.7	33.9	43.6	38.1
	5	33.9	33.9	36.2	33.9	36.2	30.1	38.8	33.9
	6	30.5	30.5	32.6	30.5	32.6	27.1	34.9	30.5
	7	27.7	27.7	29.6	27.7	29.6	24.7	31.7	27.7

LCD input Frequency ~ 39.0625kHz

28Hz <= Frame Frequency <= 58Hz

Frame Frequency < 28Hz
Or Frame Frequency > 58Hz

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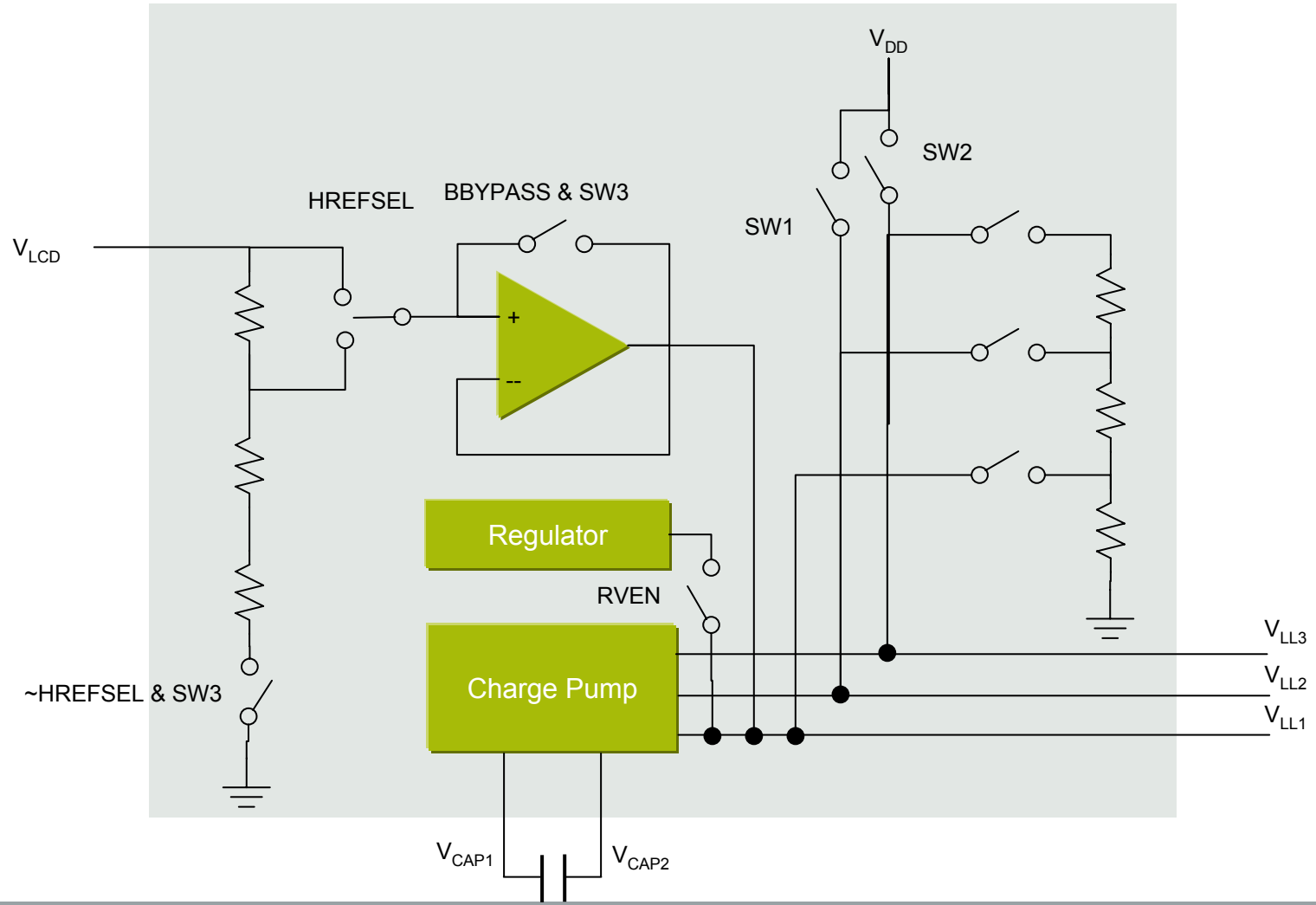
Select LCD Power Supply

- Power Supply Input
  - V_{LL2} internally from V_{DD}
  - V_{LL3} internally from V_{DD}
  - V_{LL1} internally from V_{LCD}
  - V_{LL3} externally from V_{DD}
  - V_{LL1} internally from V_{IREG}
- Bias Generator
  - Charge Pump
  - Resister Network
- V_{LCD} Operation
  - Voltage Divider
  - Op Amp Buffer
- V_{IREG} Operation
- Monitor LCD Voltage
  - V_{LCD} on AD20
  - V_{LL1} on AD21
  - V_{IREG} on AD22

LCD Charge Pump and V_{LCD} Voltage Divider



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LCD Charge Pump and V_{LCD} Voltage Divider

VSUPPLY[1:0]	Configuration	SW1	SW2	SW3
00	V_{LL2} internally from V_{DD}	1	0	0
01	V_{LL3} internally from V_{DD}	0	1	0
10	V_{LL1} internally from V_{LCD}	0	0	1
11	V_{LL3} externally from V_{DD} Or V_{LL1} internally from V_{IREG}	0	0	0

Set LCD Duty Cycle and Bias

- Set LCD Duty Cycle
  - Support 8 duty cycle modes of operation
    - 1/1 duty (1 backplane) (Phase A), 1/3 bias (4 voltage levels)
    - 1/2 duty (2 backplanes) (Phase A, B), 1/3 bias (4 voltage levels)
    - 1/3 duty (3 backplanes) (Phase A, B, C), 1/3 bias (4 voltage levels)
    - 1/4 duty (4 backplanes) (Phase A, B, C, D), 1/3 bias (4 voltage levels)
    - 1/5 duty (5 backplanes) (Phase A, B, C, D, E), 1/3 bias (4 voltage levels)
    - 1/6 duty (6 backplanes) (Phase A, B, C, D, E, F), 1/3 bias (4 voltage levels)
    - 1/7 duty (7 backplanes) (Phase A, B, C, D, E, F, G), 1/3 bias (4 voltage levels)
    - 1/8 duty (8 backplanes) (Phase A, B, C, D, E, F, G, H), 1/3 bias (4 voltage levels)

- Bias
  - The LCD module is designed to operate using the 1/3 bias mode

LCD Duty Cycle Modes

Duty	DUTY			Number of Backplanes	Phase Sequence
	DUTY2	DUTY1	DUTY0		
1/1	0	0	0	1	A
1/2	0	0	1	2	A B
1/3	0	1	0	3	A B C
1/4	0	1	1	4	A B C D
1/5	1	0	0	5	A B C D E
1/6	1	0	1	6	A B C D E F
1/7	1	1	0	7	A B C D E F G
1/8	1	1	1	8	A B C D E F G H

Enable LCD Pin and Set Waveform

- Enable LCD Pins
  - To enable all LCD pins connecting to LCD glass
- Enable LCD Backplane Pins
  - To enable LCD Backplane pins
  - Up to 8 LCD Backplane pins
- Set Waveform
  - Set Backplane Pins Phase
  - Set Front plane Pins contents

Enable LCD Pin and Set Waveform

LCD Pin: LCD0 ~ LCD29
8x21 mode
Backplane Pin: LCD7 ~ LCD14

```
// Initialize LCDPENx
LCDPEN0 = 0xFF;
LCDPEN1 = 0xFF;
LCDPEN2 = 0xFF;
LCDPEN3 = 0x1F;
// Initialize LCDBPENx
LCDBPEN0 = 0x80;
LCDBPEN1 = 0x7F;
LCDBPEN2 = 0x00;
LCDBPEN3 = 0x00;
// Initialize LCDWFx
LCDWF7 = 0x80;
LCDWF8 = 0x40;
LCDWF9 = 0x20;
LCDWF10 = 0x10;
LCDWF11 = 0x08;
LCDWF12 = 0x04;
LCDWF13 = 0x02;
LCDWF14 = 0x01;
```

Enable LCD Pins

Enable LCD Backplane Pins

Set LCD Backplane Phase

Design resources

- **Get started fast**

- **Get started with segment LCD solutions—freescale.com/8bit**
  - Documentation
  - CodeWarrior Development Studio for Microcontrollers 6.x
  - DEMOS08LL16 demo board ***$69***
  - DEMO9RS08LA8 demo board ***$59***
  - DEMO9RS08LE4 demo board ***$59***

- **Training and support—freescale.com/LCD**
  - Reference designs
  - Migration application notes
  - See a demonstration

- **Online courses—freescale.com/training**
  - RS08
  - HCS08

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Q & A

How Freescale beats the LCD design challenge

Challenge	Solutions
Too many pins required to drive many segments. Normally:	Freescale requires fewer pins to drive the same number of segments and also support 4x by mode
52 pins are required for 192 segments in 4x48 mode 44 pins are required for 160 segments in 4x40 mode 29 pins are required for 100 segments in 4x25 mode	32 pins are required for 192 segments in 8x24 mode 28 pins are required for 160 segments in 8x20 mode 17 pins are required for 104 segments in 8x13 mode
Blinking mode takes power and resources	Freescale offers a low-power blinking mode
Competitor parts offer blinking mode by setting a bit in a register. However, the microcontroller must exit stop mode, execute the code and then go back to sleep in every blinking period, which increases power consumption	Freescale's low-power blinking mode does not need to wake up the controller, Blinking mode can be activated and the CPU can go to sleep, but the segments will remain blinking at the pre-set frequency, In addition, an alternate display feature can be activated to display additional data (i.e., blink temperature and time)
Layout is very complex because the frontplanes (FPs) and backplanes (BPs) are fixed in pin-outs	Freescale offers FP and BP re- assignments
FPs and BPs are commonly distributed on all sides of the microcontroller, so special device placement and layout has to be performed to reduce electromagnetic interference (EMI) and shorten communication lines between the microcontroller and the LCD display. This makes the layout very complex, and implementing changes to improve EMI will be a time consuming task	FP and BP can be software selectable to be either FP or BP, making board layout an easier task and very flexible for changes
LCD glass requires many voltages, and voltage divider resistor ladders consume too much power	Freescale's internal charge pump provides all voltages required to power up LCD glass
Battery voltage drops over the time to the point where displays suffers degradation by not having the optimum voltage levels	Freescale solutions provide an internal software selectable regulated power supply that keeps constant voltage across LCD glass to avoid degradation. In addition, the LL16 offers 4 bits resolution trim to adjust contrast control (Only for S08 and V1 cores)

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Related Session Resources

Session Location – Online Literature Library

http://www.freescale.com/webapp/sps/site/homepage.jsp?nodeId=052577903644CB

Sessions

Session ID	Title

Demos

Pedestal ID	Demo Title

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