Freescale Technology Forum

Design Innovation.

November 2008

MPC837x and MPC8314/5 Power Architecture® Processors Interface Training

PN105

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Applications Engineer

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Agenda

- **Introductions**
- **MPC8315 and MPC837x**
  - Block Overview
  - Application Examples
- **Enablement**
  - MDS and RDB Development Platforms
  - Linux BSP and 3rd Party Support
- **New IPs Features & Performance**
  - SATA
  - PCIe
  - eTSEC
  - eSDHC
  - TDM
  - Security
  - Power Management

Next Generation PowerQUICC II Pro

▶Introducing the next generation PQ II Pro

- MPC837xE & MPC8315E families

▶Key Advantages for MPC837xE & MPC8315E

- **Integration**
  - **Key integration of Hard Disk Drive (HDD) SATA interface which reduces overall BOM cost**
  - **Integrated support for PCI-Express, to allow for high speed connectivity between SoC and peripheral devices.**
- **Scalability**
  - **Range of products from low cost consumer devices to high performance SMB applications, enabling customers to easily move up and down the value-chain**
- **Power Management**
  - **Low power (<2W for 8315, <4.4W for 837x) for battery backup applications and consumer/SMB devices.**
- **High Performance**
  - **Power Architecture™ e300 cores ranging from 266MHz to 667MHz for SMB & Consumer applications**
  - **Legacy code support**

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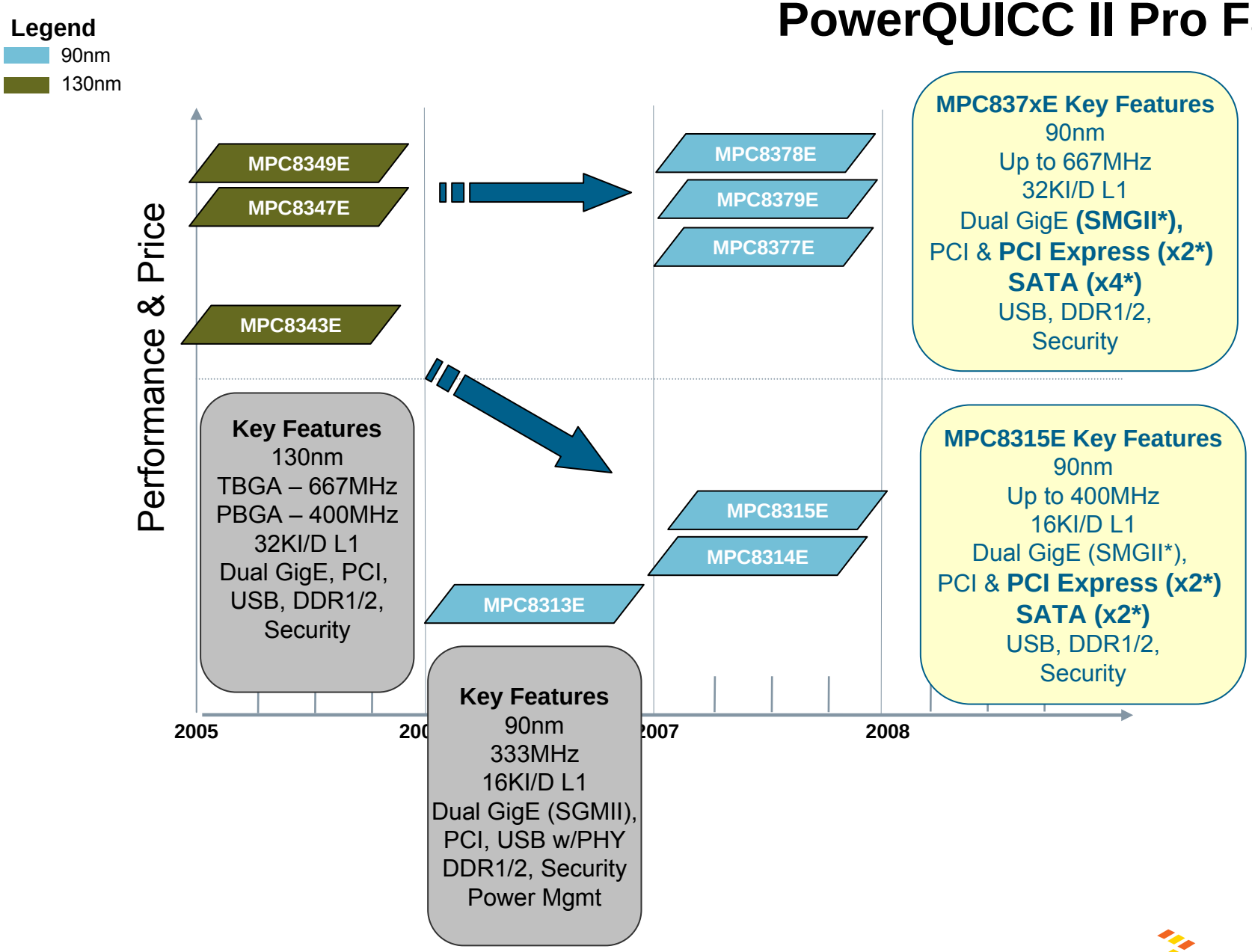
PowerQUICC II Pro Family



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MPC834xE vs MPC837xE

Feature	MPC8349E	MPC8347E	MPC8377E	MPC8378E	MPC8379E
Core	e300	e300	e300	e300	e300
CPU Speed	667 MHz *(TBGA)*	667 MHz *(TBGA)* 400MHz *(PBGA)*	Up to 667 MHz	Up to 667 MHz	Up to 667 MHz
L1 I/D Cache	32K I/D	32K I/D	32K I/D	32K I/D	32K I/D
Memory Controller	64/32 bit DDR2	64/32 bit DDR2	64/32 bit DDR2 400MHz	64/32 bit DDR2 400MHz	64/32 bit DDR2 400MHz
Ethernet	2-10/100/1000	2-10/100/1000	2-10/100/1000	2-10/100/1000 with SGMII	2-10/100/1000
PCI	2-32Bit OR 1-64bit up to 66MHz	1-32bit up to 66MHz	1-32Bit (2.3) up to 66MHz	1-32Bit (2.3) up to 66MHz	1-32Bit (2.3) up to 66MHz
PCI-E	-	-	2-x1 or 1-x2	2-x1 or 1-x2	-
SATA	-	-	x2	-	x4
USB	Hi-Speed Host or Device	Hi-Speed Host or Device	Hi-Speed Host or Device	Hi-Speed Host or Device	Hi-Speed Host or Device
Security	E version only	E version only	E version only	E version only	E version only
Package	672 TBGA	672 TBGA 620 PBGA	689 TePBGA	689 TePBGA	689 TePBGA
Power	~3.5W	~3.5W	~3.3W	~3.3W	~3.3W
Samples	Now	Now	Now	Now	Now
Production	Now	Now	Dec-08	Dec-08	Dec-08
Technology	130nm	130nm	90nm	90nm	90nm

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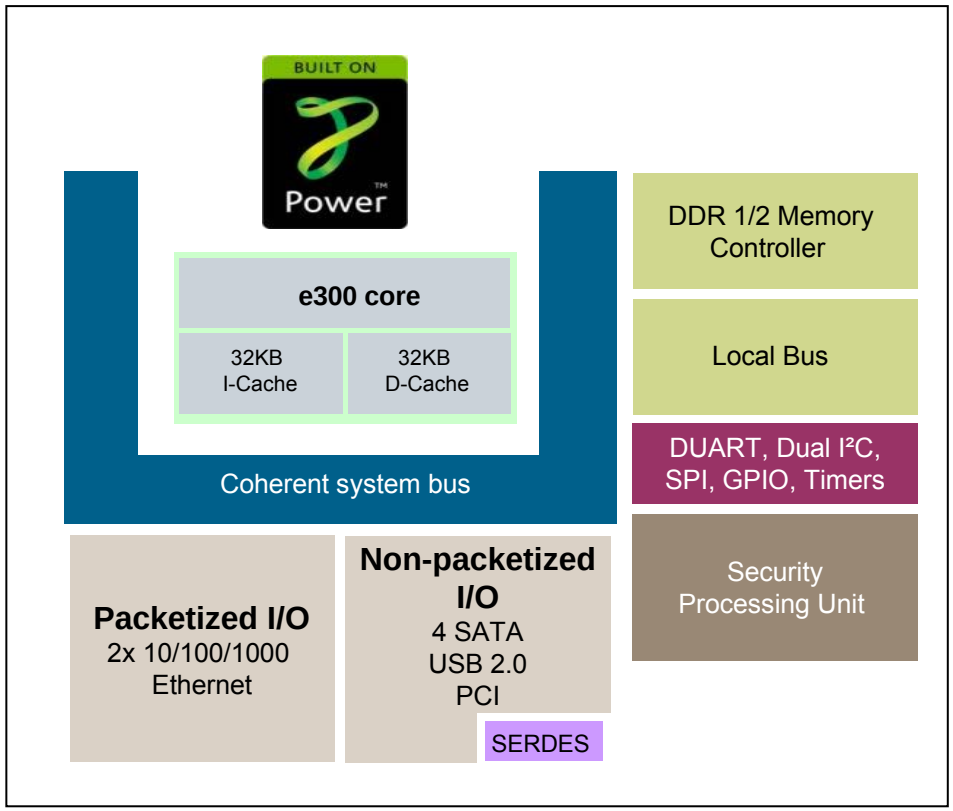
MPC8379E Block Diagram

MPC8379E



- General Sampling: Now
- Qualification: Dec 2008
  - *689 TePBGA Package*

Functional Requirements

- e300 core from 400-667MHz with floating point
- 32K D/I L1 cache

I/O Description

- 32/64 bit DDR1/2 400MHz with ECC
- Local Bus w/NAND support
- 1 PCI 2.3, 32bit up to 66MHz
- 1 USB2.0 (Host or Device)
- **4 SATA I/II (3.0Gb/s) controllers**
- 2 10/100/1000 enhanced Ethernet MACs
  - RGMII, RTBI, RMII, MII
  - Support for IEEE 1588 Rev 1.0
- Multi-channel DMA controller

Security Processing Unit

- AES, PKEU, DES, 3DES, MDEU, ARC4, XOR, CRC32C, RNG
- Optimized for IPSEC & DTCP-IP

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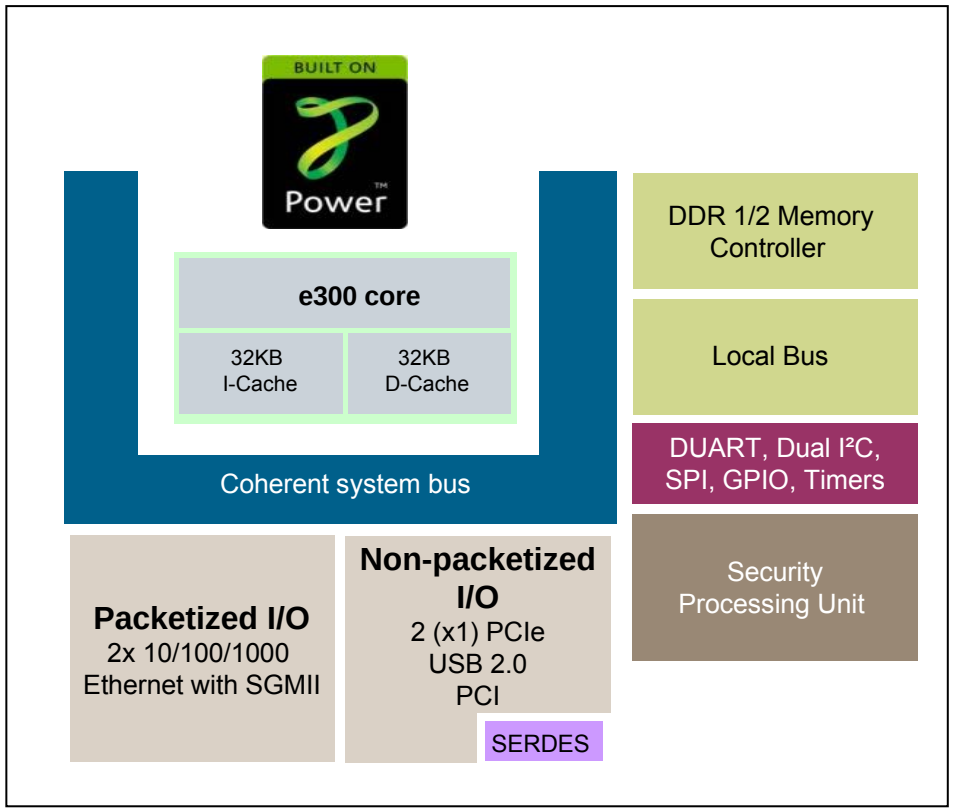
MPC8378E Block Diagram

MPC8378E



- General Sampling: Now
- Qualification: Dec 2008
  - *689 TePBGA Package*

Functional Requirements

- e300 core from 400-667MHz with floating point
- 32K D/I L1 cache

I/O Description

- 32/64 bit DDR1/2 400MHz with ECC
- Local Bus w/NAND support
- 1 PCI 2.3, 32bit up to 66MHz
- 1 USB2.0 (Host or Device)
- **2 x1 PCI Express v1.0a**
- 2 10/100/1000 enhanced Ethernet MACs
  - **SGMII**, RGMII, RTBI, RMII, MII
  - Support for IEEE 1588 Rev 1.0
- Multi-channel DMA controller

Security Processing Unit

- AES, PKEU, DES, 3DES, MDEU, ARC4, XOR, CRC32C, RNG
- Optimized for IPSEC & DTCP-IP

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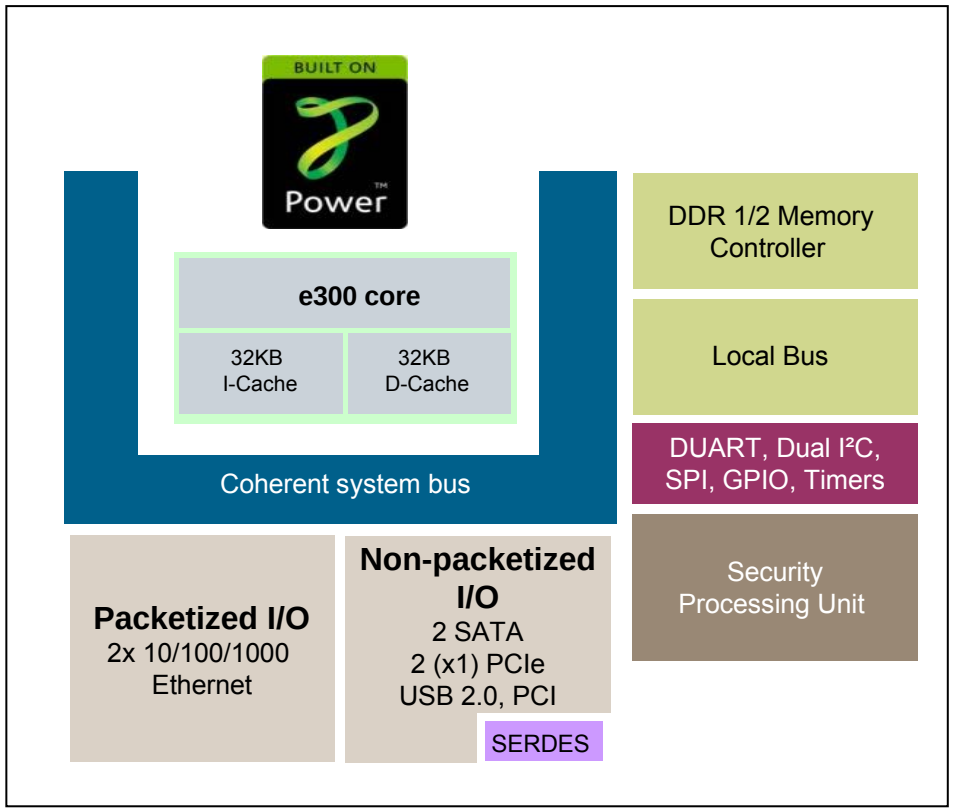
MPC8377E Block Diagram

MPC8377E



- General Sampling: Now
- Qualification: Dec 2008
  - *689 TePBGA Package*

Functional Requirements

- e300 core from 400-667MHz with floating point
- 32K D/I L1 cache

I/O Description

- 32/64 bit DDR1/2 400MHz with ECC
- Local Bus w/NAND support
- 1 PCI 2.3, 32bit up to 66MHz
- 1 USB2.0 (Host or Device)
- **2 SATA I/II (3.0Gb/s) controllers**
- **2 x1 PCI Express v1.0a**
- 2 10/100/1000 enhanced Ethernet MACs
  - RGMII, RTBI, RMII, MII
  - Support for IEEE 1588 Rev 1.0
- Multi-channel DMA controller

Security Processing Unit

- AES, PKEU, DES, 3DES, MDEU, ARC4, XOR, CRC32C, RNG
- Optimized for IPSEC & DTCP-IP

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MPC8313E vs MPC8315/4E

Feature	MPC8343E	MPC8313E	MPC8315E	MPC8314E
Core	e300	e300	e300	e300
CPU Speed	Up to 400MHz	Up to 333 MHz	Up to 400 MHz	Up to 400 MHz
L1 I/D Cache	32K I/D	16K I/D	16K I/D	16K I/D
Memory Controller	32 bit DDR2	16/32 bit DDR/2 up to 333MHz	16/32 bit DDR/2 up to 266MHz	16/32 bit DDR/2 up to 266MHz
Ethernet	2-10/100/1000 (MII, RGMII & RTBI only)	2-10/100/1000 with SGMII	2-10/100/1000 with SGMII	2-10/100/1000 with SGMII
PCI	1-32bit up to 66MHz	1-32Bit up to 66MHz	1-32Bit (2.3) up to 66MHz	1-32Bit (2.3) up to 66MHz
PCI-E	-	-	x2	x2
SATA	-	-	x2	-
USB	Hi-Speed Host or Device	1 -2.0 Host or Device w/PHY	1 -2.0 Host or Device w/PHY	1 -2.0 Host or Device w/PHY
Security	E version only	SEC 2.2	SEC 3.0	SEC 3.0
Other	-	-	-	-
Package	620 PBGA	516 TePBGA	620 TePBGA	620 TePBGA
Power		~2W @ 333MHz	~1.6W	~1.6W
Samples	Now	Now	Now	Now
Production	Now	Now	June-08	June-08
Technology	130nm	90nm	90nm	90nm

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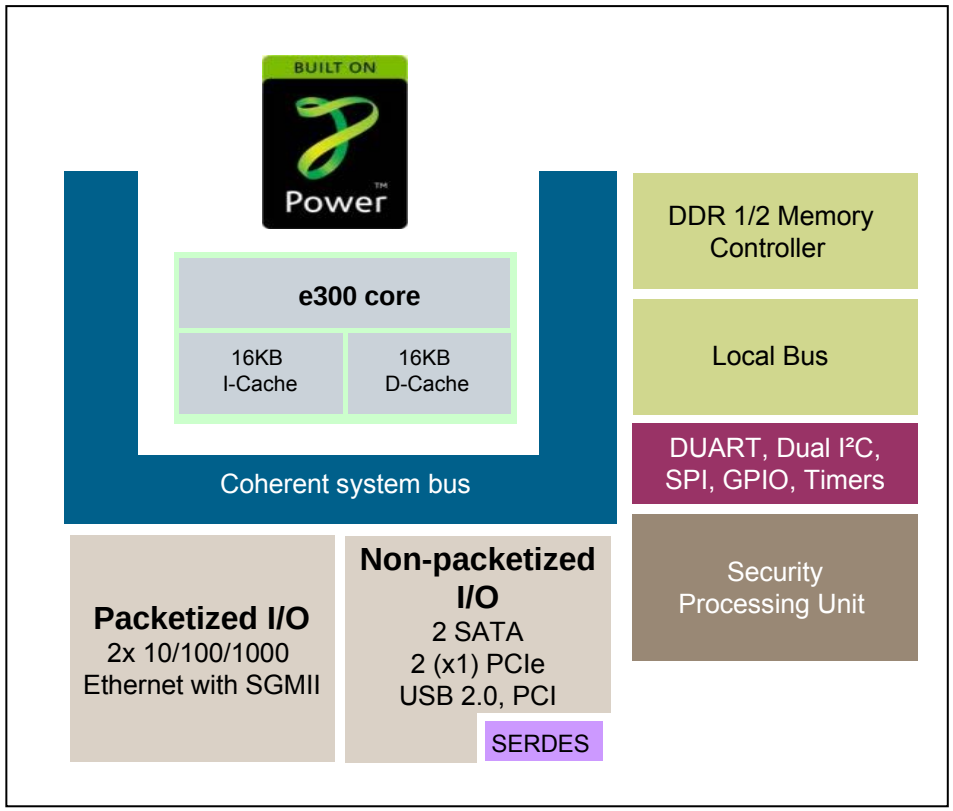
MPC8315E Block Diagram

MPC8315E



- ▶General Sampling: Now
- ▶Qualification: June 2008
  - *620 TePBGA Package*

▶Functional Requirements

- e300 core from 266-400MHz with 16K D/I L1 cache
- 2nd ALU for 2 channel voice support

▶I/O Description

- 16/32 bit DDR1/2 266MHz
- Local Bus
- 1 PCI 2.3, 32bit up to 66MHz
- 1 USB2.0 (Host/Device **with PHY**)
- **2 SATA I/II (3.0Gb/s) controllers**
- **2 x1 PCI Express v1.0a**
- 2 10/100/1000 enhanced Ethernet MACs
  - RGMII, RTBI, RMII, MII, **SGMII muxed with PCIe**
- Multi-channel DMA controller

▶Security Processing Unit

- AES, PKEU, DES, 3DES, MDEU
- Optimized for IPSEC & DTCP-IP

▶Legacy Protocol Support

- TDM – to connect to CODEC

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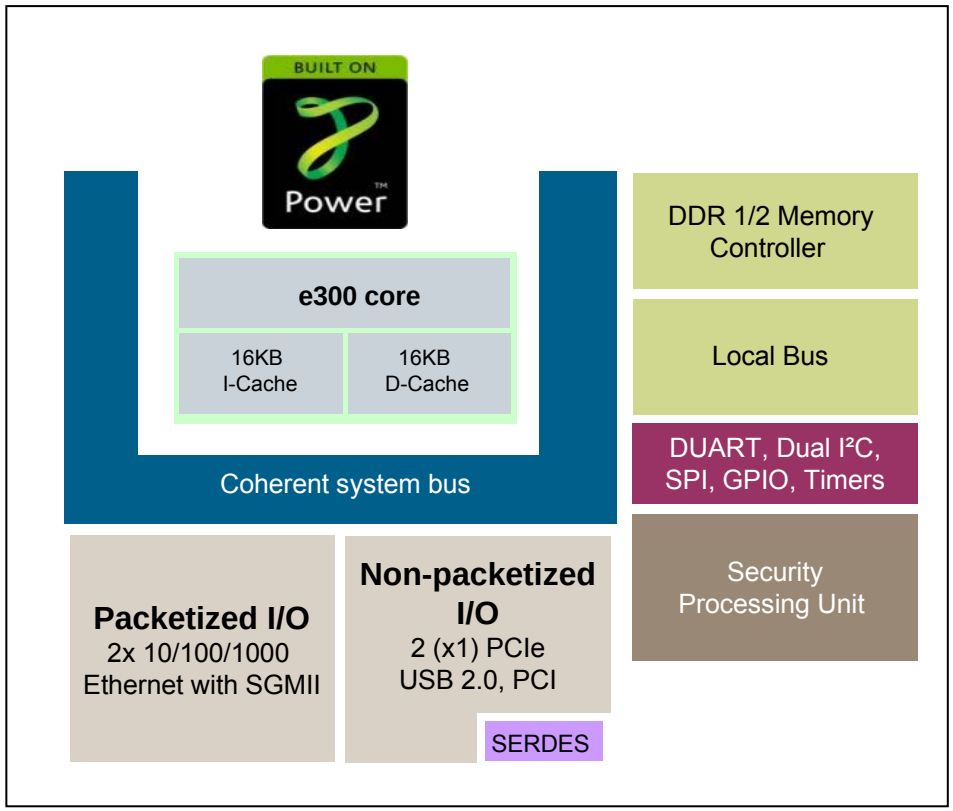
MPC8314E Block Diagram

MPC8314E



- General Sampling: Now
- Qualification: June 2008
  - *620 TePBGA Package*

Functional Requirements

- e300 core from 266-400MHz with 16K D/I L1 cache
- 2nd ALU for 2 channel voice support

I/O Description

- 16/32 bit DDR1/2 266MHz
- Local Bus
- 1 PCI 2.3, 32bit up to 66MHz
- 1 USB2.0 (Host/Device **with PHY**)
- **2 x1 PCI Express v1.0a**
- 2 10/100/1000 enhanced Ethernet MACs
  - RGMII, RTBI, RMII, MII, **SGMII muxed with PCIe**
- Multi-channel DMA controller

Security Processing Unit

- AES, PKEU, DES, 3DES, MDEU
- Optimized for IPSEC & DTCP-IP

Legacy Protocol Support

- TDM – to connect to CODEC

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Product Schedules

Deliverable	MPC8379E	MPC8378E	MPC8377E	MPC8315E	MPC8314E
Samples	*PPC8377EVRAGD* *PPC8377EVRAGD A (2.1)* ***(400/266)*** *PPC8377EVRAJD* *PPC8377EVRAJD A (2.1)* ***(533/266)*** *PPC8377EVRALG* *PPC8377EVRALG A (2.1)* ***(667/400)***	*PPC8378EVRAGD* *PPC8378EVRAGD A (2.1)* ***(400/266)*** *PPC8378EVRAJD* *PPC8378EVRAJDA (2.1)* ***(533/266)*** *PPC8378EVRALG* *PPC8378EVRALGA (2.1)* ***(667/400)***	*PPC8379EVRAGD* *PPC8379EVRAGD A (2.1)* ***(400/266)*** *PPC8379EVRAJD* *PPC8379EVRAJD A (2.1)* ***(533/266)*** *PPC8379EVRALG* *PPC8379EVRALG A (2.1)* ***(667/400)***	*PPC8315EVRADD* ***(266/266)*** *PPC8315EVRAFD* ***(333/266)*** *PPC8315EVRAGD* ***(400/266)***	*PPC8314EVRADD* ***(266/266)*** *PPC8314EVRAFD* ***(333/266)*** *PPC8314EVRAGD* ***(400/266)***
Boards	MPC8379E-MDS-PB MPC8379E-RDB	MPC8378E-MDS-PB	MPC8377E-MDS-PB MPC8377E-RDB	MPC8315E-RDB	MPC8315E-RDB
Market Launch	**Sept 2007**	**Sept 2007**	**Sept 2007**	**Sept 2007**	**Sept 2007**
Qualification	**Dec 2008**	**Dec 2008**	**Dec 2008**	**June 2008**	**June 2008**
10K Resale	**$28-37**			**$17-19**	

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Markets & Applications

MPC837xE & MPC8315/4E

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MPC834x -> MPC837x Applications

MPC834x Applications Today

Industrial

- Video Surveillance
- Instrumentation Panel
- Security
- Video Conferencing
- Servers
- IC Tester
- Sensing

Networking

- Access Points
- Routers
- Control Cards
- Optical Units

Home/Media

- Printer (MFP/Mono/Color)
- Scanner
- Media Gateway
- Residential Gateway
- Network Attached Storage
- Audio Players

MPC837x Applications

Industrial

Networking

Home/Media

- Applications requiring **more I/O connectivity**: PCI & PCI-E
- Applications requiring **more storage** interfaces: SATA
- Applications requiring **more system performance**: higher DDR interface, NAND boot support, next gen security

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Video Surveillance Example

MPC834x Benefits
MPC837x Benefits

SDRAM

Up to 400MHz for faster system performance

Flash

Boot from NAND support

MPC8347E
MPC8377E

DDR

667MHz Core & 32K L1 I/D

SATA

Security

x2 Ethernet

USB

PCI-E

PCI

Ethernet Switch

LAN/WAN

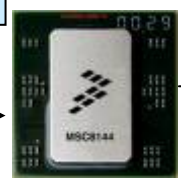
Hard Disk Drives

Used for local storage - eliminates need for external SATA controller

Input Device

CPU Chassis or Add-in Card

Support migration from PCI to PCI-E



DSP

Allows DSP connection through PCI and/or Ethernet for video analytics

FPGA

Cameras

MPC837x enables higher integration with additional I/O connectivity!

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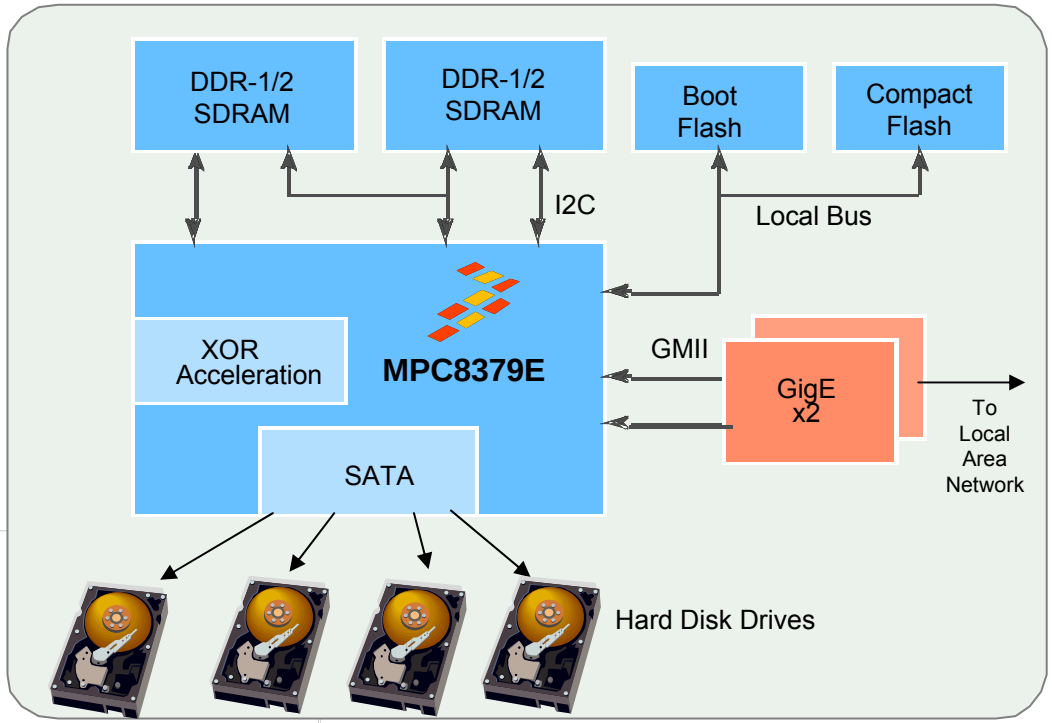
Network Attached Storage Example

Applications for NAS

- Small/Medium Business, Remote branch offices

- Military Applications
  - Future Combat System (FCS) within armored vehicles, UAVs

- Consumer Home



Benefit	Feature
Reducing BOM cost and board space by lowering chip count	Integrated x4 SATA controller eliminates need for external SATA controller and can connect directly up to 4 HDD
Higher overall system performance for RAID functionality	XOR engine that allows for hardware-supported RAID 5
High speed connectivity to Ethernet LAN	Integrated dual Gigabit Ethernet controllers allowing high speed connectivity

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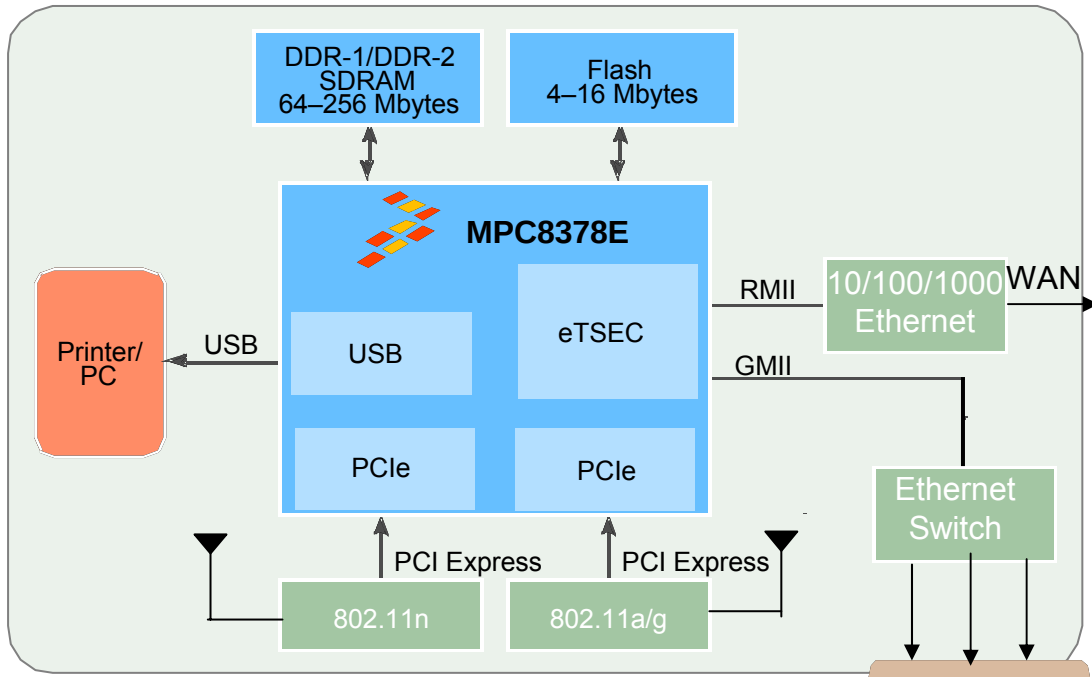
Wireless LAN Router Example

Applications for Wireless LAN

- Businesses
- Military Applications

- Factories & Building Control

- Consumer Home



Benefit	Feature
Support for up to two 802.11 chipsets to provide support for multiple WLAN	Two x1 PCIe controllers integrated for wireless 802.11 support.
Gigabit Ethernet connections to support Ethernet switches and connections to WAN	Integrated dual 10/100/1000 Ethernet controllers
High overall system performance for networking applications	E300 core based on Power Architecture running up to 667MHz at 1.95DMIPS/MHZ

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MPC8313 -> MPC8315 Applications

MPC8313 Applications Today

Industrial

- Video Surveillance
- Instrumentation Panel
- Security
- Test & Measurement
- Sensing

Networking

- WiFi Access Points
- Wimax CPE
- Routers
- Control Cards

Home/Media

- Printer (MFP/Mono/Color)
- Residential Gateway
- Network Attached Storage

MPC8315 Applications

Industrial

Networking

Home/Media

- Applications requiring **more I/O connectivity**: PCI & PCI-E
- Applications requiring **more storage** interfaces: SATA
- Applications requiring **VoIP support**: TDM interface available for 2 channel VoIP on the e300 platform

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Triple Play Distribution - Voice / Video / Data

MPC8313 Benefits
MPC8315 Benefits

SDRAM
Up to 266MHz

Flash
Boot from NAND support

MPC8313E
MPC8315E

DDR2

TDM

400MHz Core & 16K L1 I/D

SATA

Security

x2 Ethernet

USB w/ Phy

PCI-E

PCI

Hard Disk Drives

Used for local storage - eliminates need for external SATA controller

Ethernet Switch

WAN

LAN

Input Device

802.11n Chipset

Support migration from PCI to PCI-E

MPC8315 enables higher integration with more I/O connectivity!

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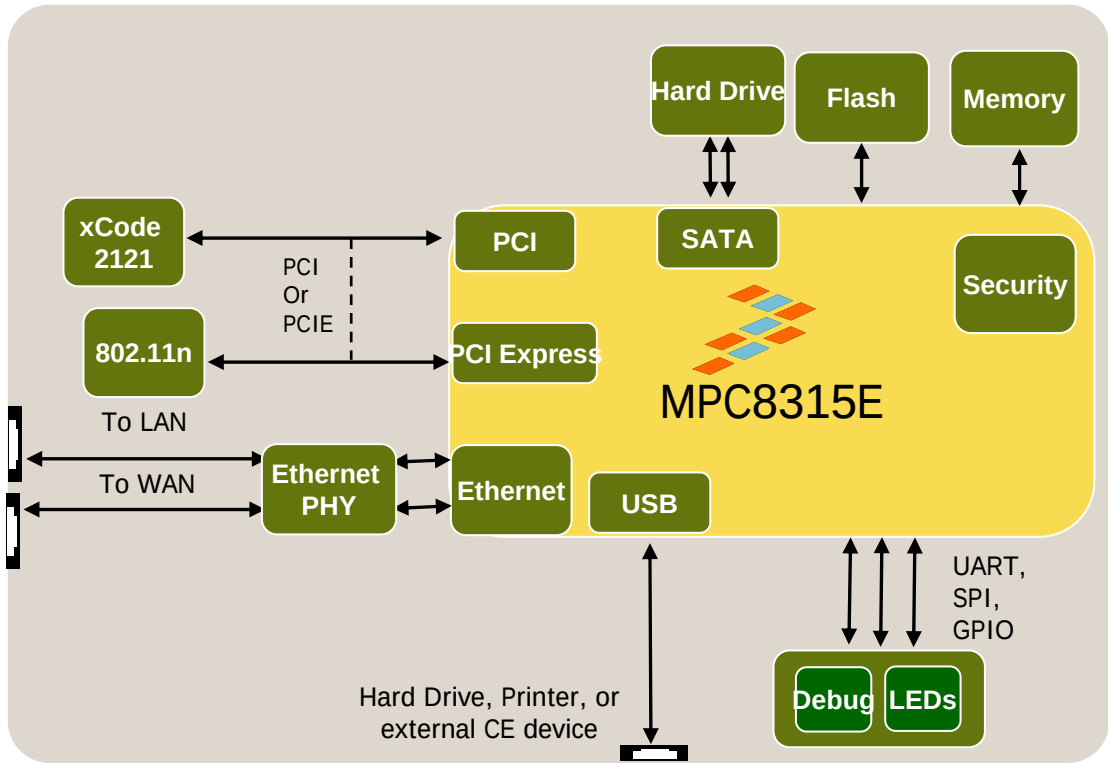
Media Distribution

Applications for DMS

• Digital TV

• Medical / Imaging (PCI Express)

• Video Surveillance



Benefit	Feature
Reducing BOM cost and board space by lowering chip count	Integrated x2 SATA controller eliminates need for external SATA controller and can connect directly up to 2 HDD
Higher overall system performance for RAID functionality	XOR engine that allows for hardware-supported RAID 0,1
High speed connectivity to Ethernet LAN	Integrated dual Gigabit Ethernet controllers allowing high speed connectivity

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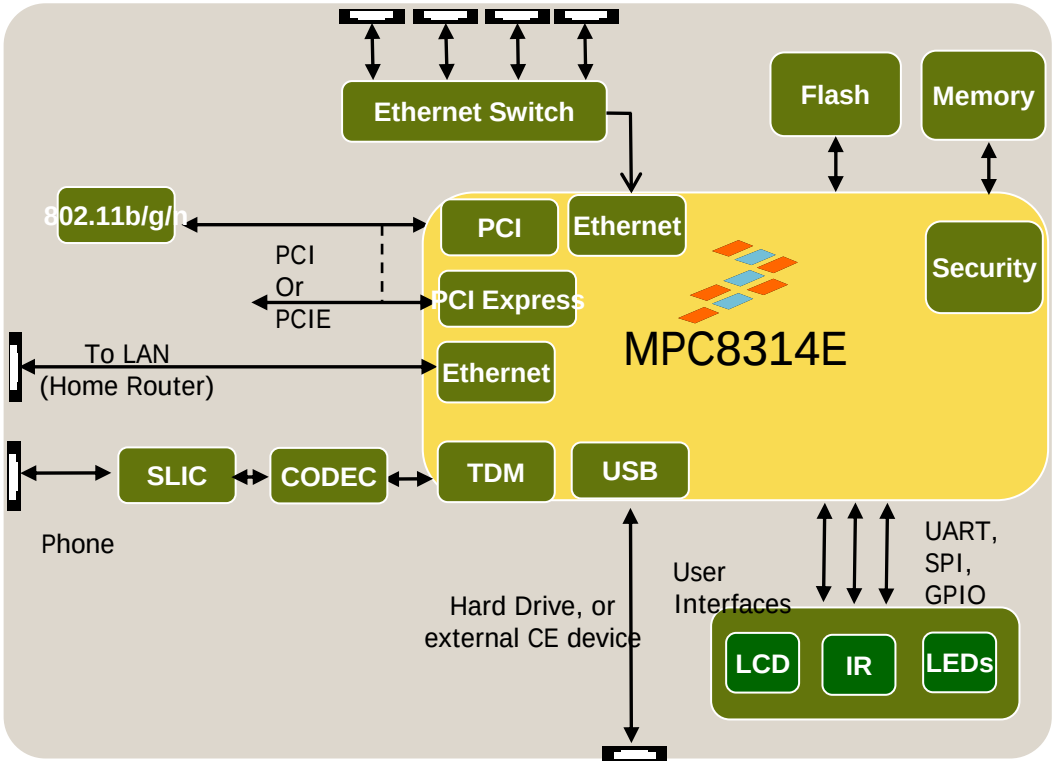
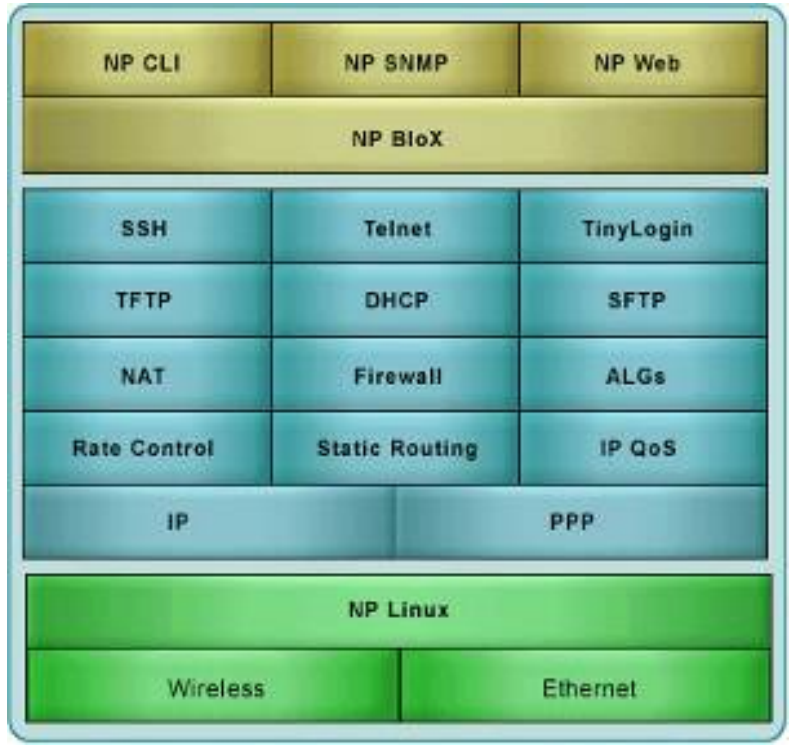
MPC8314E - Low End Voice Gateway System





Benefit	Feature
High I/O connectivity for support to multiple 802.11 WIFI/WiMAX	Support for both 32-bit PCI and 2 x1 PCIe for high I/O connectivity
High overall system performance for networking applications	E300 core based on Power Architecture running up to 400 MHz at 1.95DMIPS/MHZ

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MPC8315/7x Value Proposition

Features	Customer System Impact & Savings
Ability to scale from 400MHz – 667MHz (MPC837x) Ability to scale from 266MHz – 400MHz (MPC8315)	Can reuse design for high-end to low-end products. Saves the cost of additional engineering team.
Integrated SATA controller	Replace external SATA controller ($3 for x4 SATA controller), reducing board space and overall system cost
Integrated SGMII for Ethernet connectivity	Replace external SGMII PHY
Integrated PCI Express	More I/O bandwidth and higher system performance
Low Power: <4.1W for 837x, <1.6W for 8315	Fan less operation, more reliable
Reference Design Boards & Linux BSP	Minimize design and development time
Software ports easily from e300 core PowerQUICC® processors	Reduced time to market, lower risk, lower development cost

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MPC8377/8/9 & MPC8314/5 Enablement

Development Boards, Linux BSP & 3rd Party Support

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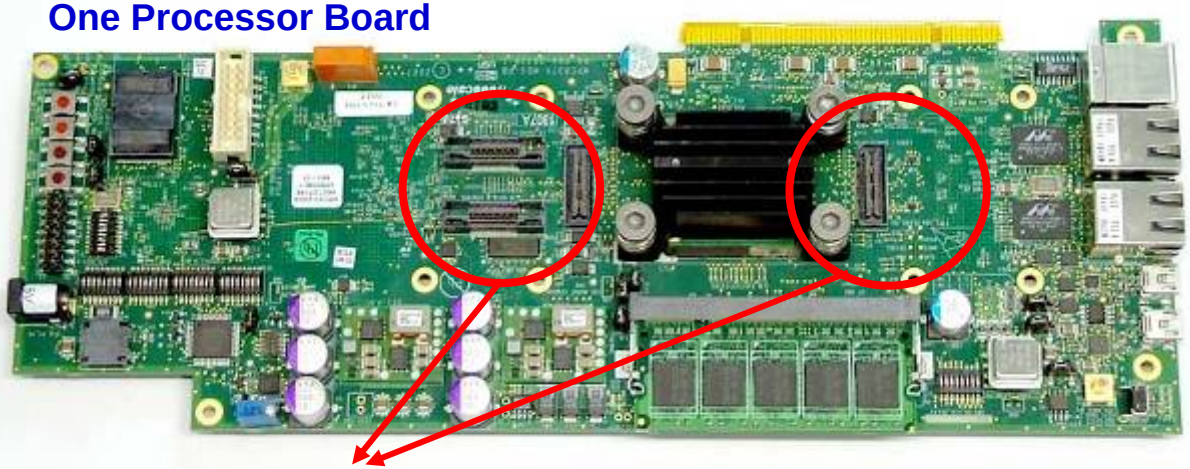
MPC8377/8/9 MDS Board

MPC837x MDS Kit Board Includes:

One Processor Board



& High Speed Serial Interface Modules

MDS Features

- MPC837x at 667MHz
- 512MB DDR2 up to 400MHz data rate
- 32bit PCI
- Dual GigaE supporting RGMII, RTBI, MII and SGMII
- USB 2.0 for High/Full speed
- 32MB NOR flash, 32MB NAND flash
- Dual RS232 to DUART
- SD Connector
- 4Mbit SPI Flash

PCI Express Module

1 PCIe Module
MPC8377 & MPC8378

SGMII Module

1 SGMII Module MPC8378

SATA Module

1 SATA Module MPC8377
2 SATA Modules MPC8379

Part Number	Description	SRC Price
MPC8377E-MDS-PB	► Includes 1 processor board, 1 SATA card, 1 PCIe card	$2,900.00
MPC8378E-MDS-PB	► Includes 1 processor board, 1 PCIe card, 1 SGMII card	$2,900.00
MPC8379E-MDS-PB	► Includes 1 processor board, 2 SATA cards	$2,900.00

Now Available

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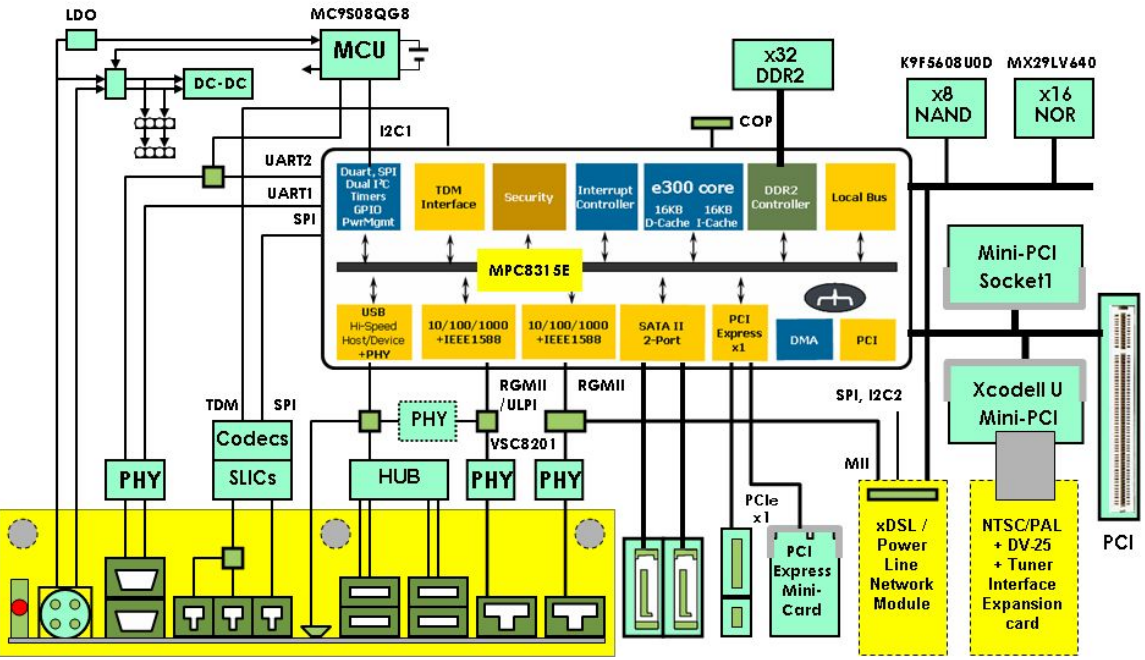
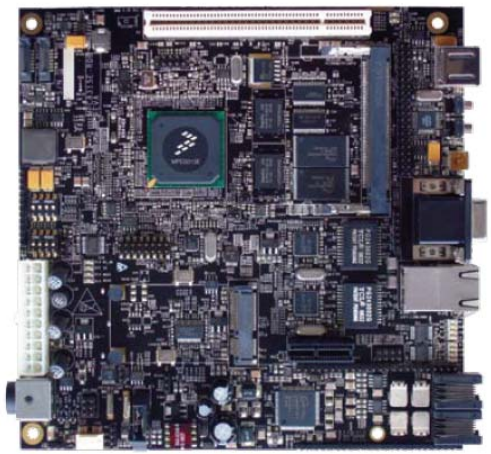
MPC8315E-RDB board





RDB Part Numbers & Price

Part Number	SRC Price
MPC8315E-RDB	$499.00

Available Now

- **CPU**
  - MPC8315E
- **Ethernet**
  - 2 Gigabit RGMII connections directly to phys.
  - One Ethernet connection to broadband powerline capability using DS2
- **PCI Express**
  - x1 PCI Express Add-in Connector
  - miniPCI Express for WLAN
- **SATA**
  - 2 standard SATA connectors
    - eSATA will be available through SATA-eSATA connectors
- **SPI / TDM**
  - Connected to dual Legerity SLIC/SLAC
- **USB Hi-Speed**
  - Connector directly on board
  - 3 port USB Hub
- **PCI**
  - One Standard and one MiniPCI connectors
- **Memory**
  - 32-bit DDR2 with population option for 16-bit.

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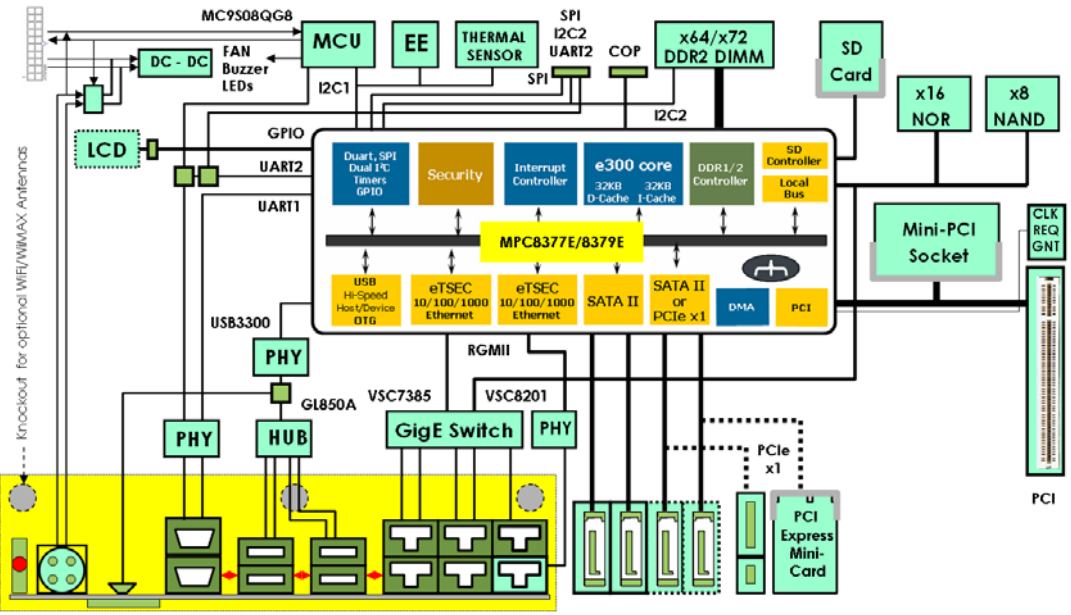
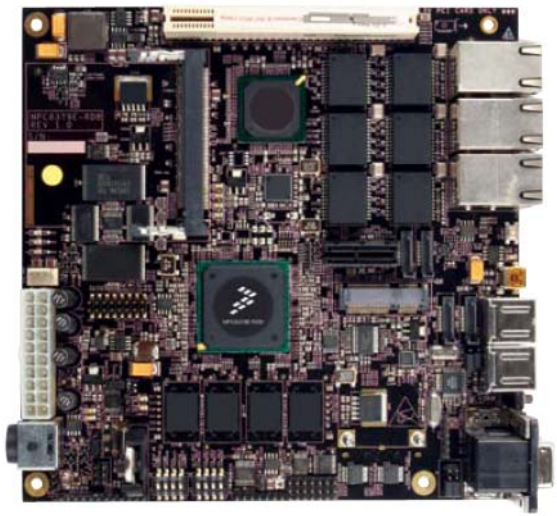
MPC8377/9 RDB Board





RDB Part Numbers & Price

Part Number	SRC Price
MPC8379E-RDB	$699.00
MPC8377E-RDB	$699.00

Available Now

Reference Design Board Features

- ***CPU***
  - Freescale MPC8379E
- ***Ethernet***
  - 1 Gigabit RGMII connect to Vitesse GE Phy
  - 5-Port Vitesse Ethernet Switch
- ***PCI Express and PCI***
  - PCI Express Add-in Connector
  - miniPCI Express for WLAN
  - One Standard PCI connector with
  - extended for riser card
  - One Mini-PCI connector
- ***SATA II***
  - 2 or 4 standard SATA connectors
- ***USB 2.0 Hi-Speed***
  - 4 port USB Hub or 1-port USB OTG (jumper selectable)
  - GL850A 4 port HUB
- ***Interfaces***
  - Dual UART
  - Connectors for debug connectivity
  - NAND flash and NOR flash

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Ecosystem Support
Designs up and Running Quickly

- MPC837x and MPC8315 are supported by many operating systems, compilers, debuggers and more.

Examples but not inclusive are:

Code-Warrior	FalconStor
WindRiver	Axentra
Green Hills	Mediabolic
MontaVista	Ralink

- A complete listing of the ecosystem can be found at http://www.freescale.com and access the Quick Links - “Alliances”

- Contact your ecosystem partner for availability.

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New IP Overview: SATA

MPC837x & MPC8315 New IP Overview

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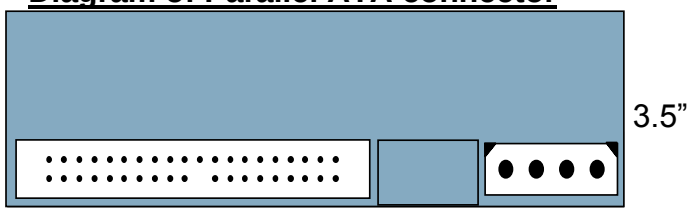
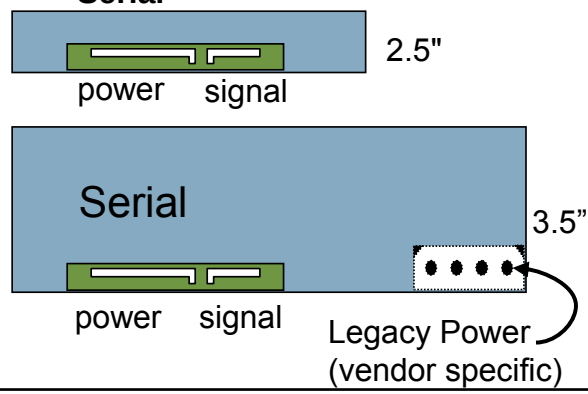
Why use Serial-ATA?

	Parallel ATA	Serial-ATA II
Bandwidth	▶Limited to 133MB/s	▶ 150MB/s -- Generation 1 ▶ 300MB/s -- Generation 2
CRC	▶Cyclic Redundancy Checking (CRC) for data but not commands	▶Supports CRC for data and commands
Command Queuing	▶Not supported	▶Support for native command queuing
Cables/ Connectors	▶Wide cables inhibit airflow, making cooling more difficult and expensive ▶High pin count on signaling interface adds cost ▶Connectors hard to plug and prone to bent pins **Diagram of Parallel ATA connector**  	▶Lower pin count & smaller cables **Diagram of Serial ATA connector** 
Additional Device Support	▶Support attachment of 2 devices per cable	▶Support for redundant hosts (Port Selector) ▶Support for adding more ports (Port Multiplier)

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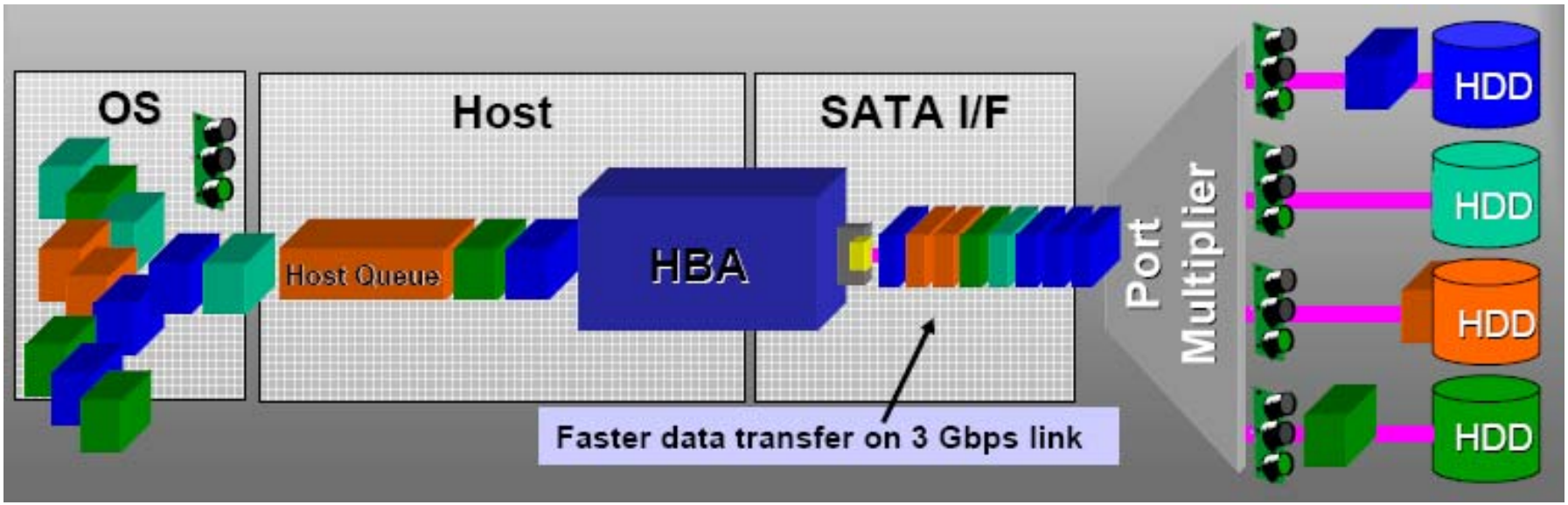
SATA Port Multipliers

- Port multipliers attach up to 15 devices to a host
  - Store and forward frames from host based on a field in the header. Port Multiplier strips off this field and zeros it.
  - Supplies the field for frames going back to host



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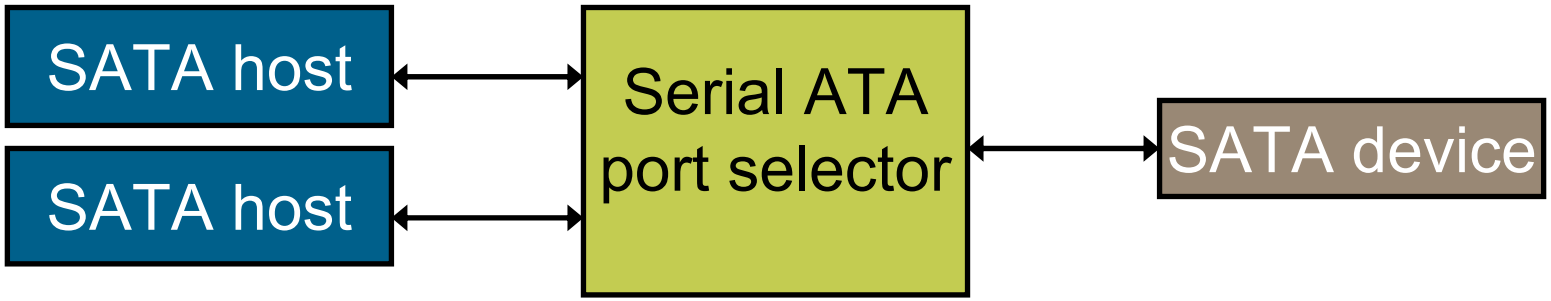
SATA Port Selectors

- Allows a device to talk with two hosts
  - Provides dual-ported option
  - First host to run OOB is active, latecomer is inactive
  - Switch over
    - Inactive host can take control by sending a particular sequence of COMINIT OOB signals



Characteristics of Port Selectors

- No modifications to Serial ATA 1.0a devices required
- No hardware modification required for Host Adapters
- No new primitives needed
- No new FIS types needed
- A port selector should not need full-function link and transport layers
- Host port connections limited to two
- Only one port can be active at a time
- Port selectors cannot be cascaded

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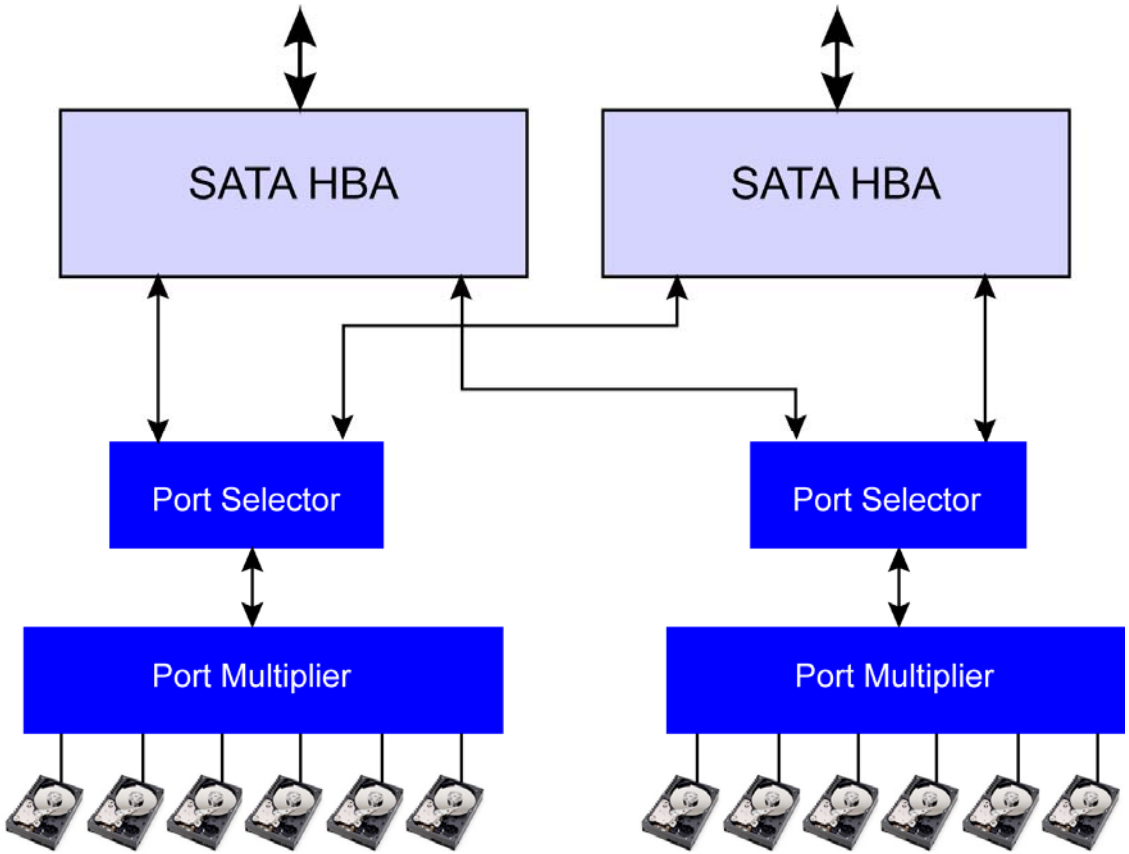
SATA Port Multiplier and Selector

Combination of port selectors and port multipliers provides options for the user



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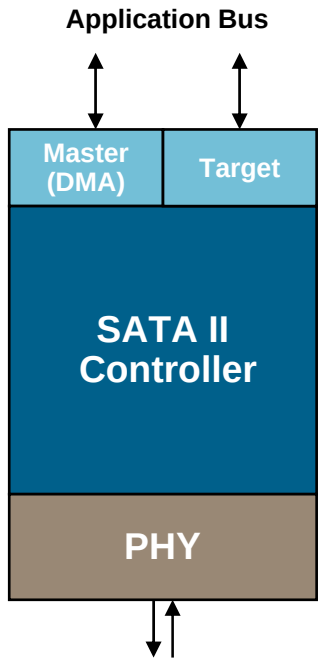
MPC837x/8315 SATA II Controller IP

- **Supports Host SATA II**
  - OOB
  - Port Multipliers
  - ATAPI 6+
  - Spread Spectrum clocking on Receive
- **Support for SATA II Extensions**
  - Asynchronous Notification
  - Hot Plug including Asynchronous Signal Recovery
  - Link Power Management
  - Native Command Queuing
  - Staggered Spin-up
  - Port Multiplier support
- **Support for SATA I and II data rates**
  - 1.5 & 3.0 Gbs
- **Implements SATA superset registers**
  - SError, SControl, SStatus
- **Interrupt driven**
- **Power management support**
- **Error handling and diagnostic features**
  - Far end/Near end loopback
  - Failed CRC error reporting
- **Support for eSATA**



- **Native Command Queuing (NCQ):** ability to issue multiple commands to the drive and to allow re-ordering

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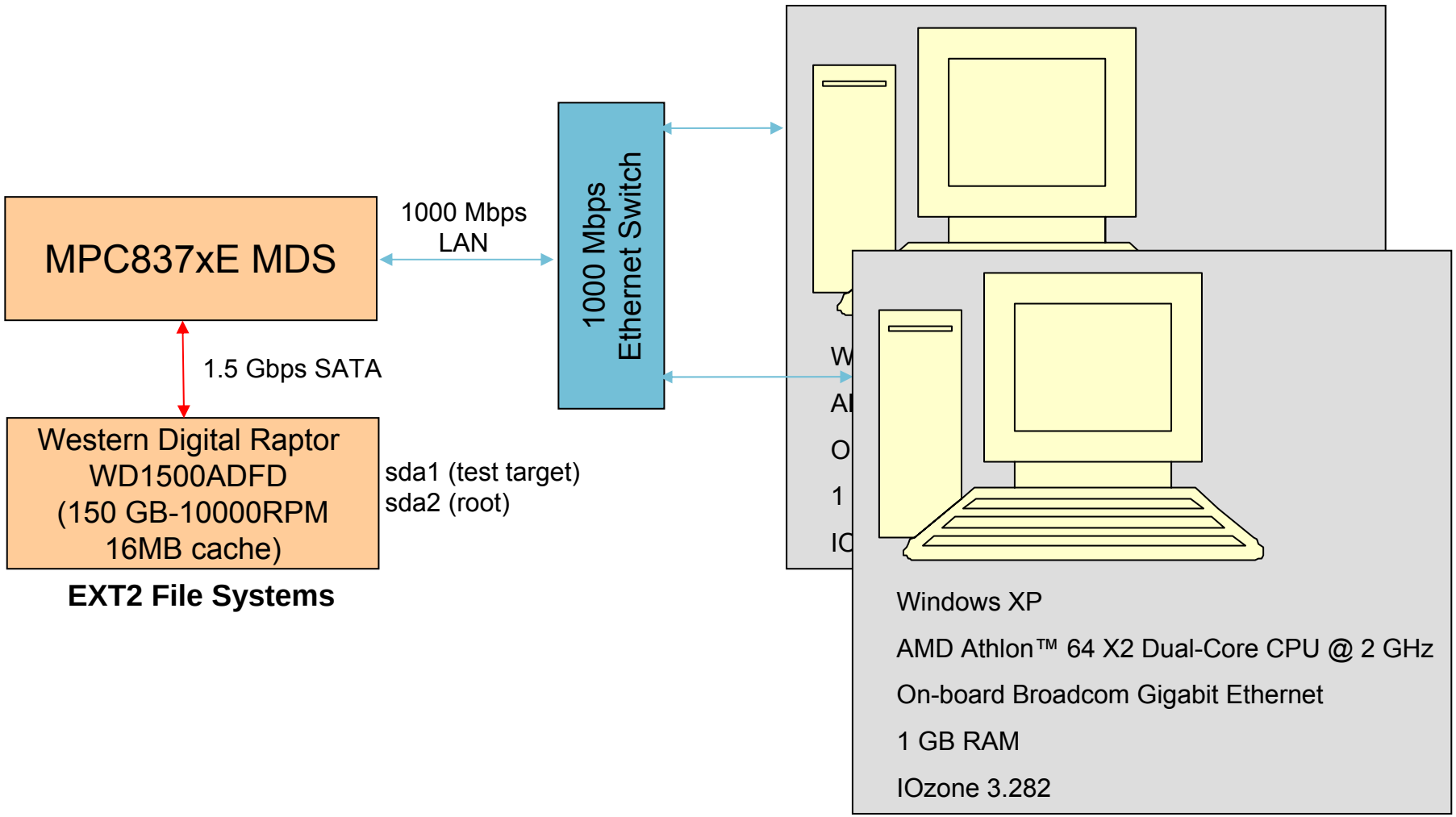
NAS Setup: Dual Client



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New IP Overview: PCI Express

MPC837x & MPC8315 New IP Overview

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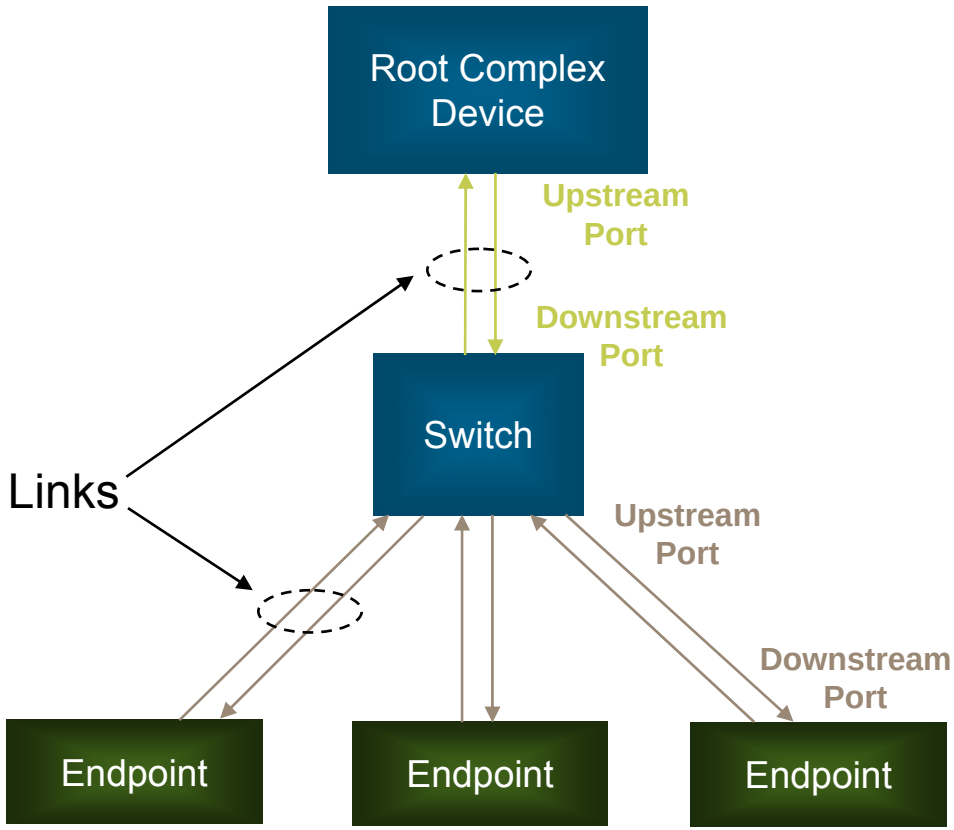
Features of PCI Express (General)

- Extension of PCI architecture
- Maintains software compatibility with PCI
- Packet based, load-store architecture
- Divided into 3 layers
  - Transaction (TL)
  - Data link (DL)
  - Physical (PL)
- Serial differential interface
- Scalable width: x1, x2, x4, x8, x12, x16, x32
- 2.5 Gbits/sec per lane
- Power management and hot plug/swap support
- QoS support (Traffic Class & Virtual Channels) on outbound packets
- Message transaction added
- Configuration address space extended from 256B to 4KB
- Improved error handling and data transfer robustness (ECRC, LCRC)

PCI Express® – System Topology



Root complex: connects CPU/memory to the I/O subsystem. Similar to host mode in PCI/X.

Switch: Connects root complex to end point or end point to end point.

End point: I/O devices or a bridge from PCI-Express to other bus. Similar to agent mode in PCI/X.

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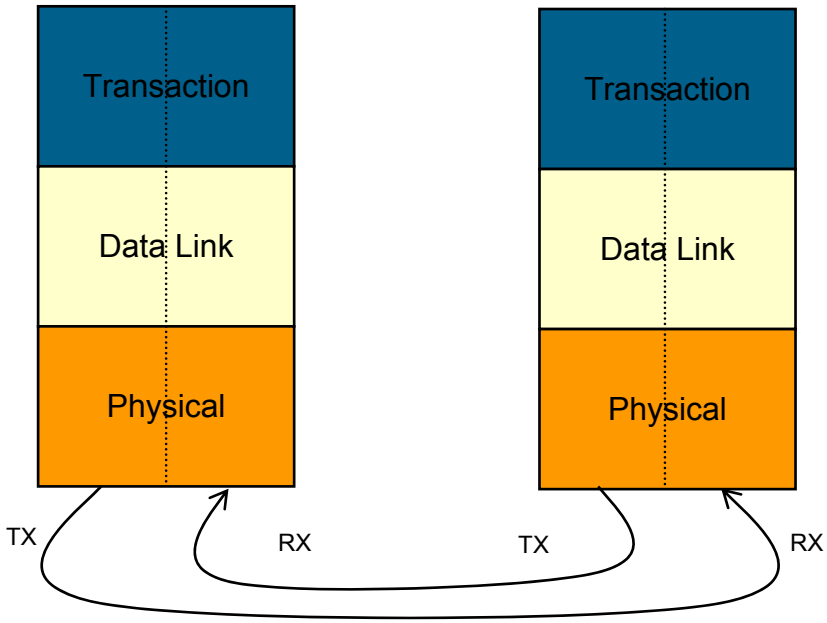
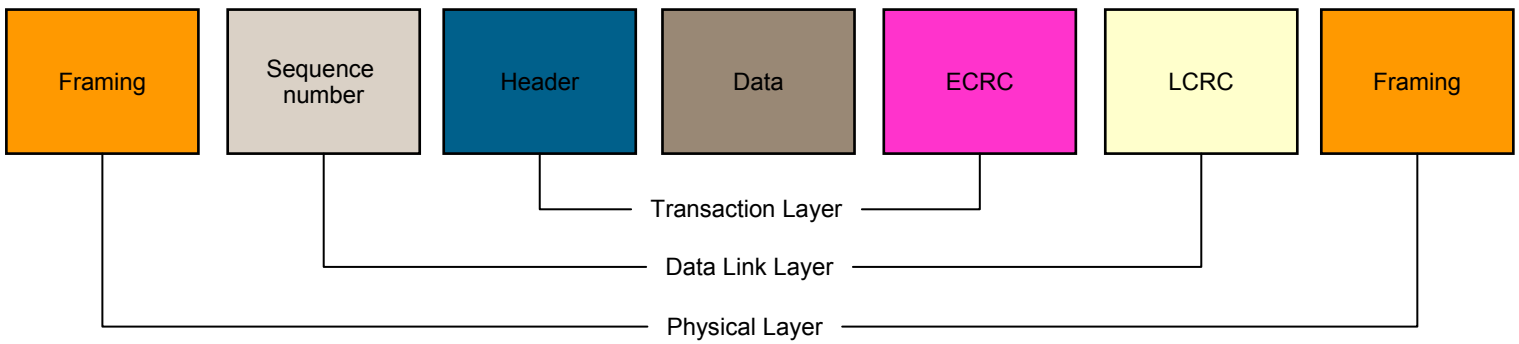
Layered Protocol Architecture



Packet Flow:



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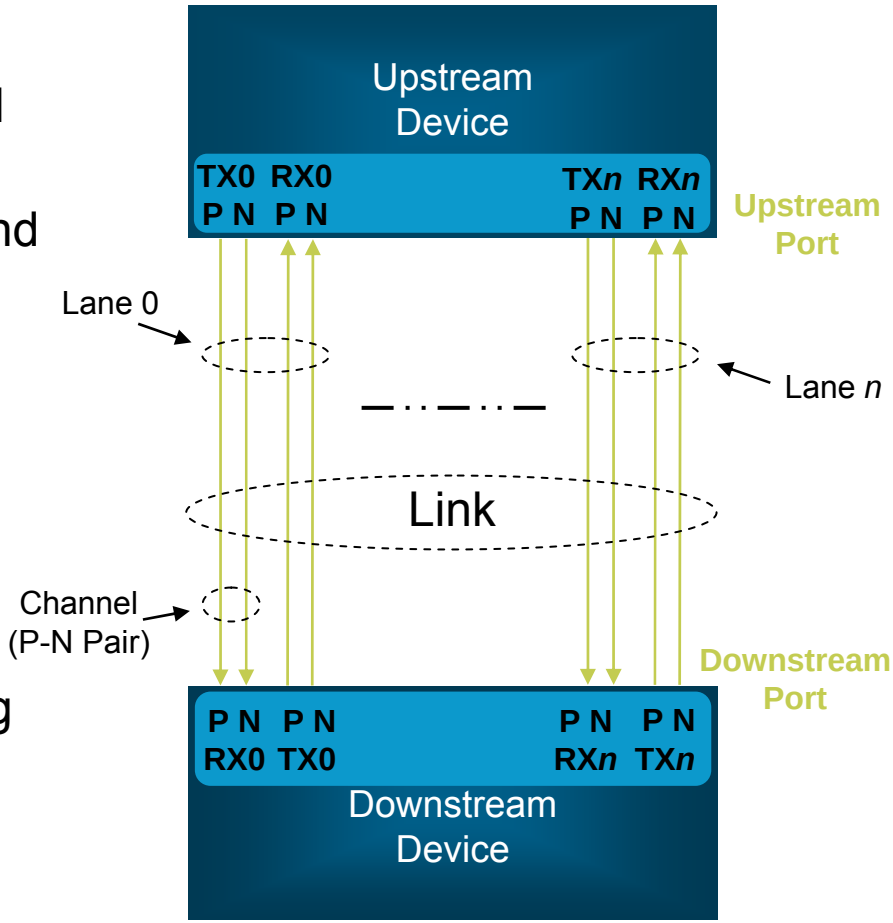
PCI Express – Link Topology & Electrical Overview

- Each Lane consists of an upstream and downstream channel
- Each Channel consists of one differential pair of signals
- High speed signaling extension to PCI and PCI-X
- Support for PCI-E 1.x: 2.5 Gb/s raw bit rate per lane (diff pair) / per direction
- Serial Interface on a dual simplex bus
- Point-to-point connections
- Differential (*LVDS*), AC coupled signaling
- Terminations built into devices
- Embedded clock in data stream (8b/10b Encoding)
- In-band sidebands (interrupts, resets …)



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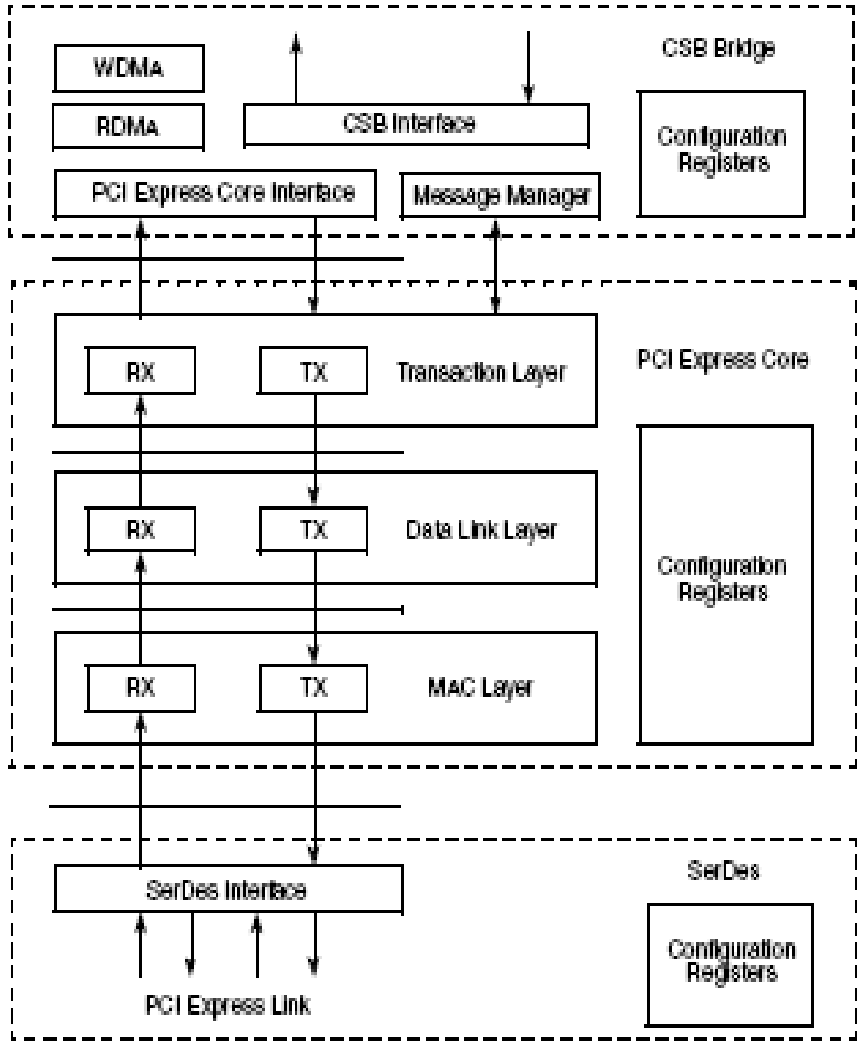
Data Link Layer & Transaction Layer

- Data Link Layer:
  - The Data link operation is user transparent
  - Ensures reliable delivery of packet across PCI Express link
  - Data integrity, error detection and management
  - Accepts power management request from TL and conveys power managed state to TL
  - Flow control initialization
  - Data Link Layer Packet (DLLP) for Link support

- Transaction Layer
  - Processes read/write requests from software
  - Split transaction protocol
  - 32-bit and 64-bit memory addressing
    - 32-bit uses 3 DW TLP Header
    - 64-bit uses 4 DW TLP Header
  - No Snoop, relaxed ordering attributes
  - 4 address spaces: memory, I/O, configuration and message
  - Optional 32-bit End-to-End CRC support

MPC837x/831x PCIE Specific Feature Set

- PCI Express 1.0a compatible
- MPC837x supports two x1 Links width or one x2 Link width
- MPC8315 supports two x1 Links width
- Independently supports RC (host) and/or EP (agent) modes per controller
- Access to all PCI-E memory space
- Access to I/O address spaces as requestor only in RC mode
- Support both 32- and 64-bit addressing
- 128-byte maximum payload size for memory read and write operations
- Internal WDMA and RDMA engines per controller



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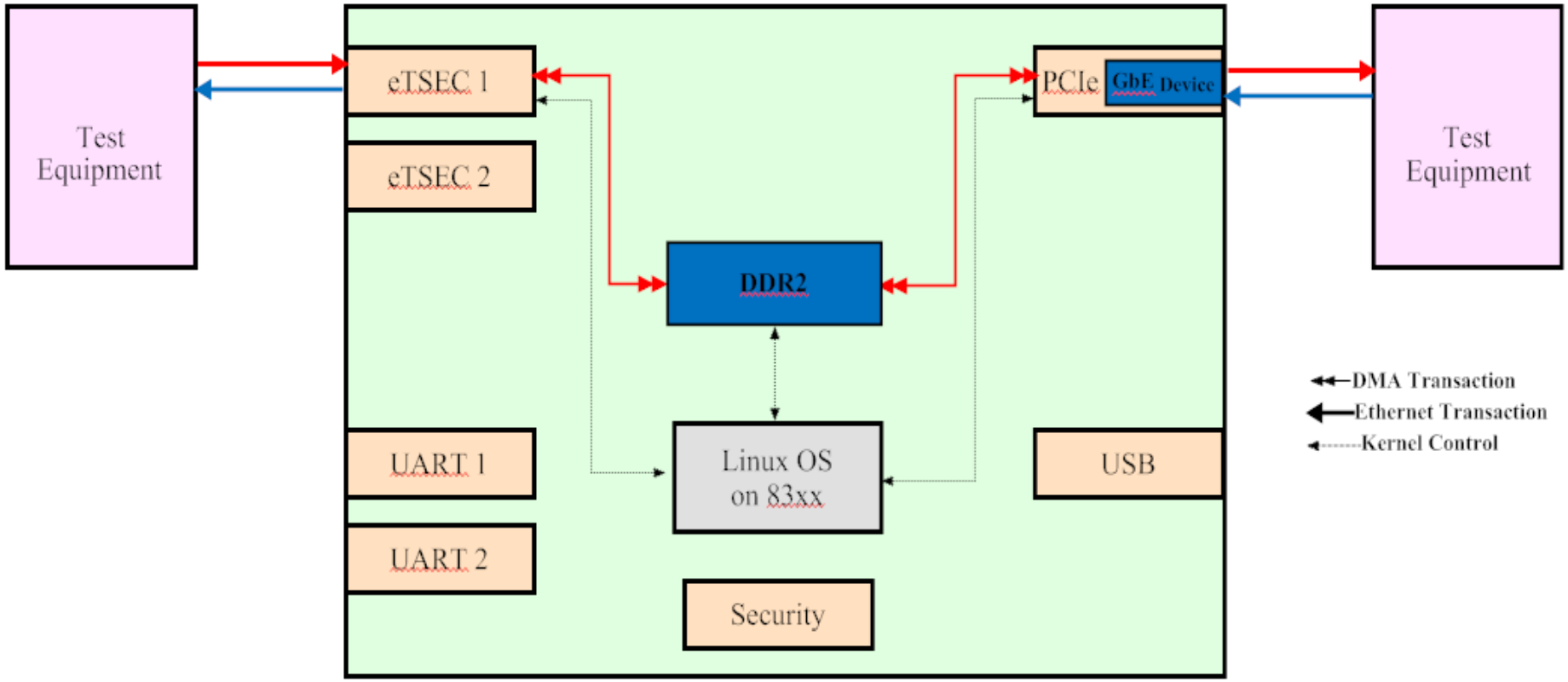
MPC837x/831x PCIE Specific Feature Set

- Configurable priority for WDMA/RDMA descriptor fetch, WDMA/RDMA data, Non-DMA data on CSB bus
- Supports maximum 32-byte payload transactions from CSB (including external DMA)
- Inbound and outbound ATMU support
- Inbound request support
  - 128-byte maximum payload size (MPS) for write requests
  - Up to 4kbyte read requests
- Outbound request support
  - Supports up to 4 outstanding PCIE transactions per each controller (Posted and Non-Posted)
  - 128 -byte maximum memory read request size (MRRS)
  - 128 -byte maximum memory write request size for WDMA (bigger packets requests are divided)
- Supports 4 general purpose windows (inbound and outbound) per controller (memory, cfg, io)

MPC837x/831x PCIE Specific Feature Set

- Auto-detection of link width, polarity inversion, and lane reversal
- Supports for MSI and virtual INTx generation
- Supports access to I/O address spaces as requestor in RC mode
- Interrupt generation and error detection
- Supports 1 traffic class as initiator and 8 traffic classes as completer
- Supports one virtual channel (VC0) per controller
- Supports strong and relaxed transaction ordering rules
- Supports operation in different modes of clock ratio between CSB clock and controller clock
- Power Management support
- Boot from PCIE is not supported

MPC837X eTSEC to PCIe 2 flow Setup



PCIe NIC used:
Intel e1000
Ethernet NIC

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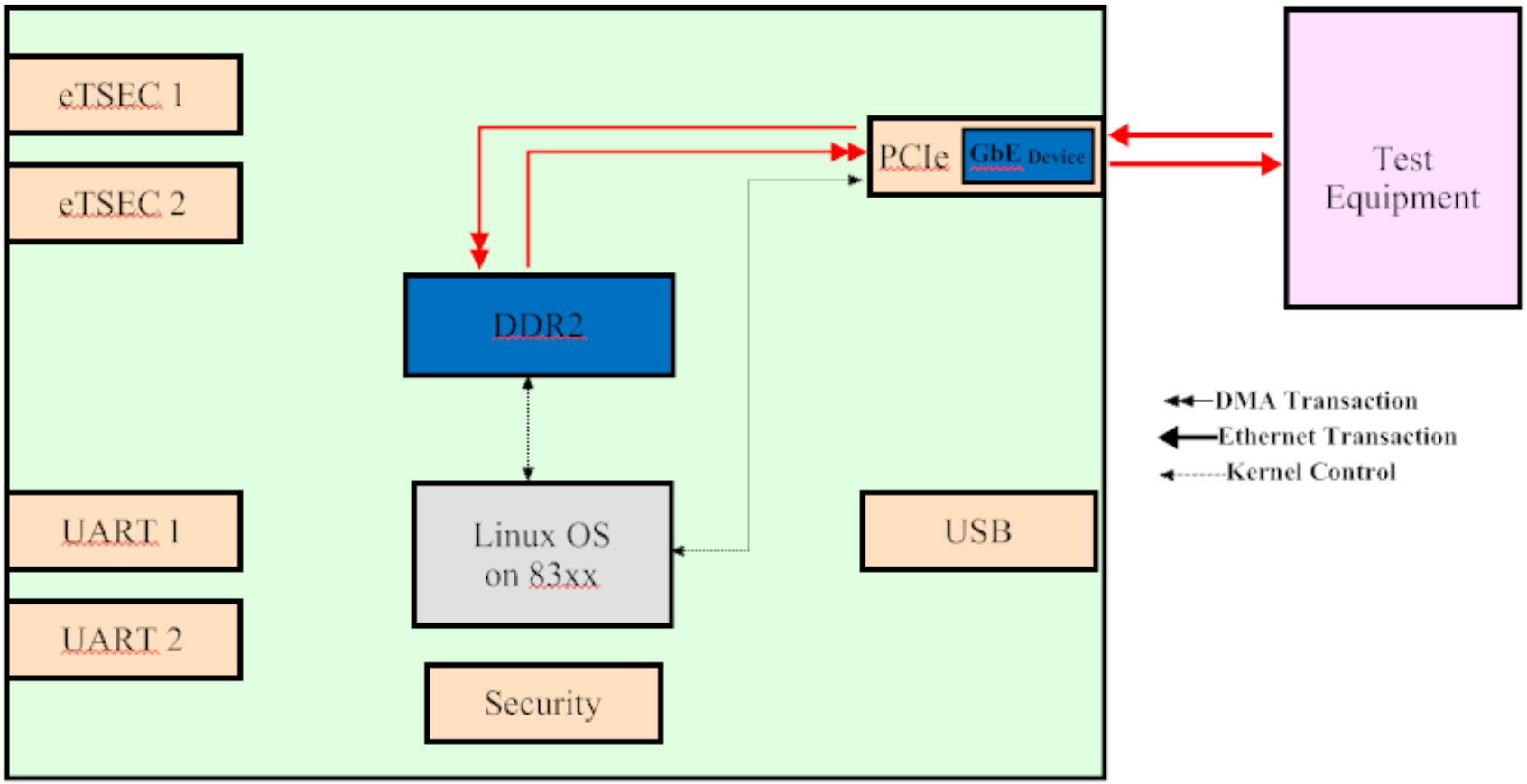
MPC837X PCIe loop back



PCIe NIC used:
Intel e1000
Ethernet NIC

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New IP Overview: eTSEC

MPC837x & MPC8315 New IP Overview

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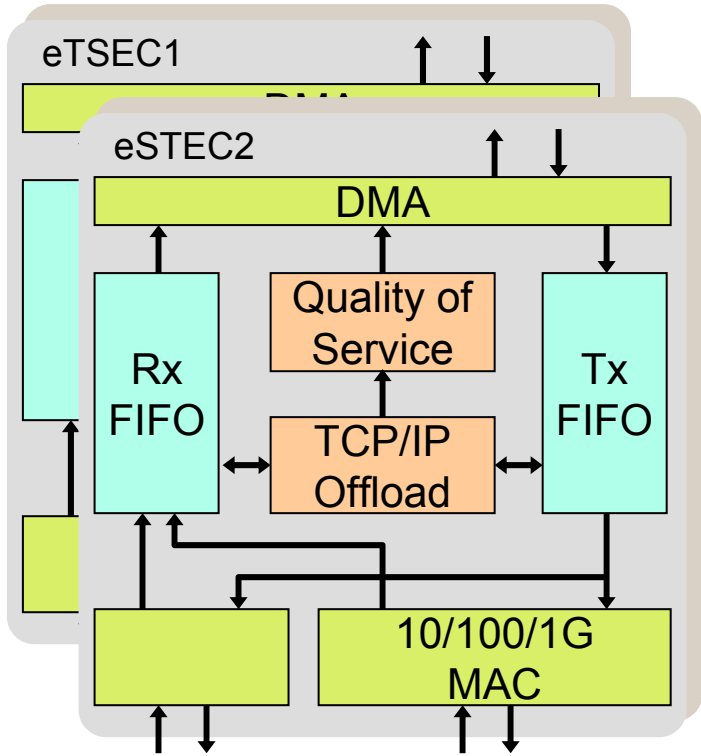
Enhanced Ethernet Controller (eTSEC)

- Enhanced Three-speed (10/100/1000) Ethernet controllers (eTSEC)
- Dual IEEE 802.3, 802.3u, 802.3x, 802.3z, 802.3ac compliant controllers
- MII, RMII, RGMII, SGMII and RTBI physical interfaces
- Full and half-duplex support (1000 Mbps only supports full duplex)
- IEEE 802.3x flow control mechanism
- Extended Programming Model Features
  - Supports Hash, Broadcast, and Multicast address recognition
  - Supports Promiscuous mode
- Jumbo frame support up to 9.6KB
- RMON statistics support
- MII management interface for control and status
- Programmable CRC generation and checking
- Interrupt coalescing for reducing core intervention



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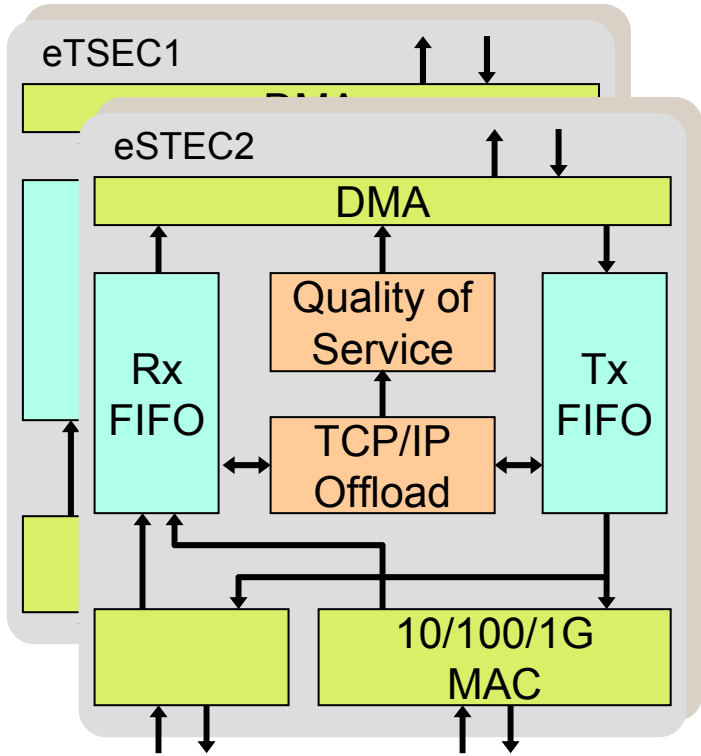
Enhanced Ethernet Controller (eTSEC)

- Support for IEEE1588”tm” (Production Rev.)
- Optimizes CPU performance on TCP/IP
  - TCP/IP checksum offload Rx + Tx
  - IPv6 support in H/W
- QoS support for 8 H/W queues (8 Rx + 8 Tx)
  - Customizable per-packet filtering/filing to 64 logical receive queues
  - 802.1p, IP TOS, Diffserv classification
  - Support for weighted fair queueing
  - TCP/UDP port-based flows
  - Assist firewall through IP/TCP/UDP reject
  - Ethernet preamble sorting and insertion
- Layer 2 features
  - VLAN insertion and deletion per frame
  - 16 exact-match MAC addresses



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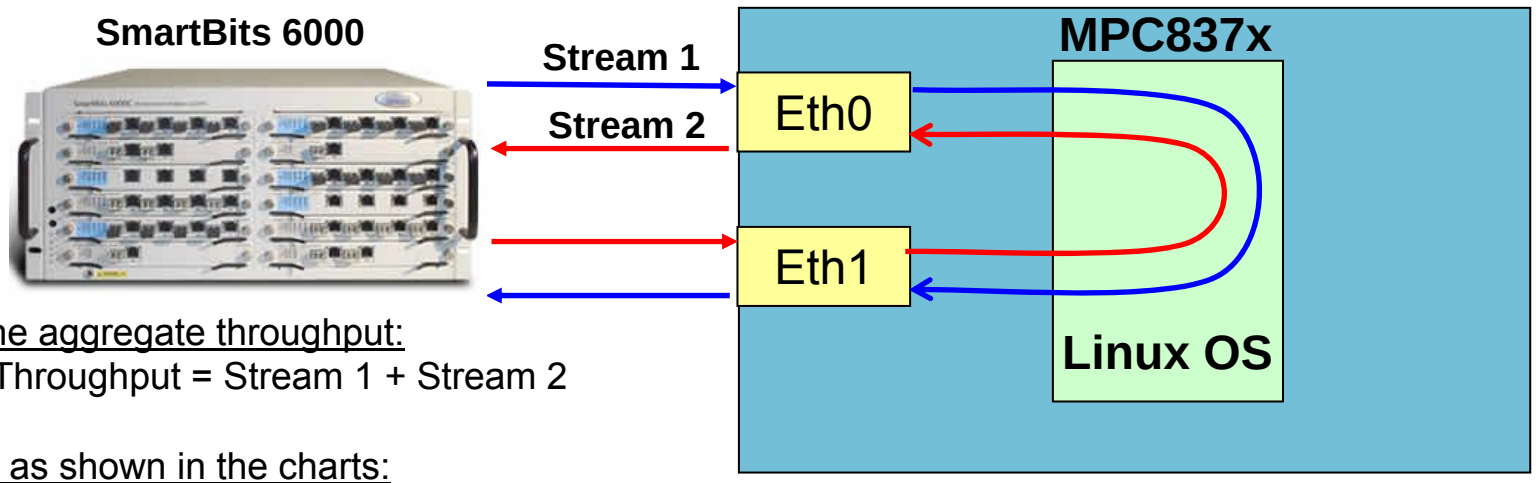
Throughput Measurement Defined

Throughput Definition

- Throughput is defined in RFC2544/1242 as the fastest rate at which the count of test frames transmitted by the DUT is equal to the number of test frames sent to it by the test equipment.
- For unidirectional (1 flow) data flows, the throughput is measured for a single path only. For bidirectional (2 flow) data flows, the throughput is measured on both paths as aggregate.



To determine aggregate throughput:
Aggregate Throughput = Stream 1 + Stream 2

Throughput as shown in the charts:
Measured Throughput = Stream 1 for unidirectional

Uni-directional (1 flow) = Stream 1
Bi-directional (2 flow) = Stream 1 + Stream 2

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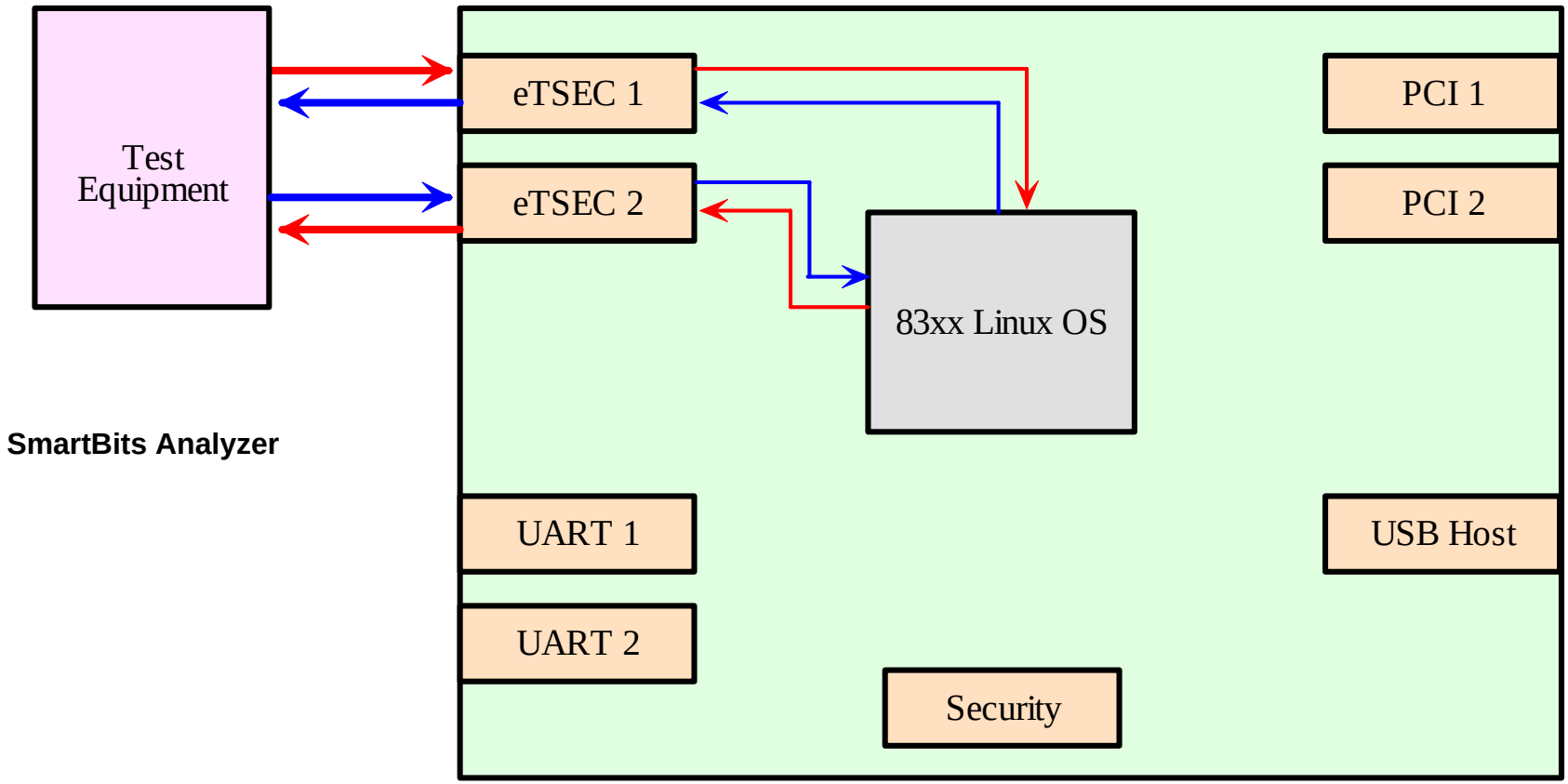
IPv4 Forwarding Results

- The purpose of the IPv4 Forwarding benchmarking is to demonstrate the typical Layer 3 based IPv4 forwarding throughput performance that can be achieved for various Ethernet frame sizes.
- The Linux OS configures the two eTSEC ports as interfaces on two separate and unique subnets, with separate and unique MAC and IP addresses for each eTSEC.
- All incoming traffic is routed to the appropriate subnet based upon the (Layer 3) IP Destination field contained within the incoming frame/packet.
- The incoming frame, if destined for the corresponding subnet, must have its Destination MAC address changed to reflect the MAC of the next hop, i.e., the test equipment. The Linux OS may learn of the next hop via static or automatic ARP entries to the ARP table. This means all frames must be inspected at the Layer 3 IP level and mangled at the Layer 2 MAC level.

IPv4 2 Flow Set Up



SmartBits Analyzer

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New IP Overview: Power Management, eLBC, eSDHC, TDM & SEC

MPC837x & MPC8315 New IP Overview

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Power Management Features

- The MPC837x device supports the following power saving modes:
  - Shutting down unused blocks, by S/W
  - Software-controlled power-down states
    - Doze, Nap and Sleep for the e300 Core
    - System idle with or without DDR disabled
  - *PCI Power Management Interface Specification in both host and agent modes*
  - *PCI Express Power Management events are not supported*

- The MPC8315E supports a range of power saving modes:
  - Split power planes to turn OFF unused blocks (core, eTSEC, USB etc.)
  - A new low-power standby power management state called D3warm
    - The PMC, one Ethernet port, and the GTM block remain powered via a split power supply controlled through an external power switch
    - Wake-up events include Ethernet (magic packet), GTM, GPIO, or IRQ inputs and cause the device to transition back to normal operation
  - Provides power management support for both PCI host and agent modes
  - PCI Power Management 1.2 D0, D1, D2, D3hot, and D3cold states
  - PME generation in PCI agent mode, PME detection in PCI host mode
  - Wake-up from Ethernet (magic packet), USB, GPIO, and PCI (PME input as host) while in the D1, D2 and D3hot states
  - PCI agent mode is not be supported in D3warm state
  - *PCI Express-based PME events are not supported*

MPC837x Power Spec

Core Frequency (MHZ)	CSB/DDR (MHz)	Typical App at 125C (W)	Max App at 125C (W)
400MHz	266MHz	3.3W	4.0W
500MHz	333Mhz	3.3W	3.9W
600MHz	400MHz	3.4W	4.1W
667MHz	333MHz	3.3W	4.1W

Note:
• The values do not include I/O supply power (OVDD, LVDD, GVDD) or AVDD. For IO power values, see Table 6 in HW Spec.
• Maximum power is based on a voltage of VDD = 1.0V, a junction temperature of Tj =125C, worst case process, and an artificial smoke test.
• Typical power is based on a voltage of VDD = 1.0V, a junction temperature of Tj=125C, and a Dhrystone benchmark application.

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MPC8315 Power Spec

Table 4. MPC8315E Power Dissipation[1] (Does not include I/O power dissipation)

Core Frequency (MHz)	CSB Frequency (MHz)	Typical [2, 3]	Maximum [2,3]	Unit
266	133	1.116	1.646	W
333	133	1.142	1.665	W
400	133	1.167	1.690	W

Note:

1. The values do not include I/O supply power, but do include core, AVDD, USB PLL, digital SerDes power, and SATA PHY power.
2. Typical power is based on a voltage of V_{dd} = 1.05V, a junction temperature of T_j = 105°C, and an artificial smoker test.
3. These are preliminary estimates

Enhanced Local Bus
(new features in Blue)

- Enhanced Local Bus Features (eLBC)
  - Multiplexed 32-bit address and data operating up to 167MHz for MPC837x
  - Non Multiplexed 25-bit address and 16-bit data for MPC837x.
  - Multiplexed 26-bit address and 8/16 data up to 66MHz for MPC8315/14
  - Eight chip selects support eight external slaves (Four Chip Selects for MPC8315/14)
  - Up to eight-beat burst transfers, with Parity support
  - 32-(muxed), 16-, and 8-bit port sizes are controlled by an on-chip memory controller
  - General purpose chip select machine (GPCM)
  - Three user programmable machines (UPM)
  - NAND Flash controller machine (FCM) with support for small and large page NAND Flash
  - Supports automatic, hardware-based single bit ECC.
  - Default boot ROM chip select, configurable bus width (8-, 16-, or 32-bit)
  - Enhanced Parallel boot options (see Boot Options Slide)
  - Used to interface to Memories (NOR, NAND), ASICs, FPGA, and other devices
  - Provides GPIO port expansion (ext. latch provides 32 GPIO pins per CS)

Enhanced Secure Digital Host Controller (eSDHC)
MPC837x Only

The eSDHC includes the following features:

- Conforms to SD Host Controller Standard Specification version 2.0 with test event register support
- Compatible with the MMC System Specification version 4.0
- Compatible with the SD Memory Card Specification version 2.0, and supports High Capacity SD memory cards
- Compatible with the SDIO Card Specification version 1.2
- Designed to work with SD Memory, miniSD Memory, SDIO, miniSDIO, SD Combo, MMC, MMC*plus*, and RS-MMC cards
- SD bus clock frequency up to 50 MHz
- Supports 1-/4-bit SD and SDIO modes, 1-/4-bit MMC modes
- Up to 200 Mbps data transfer for SD/SDIO/MMC cards using 4 parallel data lines

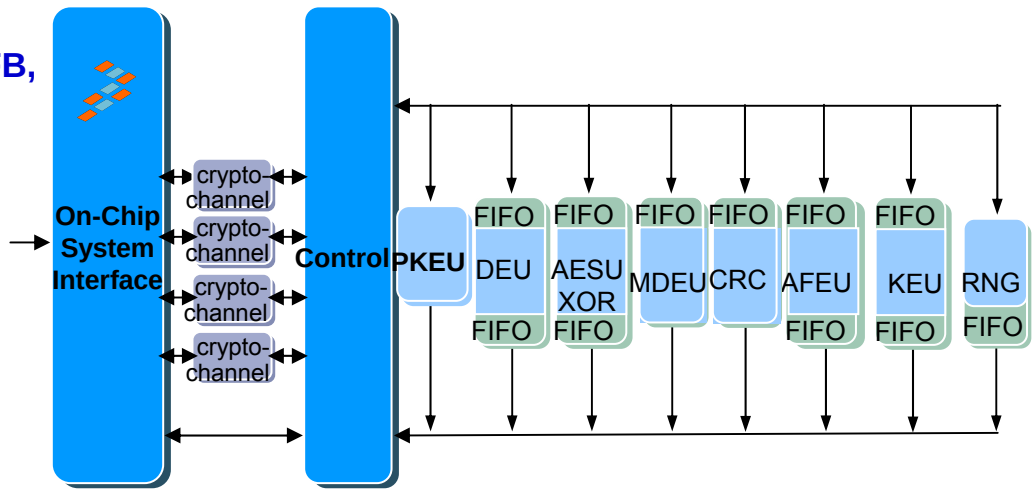
TDM (Time Division Multiplexing) Interface
MPC8315/14 Only

The TDM Interface includes the following features:

- Independent receive and transmit with dedicated data, clock and frame sync line
- Separate or shared RCK and TCK whose source can be either internal or external
- Glue-less interface to E1/T1 frames and MVIP, SCAS, and H.110 buses
- Up to 128 time slots, where each slot can be programmed to be active or inactive
- 8- or 16-bit word widths
- The TDM Transmitter Sync Signal (TFS), Transmitter Clock Signal (TCK) and Receiver Clock Signal (RCK) can be configured as either input or output
- Frame sync and data signals can be programmed to be sampled either on the rising edge or on the falling edge of the clock
- Frame sync can be programmed as active low or active high• Selectable delay (0-3 bits) between the Frame Sync signal and the beginning of the frame
- MSB or LSB first support

Freescale Security Engine – SEC 3.0
(new features in Blue)

- Public Key Execution Unit supports:
  - RSA and Diffie-Hellman (to **4096b**)
  - Elliptic curve cryptography (**1023b**)
- Data Encryption Standard Execution Unit
  - DES, 3DES (2K, 3K)
  - ECB, CBC, **OFB** modes
- Advanced Encryption Standard Unit
  - Key lengths of 128, 192, and 256b
  - ECB, CBC, CTR, CCM, **GCM, CMAC, OFB, CFB, and LRW**
- Message Digest Execution Unit
  - SHA-1 160-bit digest
  - SHA-2 256-bit digest
  - **SHA-384/512**
  - MD5 128-bit digest
  - HMAC with all algorithms
- ARC Four Execution Unit
  - Compatible with RC4 algorithm
- Kasumi Execution Unit (KEU)
  - F8 , F9 as required for 3GPP
  - A5/3 for GSM and EDGE
  - GEA-3 for GPRS
- **CRC Execution Unit**
  - **CRC32, CRC32C**
- XOR acceleration
- Random Number Generator
- **Multi-OS Friendly**



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Summary

▶The next generation PowerQUICC II Pro: MPC837x & MPC8315

- Key **integration** to reduce BOM cost and improve connectivity
- High performance e300 Power Architecture™ core up to 667MHz
- Targeted power management for low-power applications
- Scalable family targeted at consumer to Small/Medium business applications

Freescale powers management solutions by accessing, storing & streaming secure data and digital media content

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Related Session Resources

Session Location – Online Literature Library

http://www.freescale.com/webapp/sps/site/homepage.jsp?nodeId=052577903644CB

Sessions

Session ID	Title

Demos

Pedestal ID	Demo Title

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