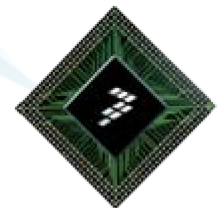
Freescale Technology Forum
Design Innovation.

Nov. 6, 2008

Quality/Zero Defect: Freescale Strategies, Measures and Tools

PA101



Peter Kang
China Automotive FAE Manager

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Freescale Quality Vision

Vision	It's ~~im~~possible. Zero = *Zero*
Mission	• Zero Defects for the Automotive Market • Safe Launch on New Product Introductions
Strategy	**Defects** • Containment • Analysis • Improvement **Spill Elimination** **Safe Launch** • New Technology Introduction • New Product Development • Technology and Product Transfers

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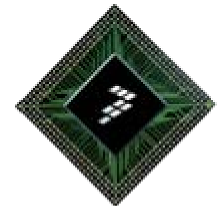
Looking Back on the Journey



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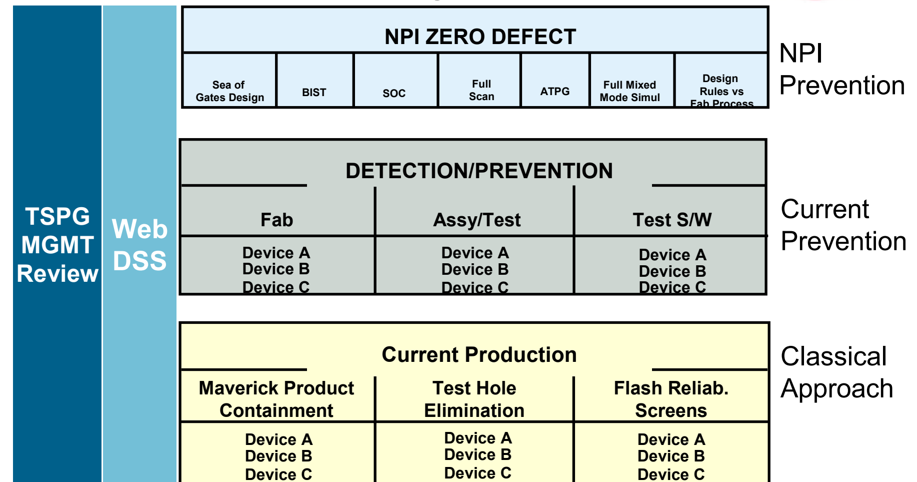
TSPG ZD: Management Frame Work



- In 2004/ 2005 we started the journey for Zero defects
- We set a management framework :
  - Classical: i.e, Containment and screens
  - Detection and Prevention
  - Focus on Zero Defect techniques for New Products
- We defined a set of ZD elements in the Manufacturing, Product and Test and Design
- These were constantly upgraded and carried forward as 'ZD base' for each new technology and product.
- In manufacturing we raised the bar successively

ZD Elements	
Product Zero Defect Program	JVT VCT/HVST Iddq Test Coverage (AEC Spec) Lessons learned Look Across Standardized NVM test methods Burn-In WebDSS CQI Entry
Manufacturing Zero Defect Program	PAT (Unit Probe) BMY SBL Phase1 SBL Phase 2
Division Specific Elements	PAT (Final Test) Gate Stress 100% Cold Test 100% Hot Test Inductive Load
Factory Driven	Continuos Improvement- Particle Continuos Improvement- Defect Density SPC- Process, Particles SPC- Class Probe SPC- Unit Probe ISTAB- Process, Particles ISTAB- Class Probe Problem Solving- 8D/ 5 Why's Problem Solving- FMEA Problem Solving- CAB Maverick Prevention- Lot Maverick Prevention- Wafer BMY Maverick Anamolous- Process, Particles Maverick Anamolous- Class Probe

	NPI ELEMENTS
Design	DFM(accuracy of device models for process) Design for Test Design for FA Full Chip STA vs Module Flash & SRAM ECC
Verification	Independent Verification Team Verification at module , platform , system level Random Pattern generation at Module level 100% RTL block & expression coverage Spec Tagging
Test	SRAM & Flash BIST Trace Matrix Full Chip AC & DC Scan >98% Stuck Fault coverage Code execution memory tests
Product	Reliability Lookahead(ESD/ NVM/ HTOL/TV) Burn-in Scan* & BIST Matrix CZ prior to launch & or 2nd tape out Failure Analysis Capability
	Smoke alarm / Volt storm Top level simulation - mixed signal
	Peer reviews
	Analog HVST (SOA, inductive load, gate stress, bvds:

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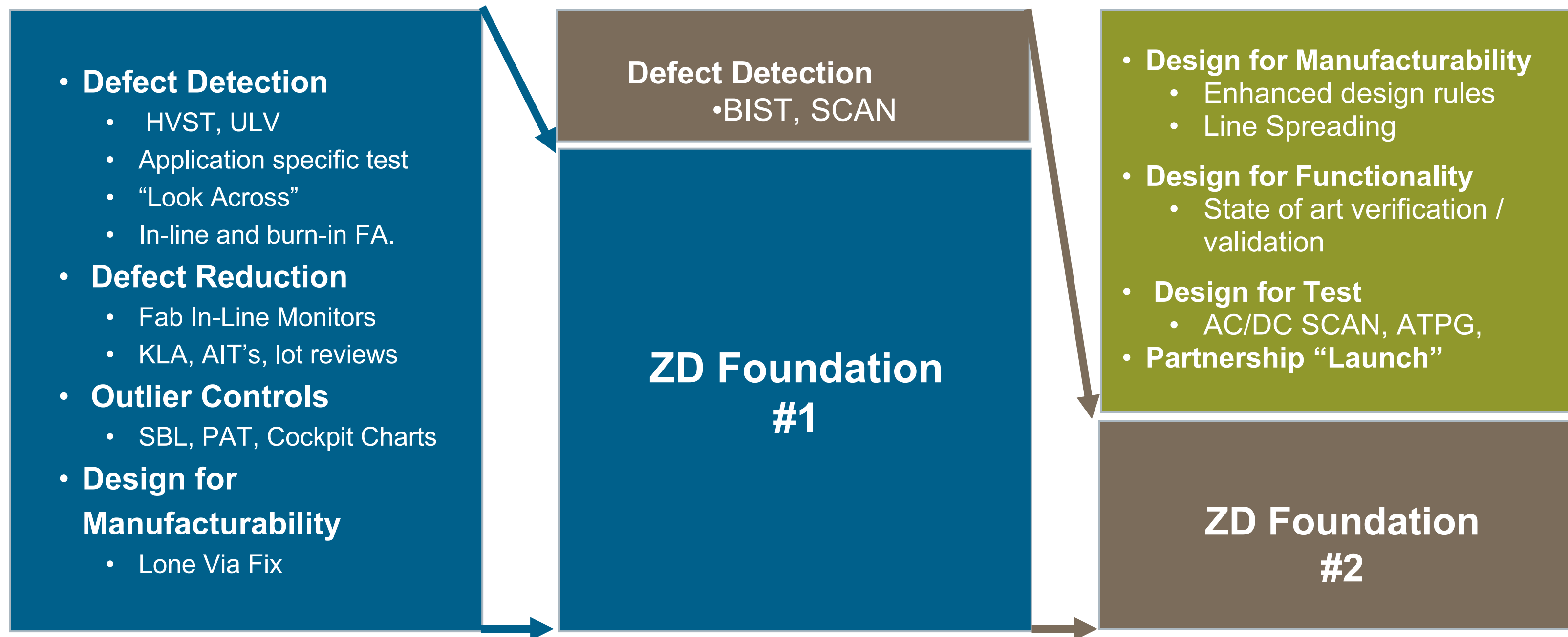
Freescale TSPG ZD Approach

▶ Institutionalize ZD elements as the foundation and add new learnings'



- Introduce 'Safe launch' process with the customer
- Continue to raise the ZD requirements every year for manufacturing

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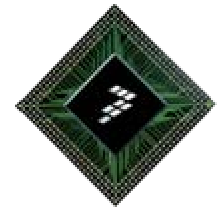
What is the ZD Methodology in Freescale?



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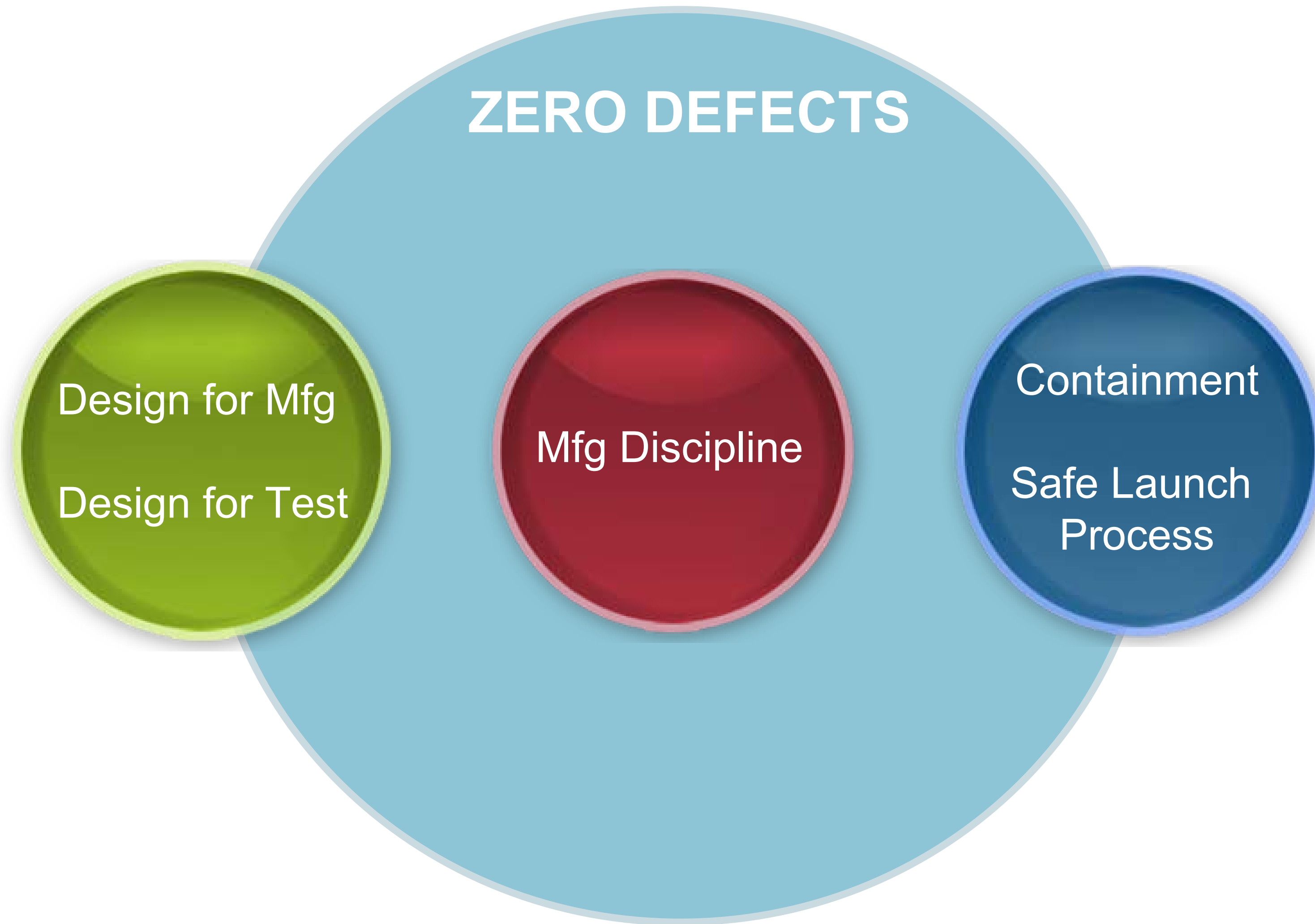
Freescale Zero Defects Methodology



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Design for Mfg

DFM in Freescale

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Design for Manufacturability Strategy

- **Freescale has invested substantially to advance DFM**
  - A dedicated group is assigned to develop and aggressively deploy advanced techniques to impact our products
- **Target quality throughout the design lifecycle**
  - Standard cells are scored and corrected. Newer cells must ensure that area / quality is maximized
  - SoC: Physical design flow is continuously updated to incorporate latest techniques nearly as transparently as possible
- **Continuously improve DTMS process**
  - DRC, DFM compliance are checked prior to tape-out
  - Due diligence checks are added to ensure corrective actions have been successful
- **Drive the “Designed for Reality’ initiative**
  - Close the gap between predicted and true product results

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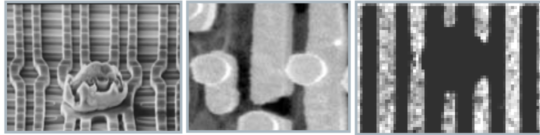
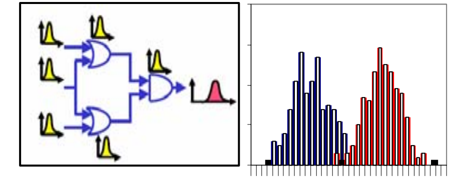
DFM Techniques

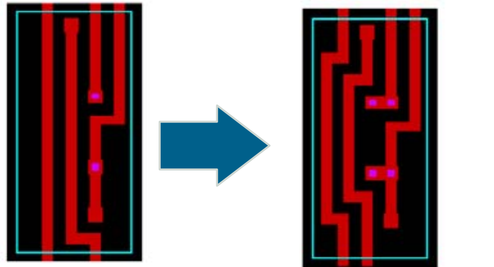


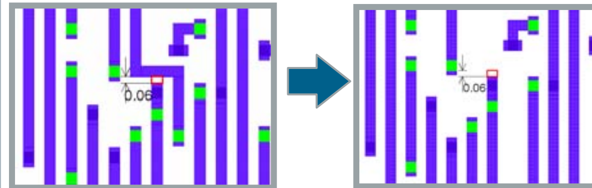
- Random particle induced opens & shorts
- Resistive vias & via opens due to copper cladding and litho process

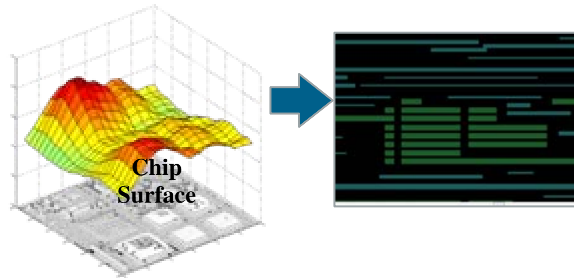
- Inability to print desired shapes due to physical limitations of the litho process
- Chemical & mechanical impacts of the mfg process on wafer/die planarity



- Occurrence of devices that fail to meet power and timing requirements







- Model based parasitic extraction
- Statistical static timing analysis and optimization
- More intelligent margining
- Variation robust design

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SoC DFM Methodology by Technology

Defect Class	DFM Technique		0.35um SMOS8, CDR3	0.18/0.25um 25SGF, LL18, HiP6WRF	0.13um HiP7, SMOS10	90nm LP/GP, NVM, RF, SOI	65nm LP/GP	45nm LP/GP, SOI
Random	Optimization	Via	**Recommend**	**Required**	**Required**	**Required**	**Required**	**Required**
		Wire			**Required**	**Required**	**Required**	**Required**
		Synthesis for yield				**Recommend**	**Recommend**	**Recommend**
Systematic	Timing Aware Tiling (Metal Fill)					**Recommend**	**Recommend**	**Recommend**
	Model Based Lithography and CMP						**Required**	**Required**
Parametric	Variation Tolerant Design	SSTA						**Pilot**
		Model based extraction						**Pilot**

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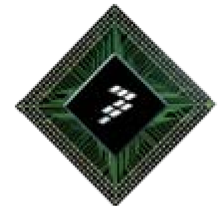

Design-for-Test

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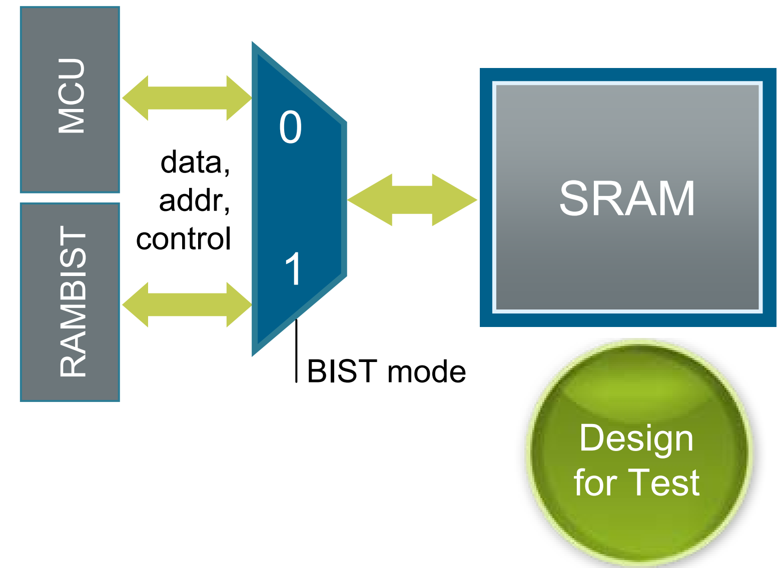
Test Methodologies

▶ Digital Logic

- Scan is dominant test method with SA fault coverage goal of >99%
  - Scan test through I/O pads increases die area covered and through RAM increases coverage in RAM surrounding logic
  - Inter clock domain scan increases transition fault coverage
  - On-chip decompression / compression logic enables high parallel test and test pattern increase required for advanced fault models.
- Functional test patterns on top of scan
  - Test basic functionality on module basis
  - Covers what scan missed
- Defect based tests IDDq, HVST
  - Pseudo stuck at fault coverage



▶ SRAM and ROMs

- Memory BIST implemented for all SRAM and SDPRAM hard macros.
- Test Algorithms cover applicable Fault Models in SRAMs and SDPRAMs:

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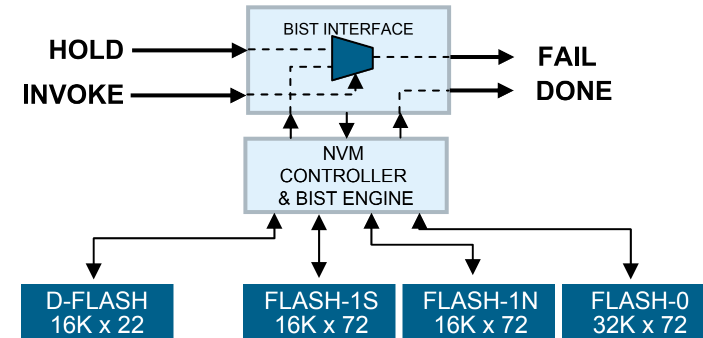
Test Methodologies

▶ NVMBIST for Non-Volatile Memories

- Flexible, embedded test of NVM controlled via a dedicated test interface
  - Next generation NVM BIST engine combines hard coded algorithm elements on chip in combination with pattern selectable features
  - BIST serial scan chain loaded / unloaded via the 4 pin interface
- Benefits
  - Highly parallel NVM test at Sort-1 (x16 already).
  - Test all P-Flash and D-Flash blocks on a die in parallel.
  - Provides means for easy test standardization/control



▶ Analog

- Approach
- Test specification derived from electrical specification, test guide, and module characterization results
- Functional patterns/functional tests development according to test development process
- Test Quality
- Fault coverage achieved through functional coverage of tests

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Design for Test

DFT Maturity Matrix–Clear standard for Design-for-Test

DFT Maturity	Level 0	Level 1	Level 2	Level 3	Level 4	Level 5
Digital	• Ext. generated functional	• SAF > 90%	• SAF > 95%	• SAF > 98% • Transition >85% • Path Delay >= 200 out of 1000 most critical	• Transition > 90% • SAF > 99%	• SAF > 99.5% • Transition > 95% • Bridge > 70% • 70% SI CFs • Massively parallel test enabler (UTI like)
Analog (ADC, DAC, PLL, Oscillators)	• Ext. generated functional	• Partial Scan Wrapper	• Full Scan Wrapper (DC) • Ad-hoc analog test modes (based on designer intuition)	• Additional signals to increase analog testability • DC scan stuck-at > 95%	• Appropriate level of critical test points and test modes with Appropriate level of Analog BIST • AC Scan Wrapper	• Quantifiable boundary coverage > 99% • 100% SAF & 95%Transition testing of logic • Structural test of analog • Full Analog BIST
SRAM	• Externally generated	• Large Array MBIST generated • March C- or PMOVI algorithm	• Data Retention support • Checkerboard & Inverse tests • Different data backgrounds run on the March	• All RAMs BIST tested with same BIST type • BIST March LR/LA better • BIST X/Y fast addressing • BIST Bit Mapping • SCAN write through	• Sep BIST for DP RAMS • BIST Intra-Word Coverage • BIST Any-bit-fast tests • Cell Stability Test • Cell Stress Test • BIST paths >= Func paths.	• Programmable BIST capable of running up to 40+ N March tests • In the Field BISR
ROM	• Externally generated	• MBIST tested • 100% SAF	• 100% AF (inc and dec addressing)	• BIST X/Y fast addressing • MBIST Bit Mapping Support • Scan read support • BIST MISR Aliasing probability < 1PPM (>= 20-bit MISR)	• BIST Any-bit-fast tests • BIST paths >= Functional paths. • BIST MISR Aliasing probability < 0.1PPM (>=24-bit MISR)	
NVM, Flash	• Ext. generated functional based • User modes only	• Array Test Modes	• Basic BIST supported by State Machine • Independent erasable test row	• Configurable BIST • DC Scan logic > 98% • Massively parallel test enabler (UTI or BDM based) • MBIST Bit Mapping Support	• Code Execution BIST that detects Address Decode SOF and Address Coupling Faults • BIST paths >= Functional paths • DC Scan logic part > 99%	• BIST include decode error detection • 100% testpoints or BISTs of embedded analog • Scan read support
I/O	• Ad hoc, functionally generated	• Most I/Os controllable via register	• Full control* of all pads I/O state (jtag or registers)	• Full control* of all pad electricals • High speed IO 2^^7-1 random sequence for BER (PRBS loopback to PRSA):	• All pad electrical controls observable via ATPG scan	• I/O DFT/BIST
Parametric, IDDQ, HVST, Burn-in, Voltage Margin, JVT Support	• No DFT support for IDDQ, High Voltage Stress, Burn in, Voltage Margin, Low Frequency and JVT	• Power down mode for IDDQ	• Limited / Partial support • MBIST used for Burn IN	• Scan based ATPG for IDDq • Burn In Mode covering Memories and partial scan • PLL Bypass for low frequency	• DFT techniques to enable HVT and voltage margin test for designs including level shifters • Burn In Mode covering 100% memories and scan	• Self monitoring Burn In • Burn-in Self Test

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Design For Test – Continuous Improvement

Oaks→S12→S12X → S12Xe → MPC5500 → next Gen @ 90nm

Spanish Oak DFT Maturity

S12 DFT Maturity

S12X DFT Maturity

S12Xe DFT Maturity

Copperhead DFT Maturity

Viper DFT Maturity Matrix

DFT Maturity	Level 0	Level 1	Level 2 (L1 +)	Level 3 (L2 +)	Level 4 (L3 +)	Level 5 (L4 +)
Digital	• Ext. generated functional	• DC Scan (TC > 90%)	• DC scan (TC > 95%)	• AC scan (TC > 70%)	• AC scan (> 80%), • DC (> 98%)	• AC scan (> 85%), • DC (> 99%) • Massively parallel test enabler (UTI like)
Analog (ADC, DAC, PLL, Oscillators)	Ext. generated functional	• Partial Scan Wrapper	• Full Scan Wrapper (DC) • Ad-hoc analog test modes .	• Additional signals to increase analog testability • DC scan stuck-at> 95% • AC Scan Wrapper	• Partial Analog BIST complemented by test points or exhaustive test points / testbench	• Full Analog BIST
SRAM	• Externally generated	• Large Array MBIST generated • March C- or PMOVI algorithm	• Data Retention support • Checkerboard & Inverse tests • Different data backgrounds run on the March	• All RAMs BIST tested with same BIST type •March LR, LA, or better • X-test option • BIST Bit Mapping support • SCAN write through	• Intra-Word March tests • Any-bit-tas tests • SDD Support • UWSH support • BIST paths >= Functional paths.	• Programmable BIST capable of running up to 40+ N March tests
NVM, Flash	• Ext. generated functional based • User modes only	•Array Test Modes	• Basic BIST supported by State Machine • Independent erasable test row	• Configurable BIST • DC Scan of logic part> 90% • Massively parallel test enabler (UTI or BDM based) • MBIST Bit Mapping Support	•Code Execution BIST that detects Address Decode SOF and Address Coupling Faults • BIST paths >= Functional paths • DC Scan of logic part> 98% • Scan read support	• BIST include decode error detection • 100% testpoints or BISTs of embedded analog
I/O	• Ad hoc, functionally generated	• Most I/Os controllable via register	• Full control of all pads I/O state (jtag or registers)	•Full control of all pad electricals	• All pad electrical controls observable via ATPG scan	• I/O DFT/BIST
Parametric, IDDQ, HVST, Burn-in, Voltage Margin, JVT Support	• No DFT support for IDDQ, High Voltage Stress, Burn In, Voltage Margin, Low Frequency and JVT	• Power down mode for IDDQ	• Limited / Partial support MBIST used for Burn IN	• Scan based ATPG for IDDq • Burn In Mode covering Memories and partial scan • PLL Bypass for low frequency	• DFT techniques to enable HVT and voltage margin test for designs including level shifters • Burn In Mode covering 100% memories and scan	• Self monitoring Burn In • Burn-In Self Test

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Planned DFT Maturity for New NPIs

DFT Maturity	Level 0	Level 1	Level 2	Level 3	Level 4
Digital	• Ext. generated functional	• SAF > 90%	• SAF > 95%	• Transition >85% • Path Delay >= 200 out of 1000 most critical	• Transition > 90% • SAF > 99% • Bridge > 80% • Small-delay defect coverage • Selective path-delay testing
Analog (ADC, DAC,PLL, Oscillators)	• Ext. generated functional	• Partial Scan Wrapper	• Full Scan Wrapper (DC) • Ad-hoc analog test modes (based on designer intuition)	• Additional signals to increase analog testability • DC scan stuck-at > 95% • AC Scan Wrapper if module running near Fsys.	• Partial Analog BIST and/or critical test points (tool determined test points)
SRAM	• Externally generated	• Large Array MBIST generated • March C- or PMOVI algorithm	• Data Retention support • Checkerboard & Inverse tests • Different data backgrounds run on the March	• All RAMs BIST tested with same BIST type • BIST March LR/LA better • BIST X/Y fast addressing • BIST Bit Mapping • SCAN write through	• Programmable BIST based on 14N coverage • Sep BIST for DP RAMS • BIST Intra-Word Coverage • BIST Any-bit-fast tests • SDD BIST Support ** • LWSH BIST support ** • BIST paths >= Func paths. • ** - Only required if RAM has test mode
NVM, Flash	• Ext. generated functional based • User modes only	• Array Test Modes	• Basic BIST supported by State Machine • Independent erasable test row	• Configurable BIST • DC Scan logic > 98% • Massively parallel test enabler (UTI or BDM based) • MBIST Bit Mapping Support	• Code Execution BIST that detects Address Decode SOF and Address Coupling Faults • BIST paths >= Functional paths • DC Scan logic part > 99% • Transition delay on logic > 85%
I/O	• Ad hoc, functionally generated	• Most I/Os controllable via register	• Full control* of all pads I/O state (jtag or registers)	• Full control* of all pad electricals	• All pad electrical controls observable via ATPG scan
Parametric, IDDQ, HVST,Burn-in, Voltage Margin, JVT Support	• No DFT support for IDDQ, High Voltage Stress, Burn in, Voltage Margin, Low Frequency and JVT	• Power down mode for IDDQ	• Limited / Partial support • MBIST used for Burn IN	• Scan based ATPG for IDDq • Burn In Mode covering Memories and partial scan • PLL Bypass for low frequency	• DFT techniques to enable HVT and voltage margin test for designs including level shifters • Burn In Mode covering 100% memories and scan

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Ongoing

- FSL uses best-in-class Design-for-Test technology, test engineering processes to proactively enable Zero Defect Quality for NPIs.
- Statistical analysis through volume diagnosis ensures efficiency of institutionalized methods and enables further improvements through 'lessons learned'.
- FSL working with leading EDA vendors and universities and investing in research for new DFT technology:
  - New Fault Models to better model silicon defects:
    - Bridging Fault Model (statistical and layout based)
    - Timing Aware ATPG - Small Delay Defects
    - Opens Defects
  - New DFT architectures:
    - Field Programmable BIST for SRAMs
    - Core Self Test for Safety Critical applications
- New technology is integrated into DFT Maturity Matrix as standard best practice and rolled out world wide.

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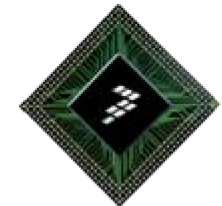
Mfg Discipline

Containment

Safe Launch Process

Manufacturing & Continuous Improvement



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Zero Defects Methods in Manufacturing

- Manufacturing uses a structured approach to institutionalize zero defect elements
- Die and Final Manufacturing SPC programs and specification limits identify rogue product & processes
- Specification limits are used as the gauge to determine if product is fit for use.
- Capability (CpK) studies are performed monthly on various inline process and class probe parameters
- Advanced Intelligent Manufacturing techniques such 'input controls' and Fault Detection Control are being deployed

ZD Elements	
Product Zero Defect Program	JVT VCT/HVST Iddq Test Coverage (AEC Spec) Lessons learned Look Across Standardized NVM test methods Burn-In WebDSS CQI Entry
Manufacturing Zero Defect Program	PAT (Unit Probe) BMY SBL Phase1 SBL Phase 2
Division Specific Elements	PAT (Final Test) Gate Stress 100% Cold Test 100% Hot Test Inductive Load
Factory Driven	Continuos Improvement- Particle Continuos Improvement- Defect Density SPC- Process, Particles SPC- Class Probe SPC- Unit Probe ISTAB- Process, Particles ISTAB- Class Probe Problem Solving- 8D/ 5 Why's Problem Solving- FMEA Problem Solving- CAB Maverick Prevention- Lot Maverick Prevention- Wafer BMY Maverick Anamolous- Process, Particles Maverick Anamolous- Class Probe

Containment

Safe Launch Process

Mfg Discipline

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Zero Defects: Continuous Improvement

"WAFER FAB PROGRAMS"

WAFER FABS	Location	Continuous Improvement: Particle	Continuous Improvement: Defect Density	Continuous Improvement: CQI	Excursion Prevention – Statistical Tools – SPC: Process	SPC: Particles	SPC: Class Probe	SPC: Unit Probe	ISTAB: Process	ISTAB: Particles	ISTAB: Class Probe	Data Analysis: Dashboard / ANOVA	Data Analysis: SODA / Others	Problem Solving: FMEA	Problem Solving: 8D	Problem Solving: CAB	Prevention – "Maverick" – BMY: Lot	BMY: Wafer	"Anomalous": Process	"Anomalous": Particles	"Anomalous": Class Probe	"Anomalous": Unit Probe (SBA)	"Anomalous": PAT (Unit Probe)
MOS9	EKB, Scotland	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES
MOS11	Austin, TX	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	Q2 '04	Q2 '04
MOS12	Chandler, AZ	YES	YES	YES	YES	YES	Q4 '03	Q4 '03	YES	YES	YES	YES	Q1 '04	Q4 '03	Q4 '03	YES	YES	YES	YES	YES	YES	Q4 '03	Q4 '03
MOS13	Austin, TX	YES	YES	YES	YES	YES	Q1 '04	Q4 '03	YES	YES	Q1 '04	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	Q4 '03	Q1 '04
MOS20	Tolouse, France	YES	YES	YES	YES	YES	YES	YES	YES	YES	Q4 '03	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	Q4 '03	YES
TSC6	Sendai, Japan	YES	YES	YES	Q2 '04	Q2 '04	Q2 '04	Q2 '04	Q2 '04	Q2 '04	Q2 '04	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	Q4 '03	Q2 '04
TSMC	Hsinchu, Taiwan	YES	YES	YES	YES	YES	YES	YES	Q4 '03	Q4 '03	Q4 '03	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	Q4 '03	YES

Achieved 1st baseline ZD Criteria

"WAFER FAB PROGRAMS"

WAFER FABS	Location	Continuous Improvement: Particle	Defect Density	5S	CQI	Excursion Prevention – Statistical Tools – SPC: Process	SPC: Particles	SPC: Class Probe	ISTAB: Process	ISTAB: Particles	ISTAB: Class Probe	Data Analysis: Dashboard / ANOVA	Data Analysis: SODA / Others	Problem Solving & prev: FMEA	DRA/PRA /detection matrix	8D	CAB	Prevention – "Maverick" – BMY: Lot	BMY: Wafer	"Anomalous": Process	"Anomalous": Particles	"Anomalous": Unit Probe (SBA)	"Anomalous": PAT (Unit Probe)	Advance Outlier Techniques	Collaboration – FMO: Sharing of BKMs'	FMO: Burn-In	PFO: Test Program Release	PFO: Test Coverage	PFO: DFM	Last Update
MOS9	EKB, Scotland				YES				YES	YES	YES	YES	YES	YES		YES	YES	YES	YES											WW04 2004
MOS11	Austin, TX				YES				YES	YES	YES	YES	YES	YES		YES	YES	YES	YES			Q2 '04	Q2 '04							WW04 2004
MOS12	Chandler, AZ				YES				YES	YES	YES	YES	Q1 '04	YES		Q4 '03	YES	YES	YES			Q4 '03								WW04 2004
MOS13	Austin, TX				YES				YES	YES	Q1 '04	YES	YES	YES		YES	YES	YES	YES				Q1 '04							WW04 2004
MOS20	Tolouse, France				YES				YES	YES	YES	YES	YES	YES		YES	YES	YES	YES			Q2 '04								WW04 2004
TSC6	Sendai, Japan				YES	Q2 '04	Q2 '04		Q2 '04	Q2 '04	Q2 '04	YES	YES	YES		YES	YES	YES	YES			Q2 '04								WW04 2004
CS1 **	Tempe Az																													
TSMC	Hsinchu, Taiwan				YES				YES	YES	YES	YES	YES	YES		YES	YES	YES	YES			Q2 '04								

Institutionalized
Actions Identified for missing elements required to meet ZD challenge
Actions identified for all elements required to meet ZD challenge

= Maintenance Items from Phase 2 activity

Raised the bar – added requirements

"WAFER FAB PROGRAMS"

WAFER FABS	Location	Continuous Improvement: Particle	Defect Density	5S	CQI	Excursion Prevention – Statistical Tools – SPC: Process	SPC: Particles	SPC: Class Probe	ISTAB: Process	ISTAB: Particles	ISTAB: Class Probe	Data Analysis: Dashboard / ANOVA	Data Analysis: SODA / Others	Problem Solving & prev: FMEA	DRA/PRA /detection matrix	8D	CAB	Prevention – "Maverick" – BMY: Lot	BMY: Wafer	"Anomalous": Process	"Anomalous": Particles	"Anomalous": Unit Probe (SBA)	"Anomalous": PAT (Unit Probe)	Advance Outlier Techniques	Collaboration – FMO: Sharing of BKMs'	FMO: Burn-In	PFO: Test Program Release	PFO: Test Coverage	PFO: DFM
MOS9	EKB, Scotland	Jun	YES	YES	YES	Jun	Jun	Jun	YES	YES	YES	YES	YES	YES		YES	YES	YES	YES	YES	YES	Dec	Dec				YES		
MOS11	Austin, TX				YES	Jun	Jan	Jun	Jun	Jun	Jun	Jun	Jun			Jun	YES	YES	YES										
MOS12	Chandler, AZ	YES	YES	YES	YES	Jun	Jun	TBD	Mar	Mar	YES	YES	YES	Jul		YES	YES	YES	YES	Jun	Jun	Dec	Dec	Dec		YES			YES
MOS13	Austin, TX	Jun	YES	Dec	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES		YES	YES	YES	YES	YES	Jun	YES	YES	Dec					
MOS20	Tolouse, France	YES	YES	YES	YES	YES	YES		YES	YES	YES	YES	YES	YES		YES	YES	YES	YES	YES	YES	Dec	YES	Sep					
TSC6	Sendai, Japan	Jun	YES	YES	YES	Jun	Jun	Jun	Jun	Jun	Jun	YES	YES	YES		YES	YES	YES	YES	YES	YES	YES	YES	Dec					
TSMC	Hsinchu, Taiwan	YES	YES		YES	YES	YES	YES	YES	YES	YES	YES	YES	YES		YES	YES	YES	YES	YES	YES	Jun	Jun						

Institutionalized
Actions Identified for missing elements required to meet ZD challenge
Actions identified for all elements required to meet ZD challenge

= Maintenance Items from Phase 2 activity

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Safe Launch Plan Template

- The Safe Launch Template defines elements to be reviewed

1. Information Overview
   - Goal, Team, Module info, Part info
2. Shipment Plan Review
3. IC Manufacturing Review
4. Module Design Review
5. Module Manufacturing Review
6. Failure Analysis Plan Review
7. Returns History Review
8. Risk Assessment

- Actions items are captured and tracked within each section

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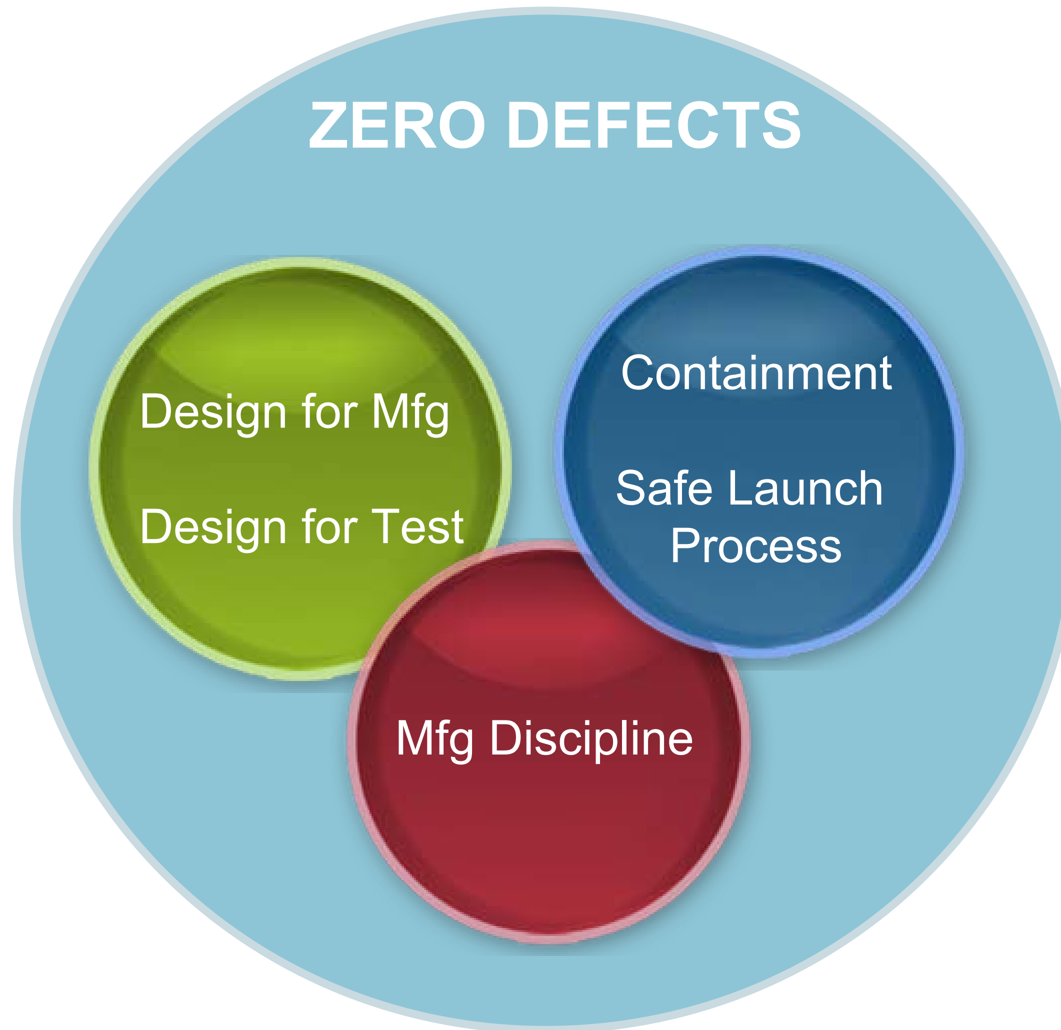
Freescale Zero Defects Methodology



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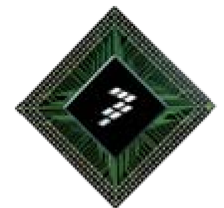

Results

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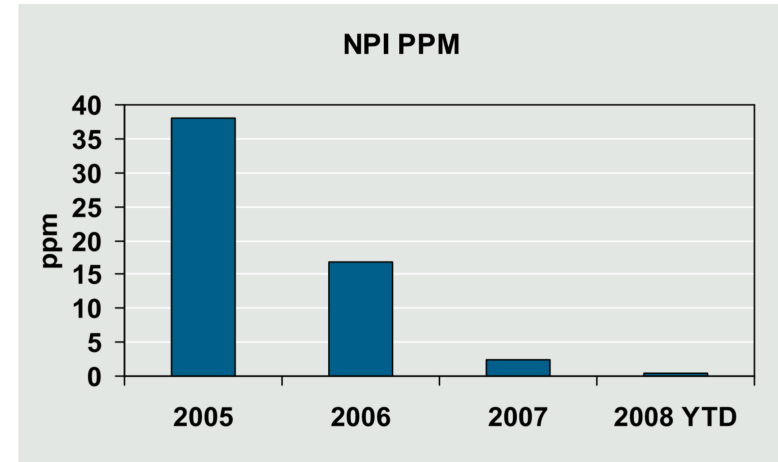
New Product Launch PPM

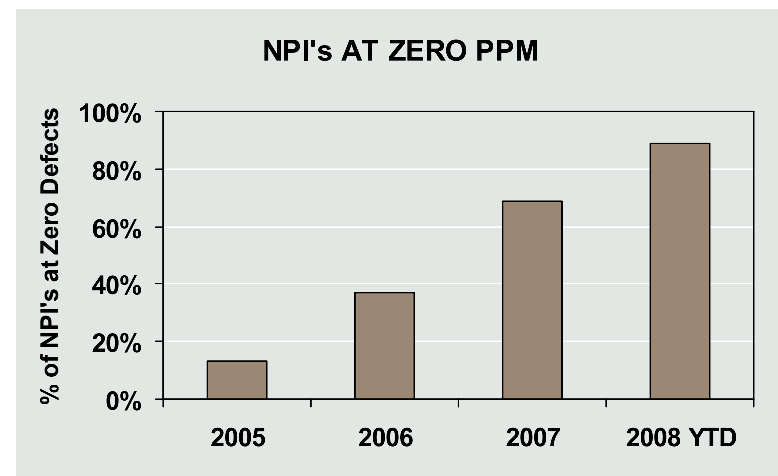
▶ Launch PPM

- First unit shipped through 100K units shipped, plus six months



▶ Improving Launch PPM through:

- Design for Zero Defect Methodology
- Improved Test Maturity Prior to Launch
- Manufacturing
- Safe Launch Partnerships



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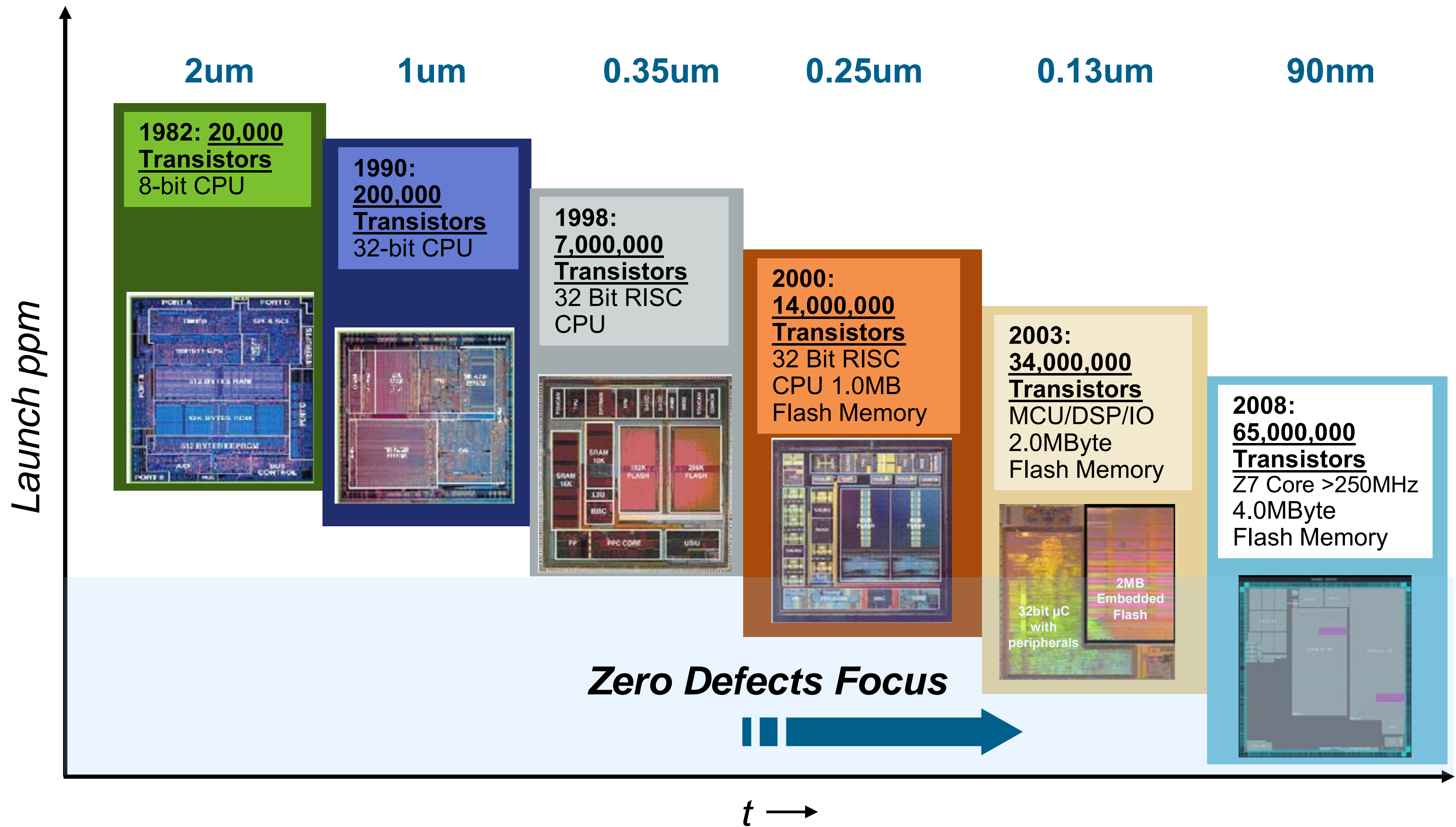
Microcontroller History



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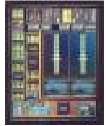
Microcontroller Zero-Defect Strategy

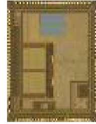


Oaks
1996 design
50 ppm capability
4Q07 ~10 ppm

- Design for Manufacturability
  - Lone Via Fix

- Defect Detection
  - •HVST, ULV
  - •Application specific test
  - •“Look across”
  - •In-line and burn-in FA
- Outlier Controls
  - •SBL, PAT, cockpit charts

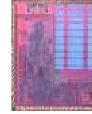
- Defect Reduction
  - Fab in-line monitors
  - KLA, AIT’s, lot reviews



S12
2000 design
<10 ppm capability
Q4’07 ~ 5.0 ppm

- Defect Detection
  - BIST, SCAN

- Zero Defects Foundation



eSYS
2003 design
<1 ppm capability

- Design for Manufacturability
  - Enhanced design rules
  - Line spreading
- Design for Functionality
  - State of art verification/validation
- Design for Test
  - AC/DC SCAN, ATPG, IDDQ
- Partnership “Launch”

- Zero Defects Foundation

C90
2008 design
<1 ppm capability

- 4th Cycle of Zero Defect Learning
- Enhanced tools and processes improve maturity of our DFx capabilities.
- Design for Test
- Design for Manufacturability
- Design for Functionality
- Design for Failure analysis

Zero Defect Foundation

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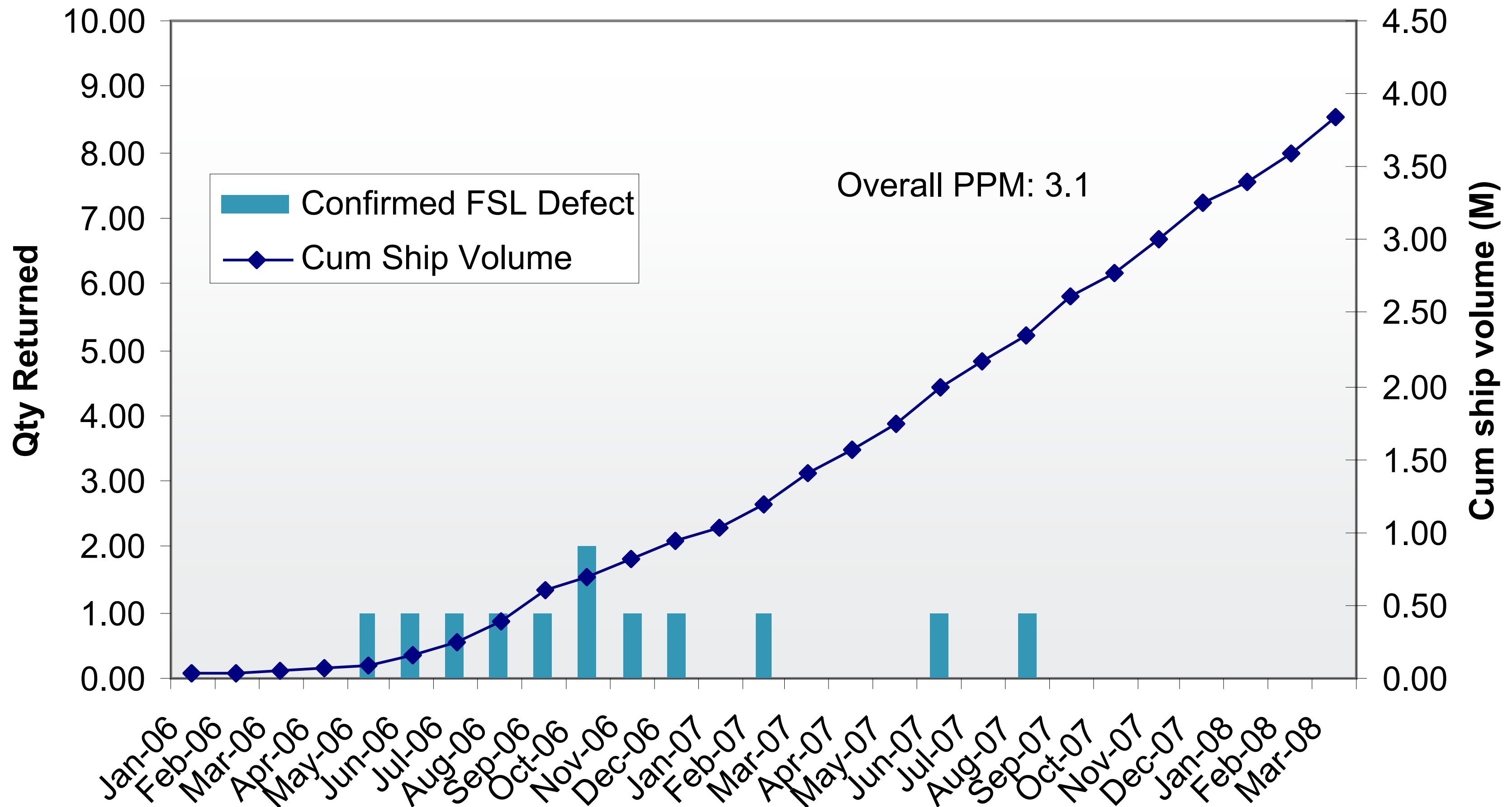
Copperhead PPM Trend



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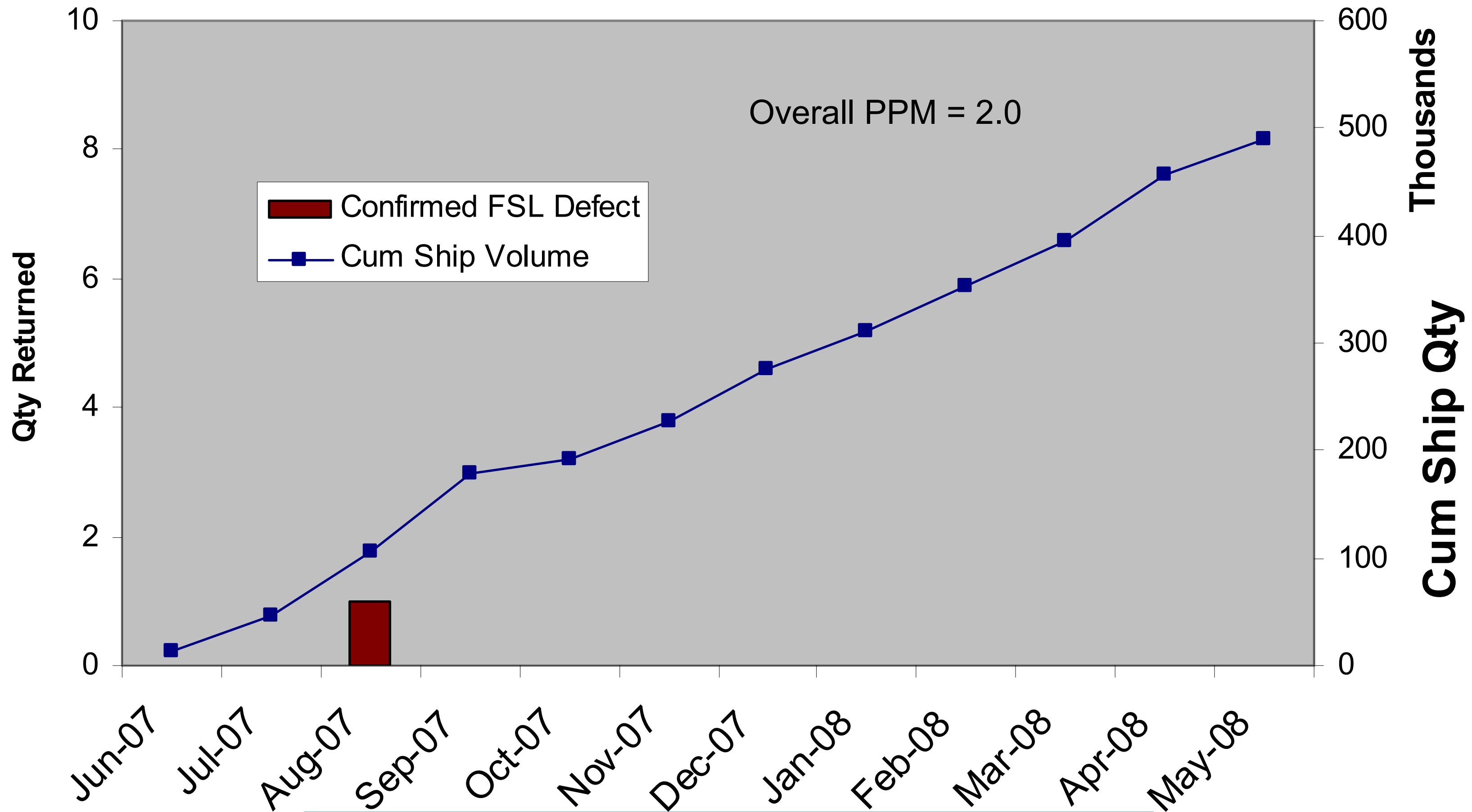
IMX31 Auto 27x27mm PPM Trend



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Freescale Zero Defects Summary

Sort, Set, Shine, Standardize and Sustain (5S)

Product Quality/ Risk Assessment

Part Average Testing and Statistical Bin Limits

Outlier Detection

Fab Defect Reduction

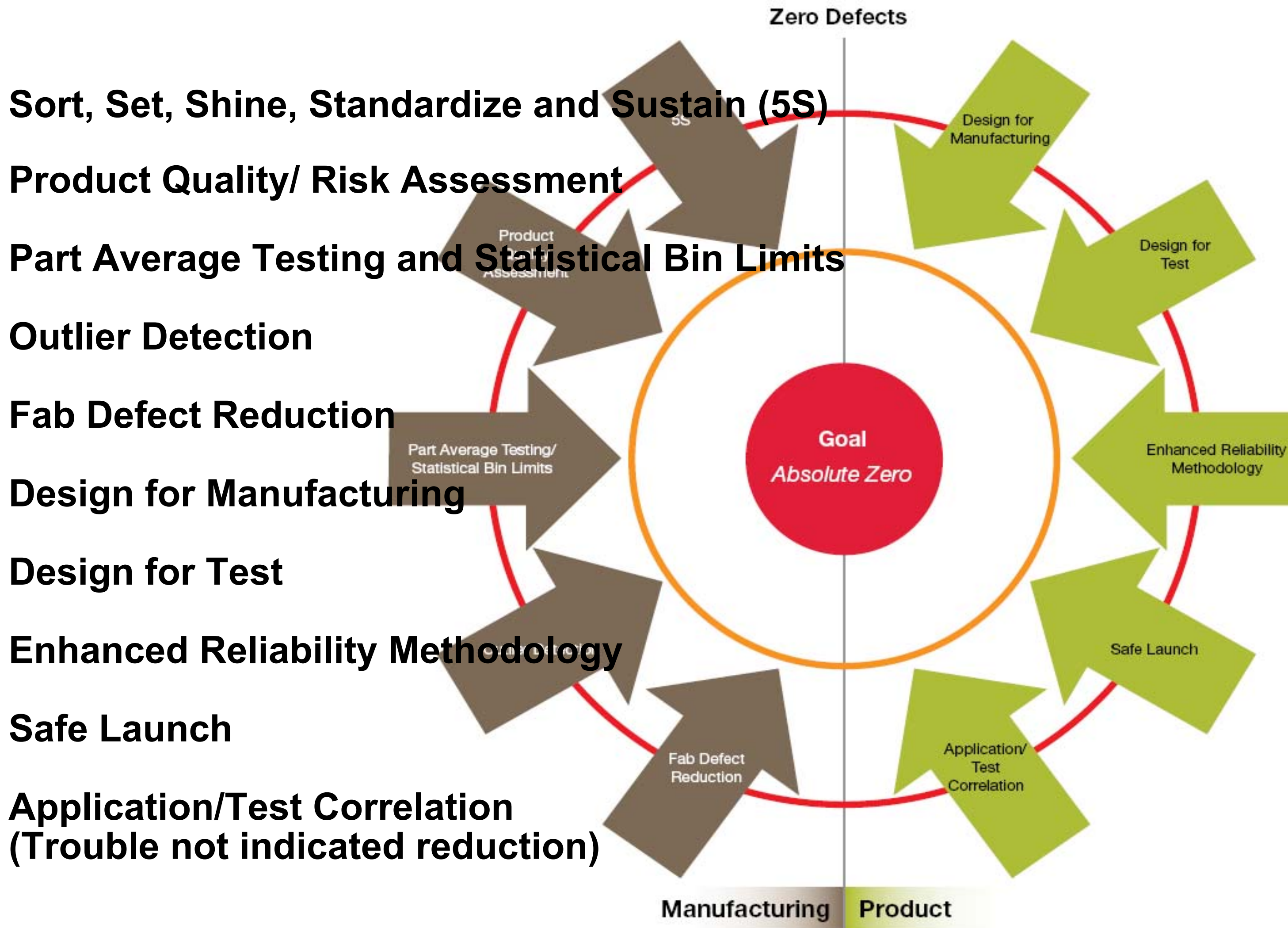
Design for Manufacturing

Design for Test

Enhanced Reliability Methodology

Safe Launch

Application/Test Correlation
(Trouble not indicated reduction)



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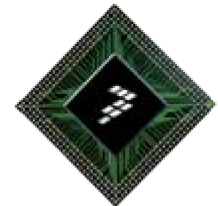
Moving Forward on this Journey



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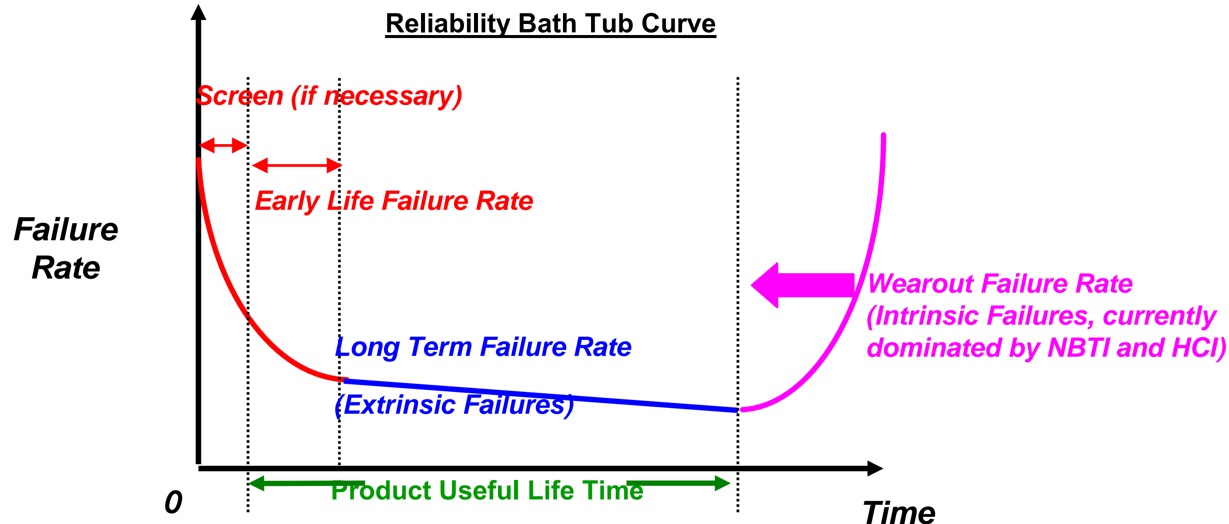
Challenges for Semiconductor Reliability in the Automotive Industry

As technology advances, gate oxides and transistor channel lengths are shrunk at a faster rate than voltage is decreased, and material compositions are changing (nitrogen content in oxides, etc.); thus, the wear out portion of the curve generally shifts to the left.



Intrinsic reliability lifetimes of new technologies are now on the order of expected product use times in the field.

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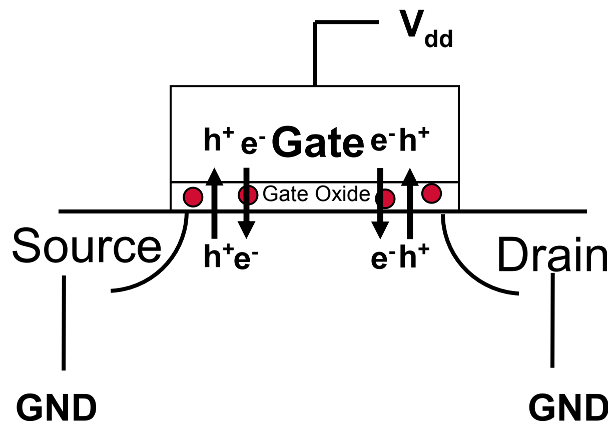
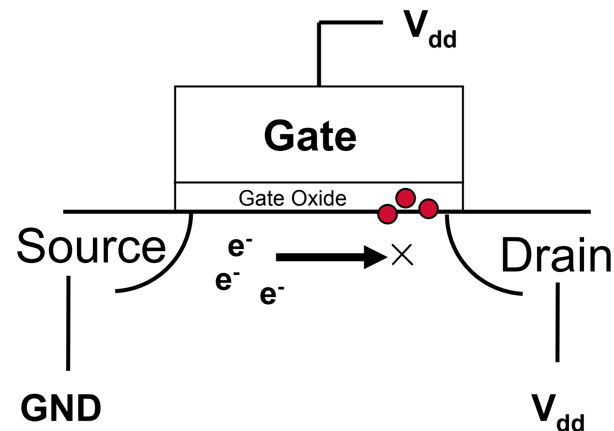
Advanced CMOS Intrinsic Wearout Mechanisms

Dominant intrinsic reliability failure mechanisms in advanced CMOS technologies are Negative Bias Temperature Instability (NBTI) and Hot Carrier Injection (HCI) which cause parametric shifts with some distribution, instead of hard failures.





Negative Bias Temperature Instability (NBTI):

Physical Mechanism:

- Electrons/holes that tunnel across the gate oxide create energetic positive charges that damage or get trapped in the gate oxide.

Effect:

- Primarily an increase in Vt due to trapped charges.
- Occurs in PMOS only.

Hot Carrier Injection (HCI):

Physical Mechanism:

- Electrons/Holes scatter as they go from source to drain.
- Damaging the interface and oxide.

Effect:

- Reduction of mobility (conductance) of the transistor.
- Change in Vt due to charge build-up in oxide.
- Occurs in both NMOS and PMOS

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Performance Shift Mitigation Activities at Freescale

1) **Life Test Simulation Optimization**

   Life Test stress conditions (voltage, temperature) are optimized to ensure AEC required stress time simulates expected field-use time.

2) **Life Test Shift Analysis**

   Critical AC/DC parameters are measured before and after required life test to check for general shifts due to extrinsic or intrinsic failure mechanisms.

3) **Intrinsic Reliability Shift Analysis**

   Required for products in CMOS090 and newer technologies. The general procedure is as follows:

   a) Measure performance before and after life test, preferably at a readpoint that simulates expected field-use time assuming the NBTI failure mechanism (may be different readpoint than (1))

   b) Extrapolate life test performance shifts to expected field shifts, based on NBTI models developed during intrinsic reliability testing. Control sample data is taken into account at this step.

   c) Add HCI effects based on NBTI versus HCI shifts observed during intrinsic reliability testing, since HCI effects are not generally observed during low frequency life testing.

   d) Create product test guardbands based on statistical distribution of normalized shifts.

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Performance Robustness Validation Activities Moving Forward

1) **Split Lot Analysis**

   Performance data is being taken on nominal versus slow PMOS transistor lots to check which patterns may be affected by NBTI. Split lot results will be checked against life test results to determine correlation.

2) **Aging Simulation in Design**

   Aged transistor models are being input to design simulation tools and performance estimates checked against split lot and life test results.

3) **Test Vehicle Evaluations**

   Stress ring oscillators and other test circuits are being stressed in parallel to device stresses to check for shift correlation.

Performance Shifts for Automotive Products

- At this time, performance shift concerns are minimal for Automotive devices, since they generally lag in technology and do not push performance limits.
- To minimize future risks and to assure Zero Defects for Automotive devices in advanced technologies, proactive steps are being taken to understand, minimize, and mitigate risks of performance shifts. Advanced reliability robustness validation techniques will be applied.

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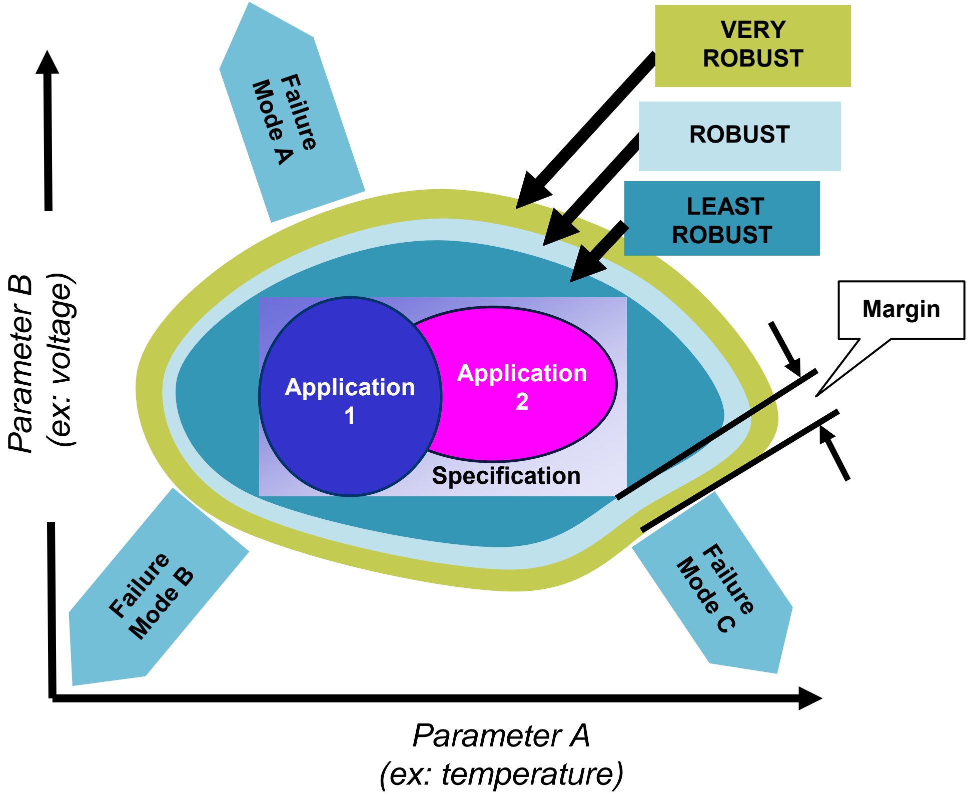
Robustness Validation

There are several techniques under evaluation in Freescale to understand Die, Die / Package, and Package wear out mechanisms

- ESD testing at multiple voltages followed by Operation Life studied to determine failure curves
- Test intrinsic silicon mechanisms to failure
- Extend traditional package level stresses to failure



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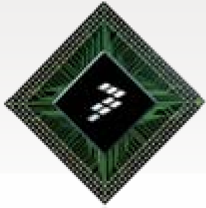

It's ~~Im~~possible.
Zero=Zero.

- Freescale is committed to Zero Defects for Automotive
- Proven commitment to Drive Quality Improvement
- Demonstrated the Ability to Launch Products at Zero Defect Levels
- Continue to Develop and Implement New Zero Defect Strategies on Next Generation Products

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Related Session Resources

Session Location – Online Literature Library

http://www.freescale.com/webapp/sps/site/homepage.jsp?nodeId=052577903644CB

Sessions

Session ID	Title

Demos

Pedestal ID	Demo Title

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