At ADLINK, We CARE

CMOS Image Sensor Testing
CMOS 影像传感器检测

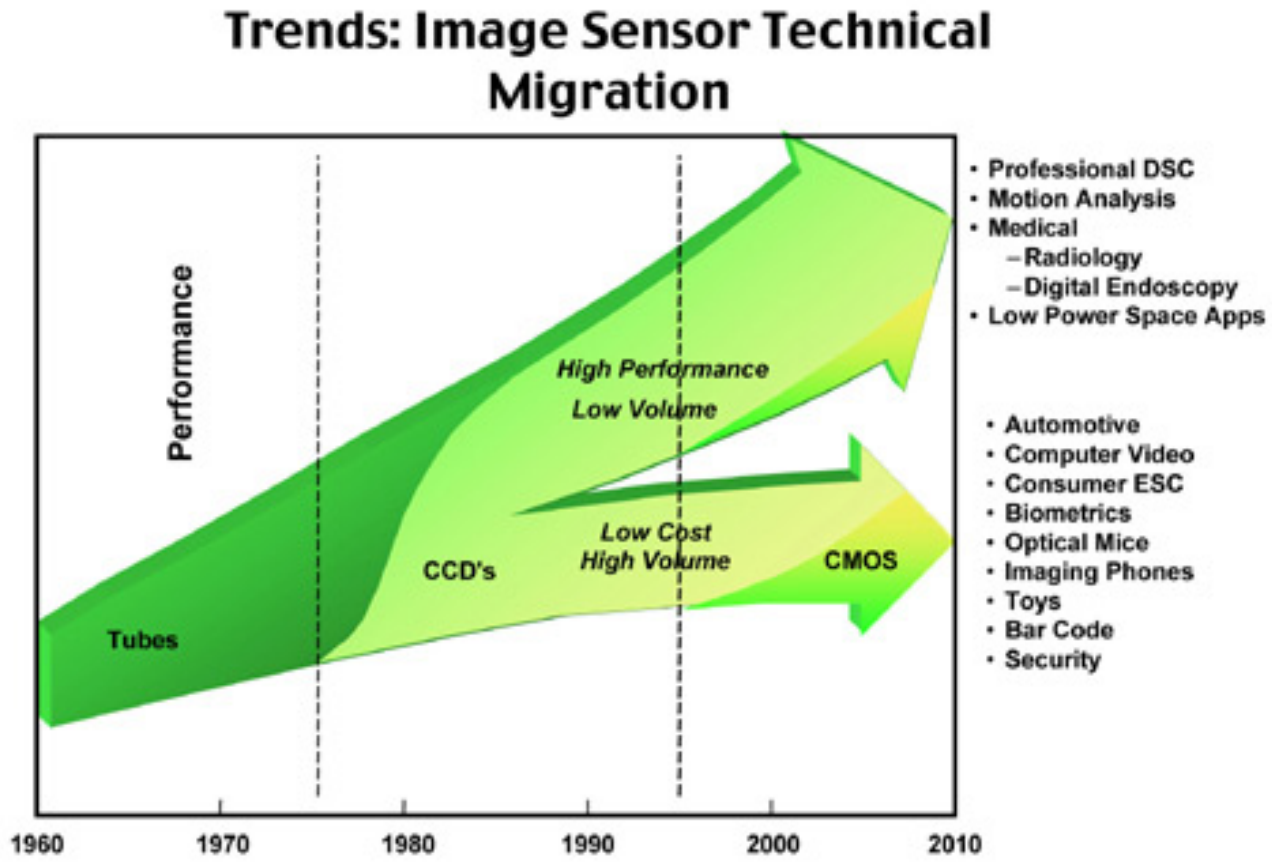
胡正涛
研发总监 量测与自动化产品事业处
凌华科技

ADLINK TECHNOLOGY INC.

CMOS 影像传感器检测

- CMOS 图像传感器(CIS)的发展走势
- CIS 的基本原理
- CIS 测试设备的技术需求与挑战
- 凌华科技对 CIS 测试设备的解决方案
- CIS测试的未来挑战

图像传感器的发展走势图



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CMOS 应用范畴与价值都在持续扩展

- 光学鼠标
- 手机
- 笔记型计算机
- 指纹辨识
- 数位相机
- 保全录像
- Wii 游戏遥控器
- 车用电子(倒车影像)

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CMOS 市场需求预期將大幅增长

- 2006年: 8亿顆
- 2007年: 10亿顆
- 2008年: 12亿顆
- 2009年: 14亿顆
- 2010年: 17亿顆

-- Micro Tech.

CMOS Image Sensor (CIS) 影像传感器测试设备的挑战

- 测试工时 (以3M 画素为例)
  - **1** 分钟**/unit** (全数据模式; 数据抓取与传输; 影像处理; 开路/短路测试…)
- 机台空间与价格
  - **2mx2m; 16** 通道**/**台**; RMB 1~1.5**百万**/**台
- 产能
  - **1K unit/hr/**台 **=> 10**万台**/**亿颗
- 测试成本**/unit: 0.1**美金**/unit**
  - 测试成本占”低阶产品” 售价**(1**美金**)**太高比例

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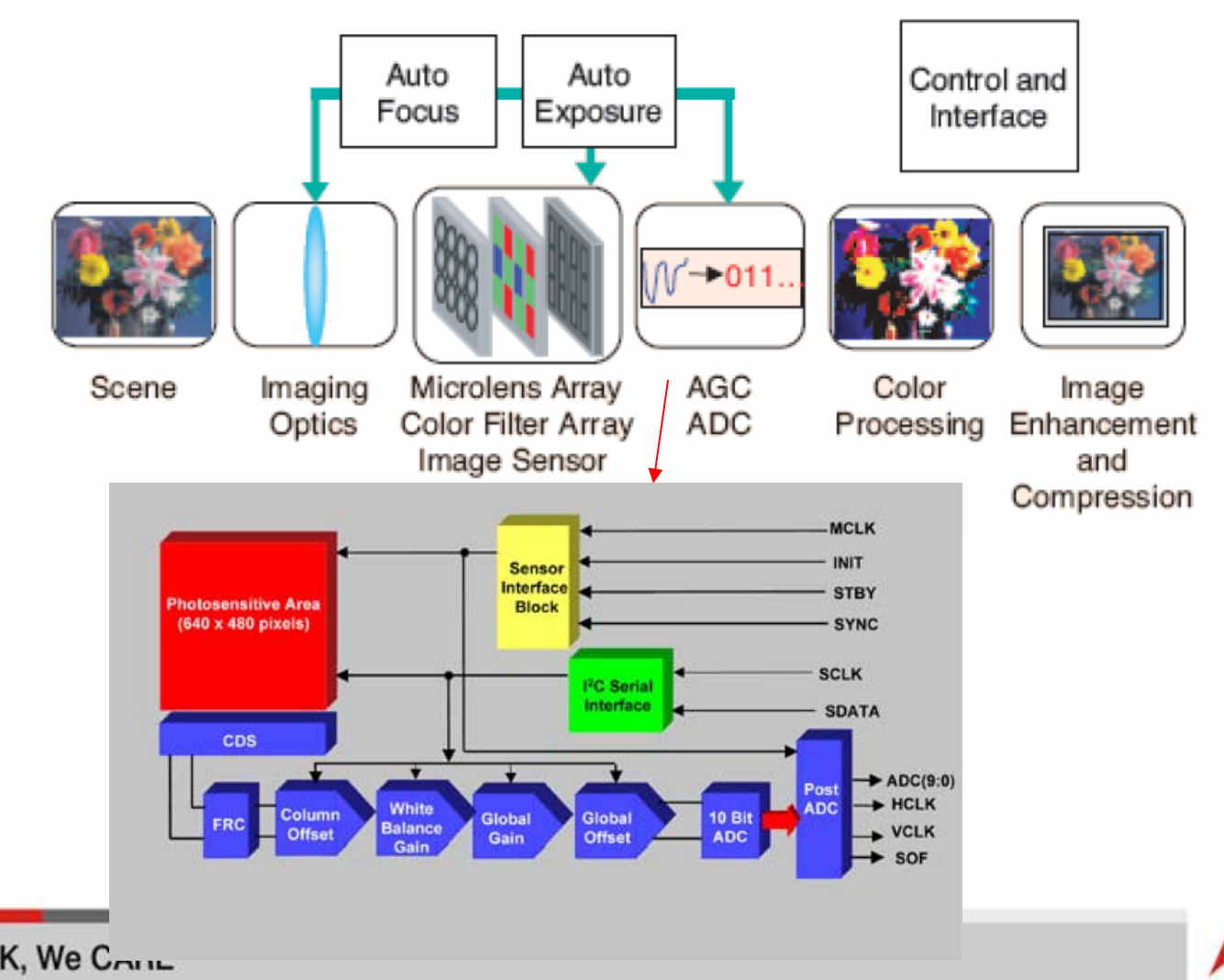
A Typical CMOS Image System



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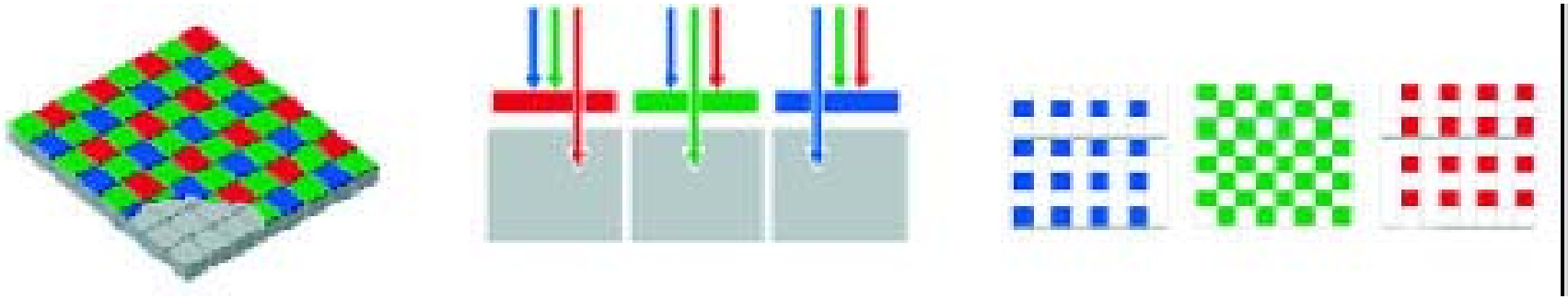
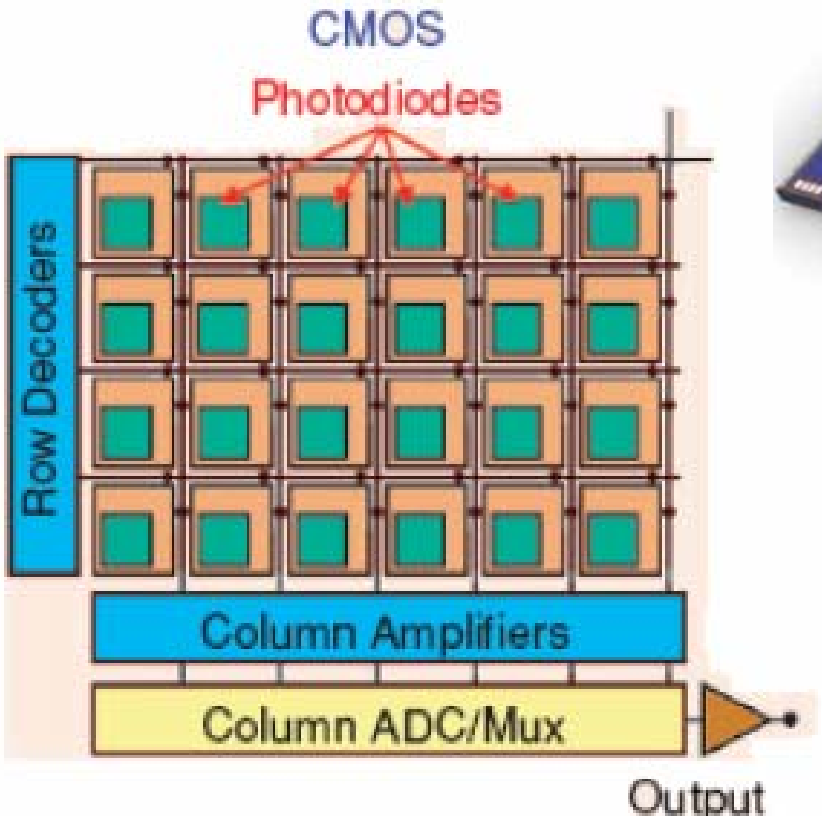
Sensor Color Array
彩色滤波数组

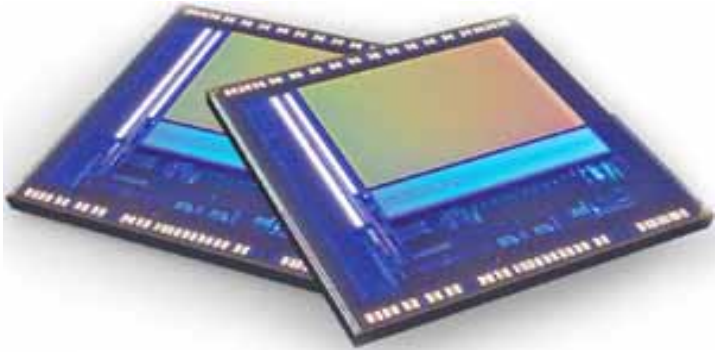


(1)偶数列Line2：B10像素之RGB各值
B10(R)=(R1+R3+R17+R19)/4
B10(G)=(G2+G9+ G11+G18)/4
B10(B)=B10
Sensor偶数Line各像素的RGB计算方法均以此类推

(2)奇数列Line3：G18像素之RGB各值
G18(R)=(R17+R19)/2
G18(G)=(G9+G11+G18+G25+G27)/5
G18(B)=(B10+B26)/2
Sensor奇数Line各像素的RGB计算方法均以此类推

Basic Architectures of CMOS Image Sensor



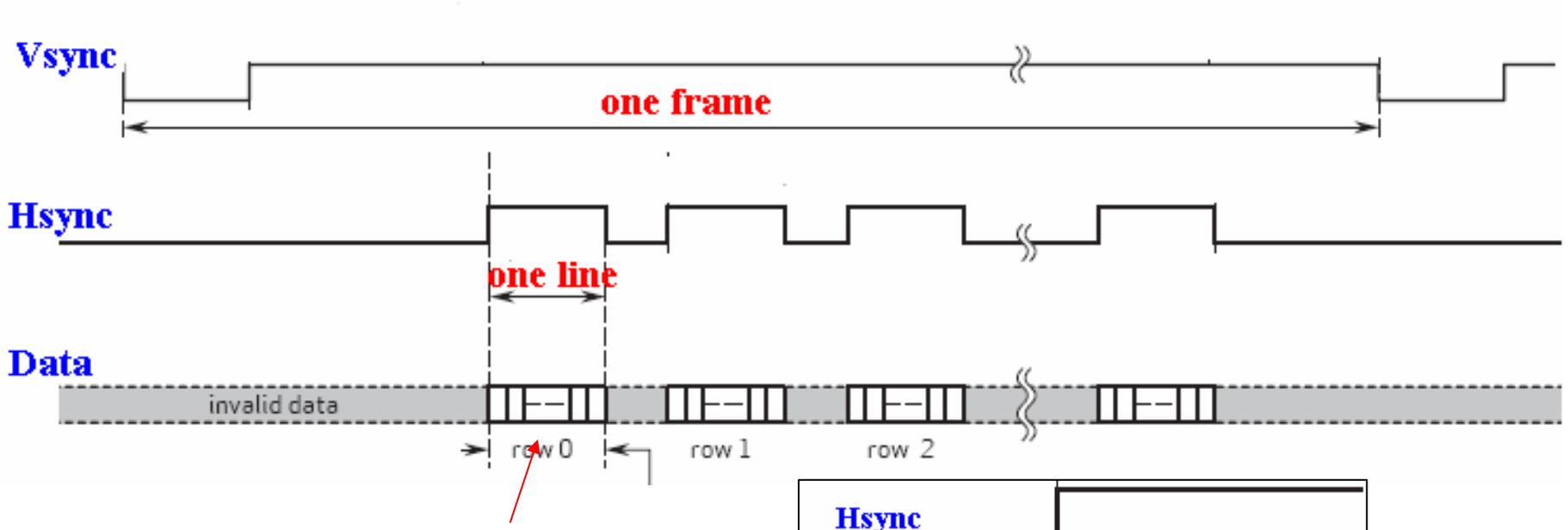


◆影像区域：3.584mm x 2.688mm
◆自动化功效：色彩还原与校正、
Gamma校正、锐利化、白平衡、
黑阶偏移校正、自动曝光
◆最大模拟增益：15.875

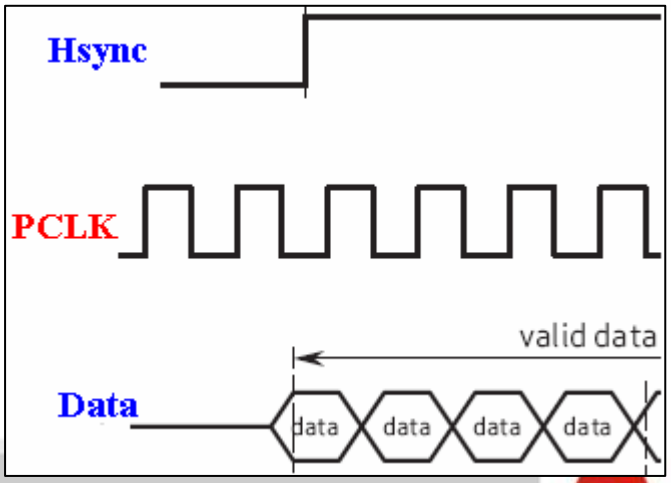
◆动态范畴：>69dB

•**Micron**（美光）**MT9V112I9ASTC**

CIS 信号特性



One pixel clock , one valid pixel data



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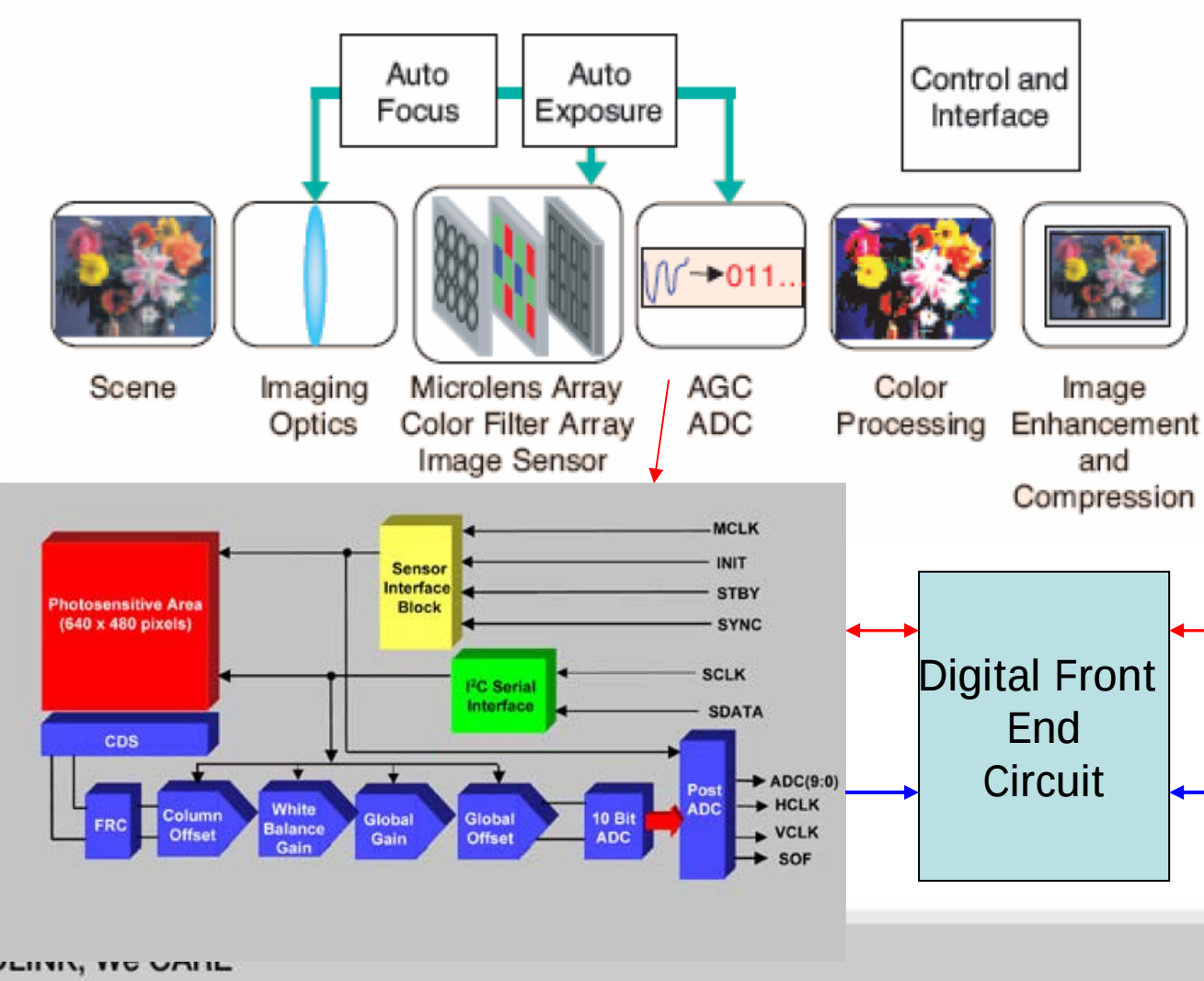
CIS 信号特性

- Array Size
  - 640x480(VGA, 30 万画素)
  - 1600x1200(UXGA, 200万画素)
  - 2048x1536(QXGA, 300万画素)
- Pixel Clock(PCLK)
  - up to 50Mhz ,100Mhz or more.
- Frame rate
  - 15 or30 Frame/Sec
- 资料量：e.g., 300万画素, full-size; 15 FPS; YUV422
  - 2048x1536x15x2 =~95MB => Need PCLK 112MHz

CIS 数据输出格式

- Raw data format
  - 8-/10-bit raw data output for each R/G/B pixel
- YUV422 data format
  - EX:YUV, 2 bytes/each pixel
- JPEG format
  - 8-bit compression data
  - The data length is not fixed

CIS 测试设备的技术需求



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CIS 测试设备的技术挑战

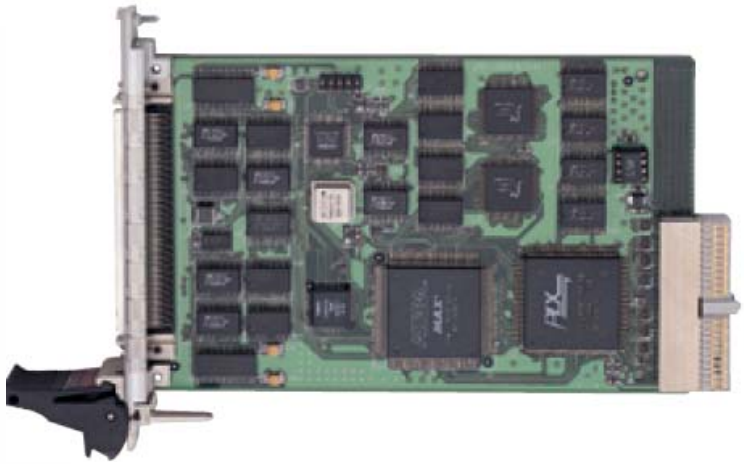
- 需适用不同的数据格式 (Raw/YUV/JPEG); 克服JPEG 每frame压缩量的数据长度的不定性 (depend on algorithm & 画面特性)
- 有时会有 “实时显示”(real-time display）需求 (供RD开发&作业员监看系统用)
- 频宽需求 (100MB/sec.) or more for 越高画素
- 整体硬件成本如何降低
  - DFE 电路最好有 ”多通道” x4 PCIe
  - IPC 可客制化背板, 减少机台体积及工厂空间需求
- CIS 讯号在传输距离如何做到最短 (CIS 通常是低功耗, 推动力会影响传输距离)

凌华科技对 CIS 测试设备的解决方案

- (A) cPCI-/PCI-/PCIe-7300A(new) 高速DIO卡
  - 32-bit @20Mhz => 30~100 万画素CIS
  - PCIe-7350(2008 new)
    - PCIe x1 32-bit @ 50MHZ
    - 300 万画素CIS
- (B) 客制化 CIS Data capture Card
  - PCIe x1 I/O extension; 10-bit data width
  - PCLK up to 112MHZ
  - I^2C configuration interface up to 400Khz
- (C) Camera Link Frame Grabber Card
  - PCIe-CML64F - PCIe x4
  - PCIe-PoL64D – PCIe x4 , Power over Camera Link (2008 new)
  - 500 万画素CIS
  - 300 万画素CIS

(A) cPCI-/PCI-/PCIe-7300A

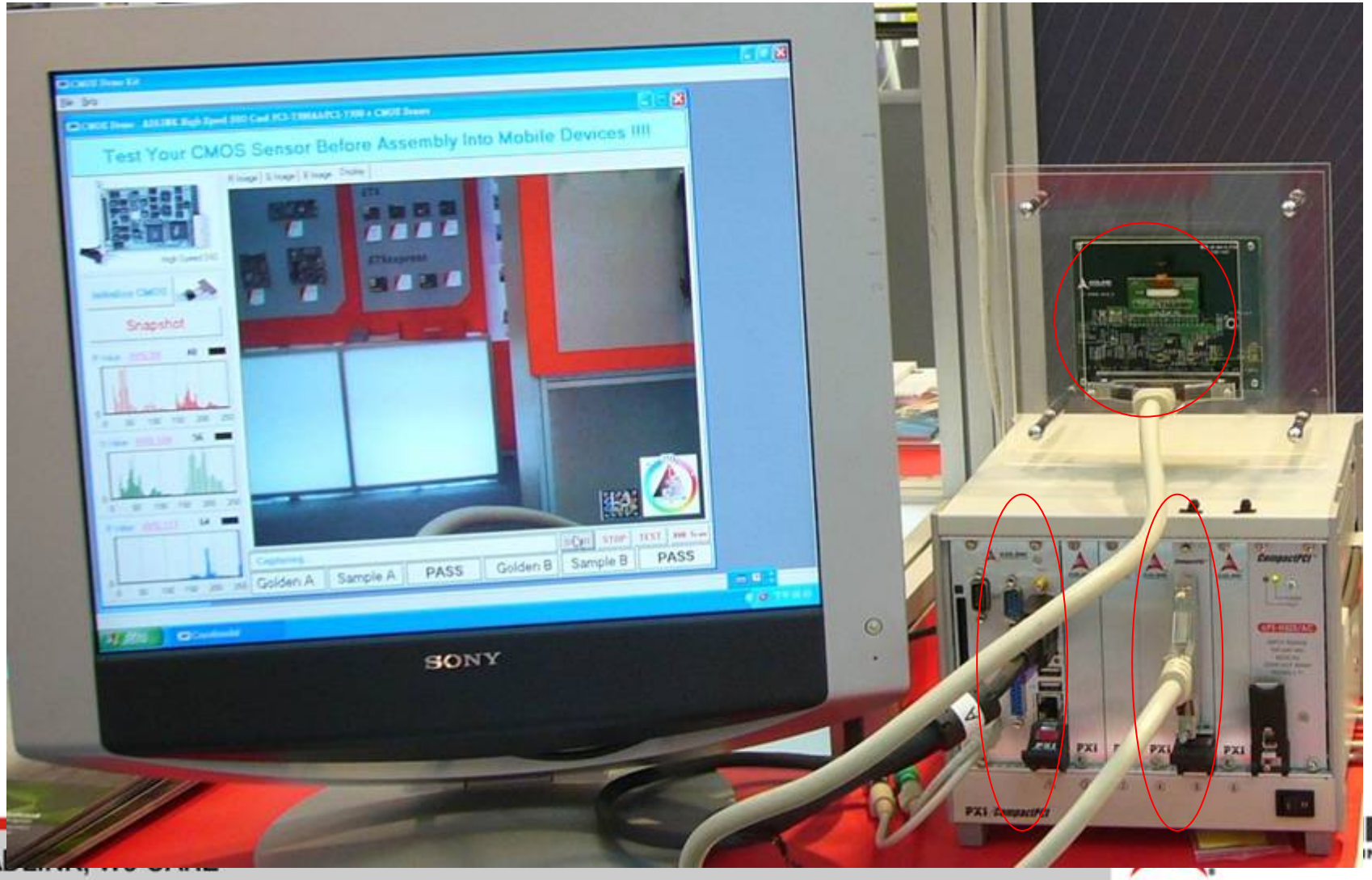
PCIe-7300A



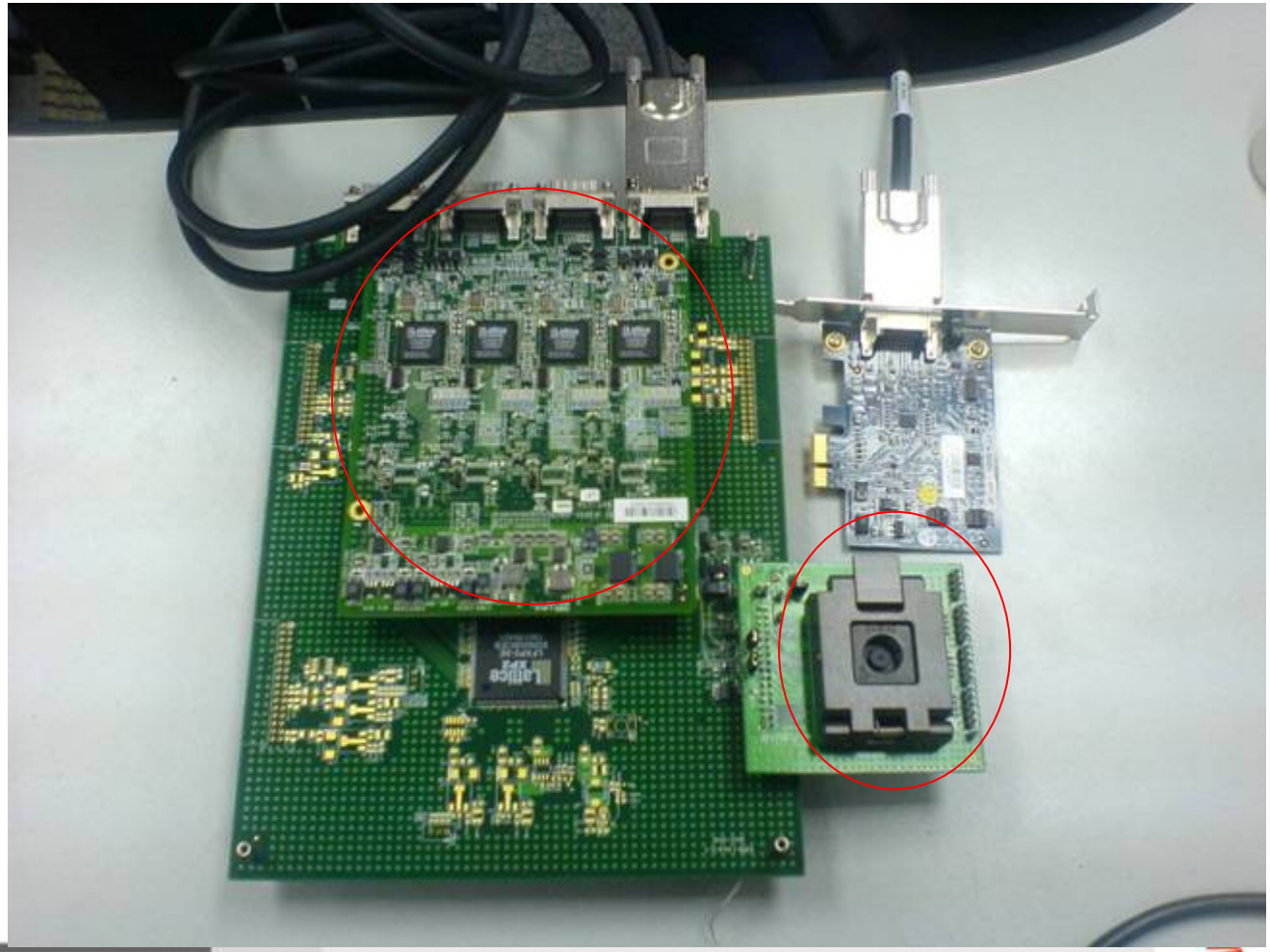
cPCI-7300A

PCI-7300A

VGA (0.3M Pixel), RGB555, 20MHz PCLK (30 FPS)

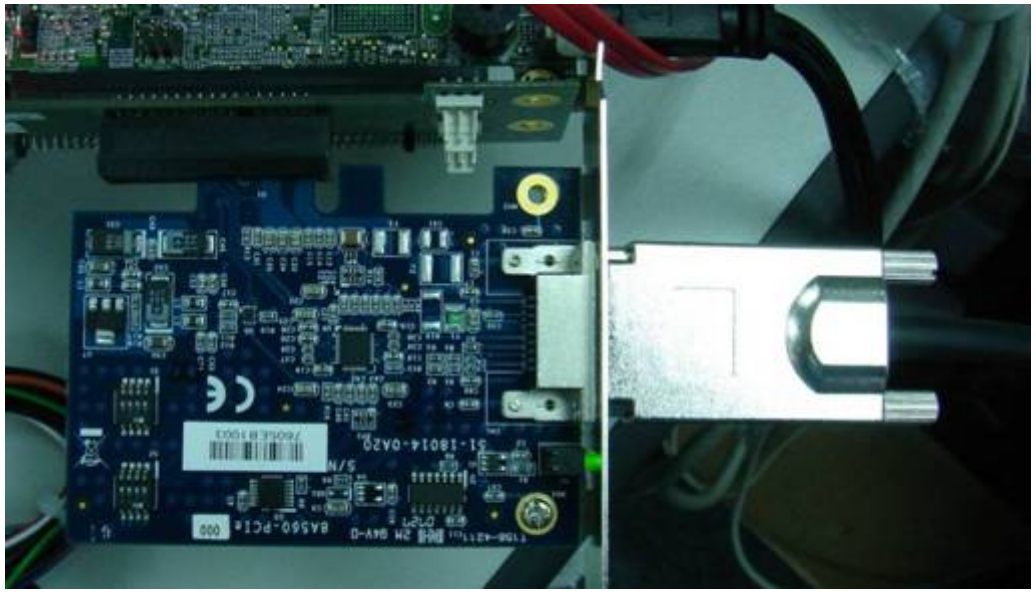


(B)客制化CIS Data Capture Card



配件一: PCIe 延伸板卡

For Mother Board



For Notebook

应用一:系统架构 – 以笔电为例

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应用一：3M Pixel, YUV, 112MHz PCLK, 15FPS

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应用二：CIS 测试机台

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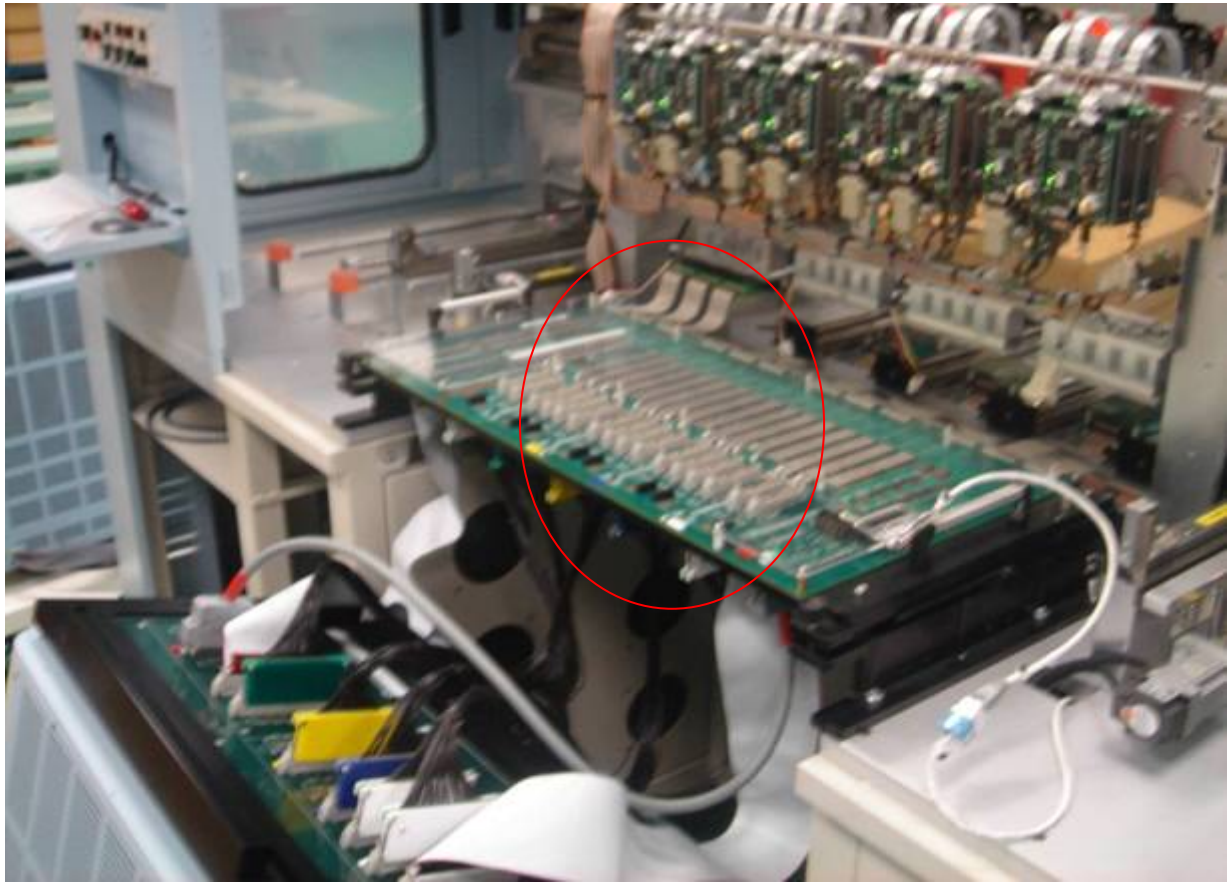
应用二：CIS 测试机台 – DFE 转接板 1



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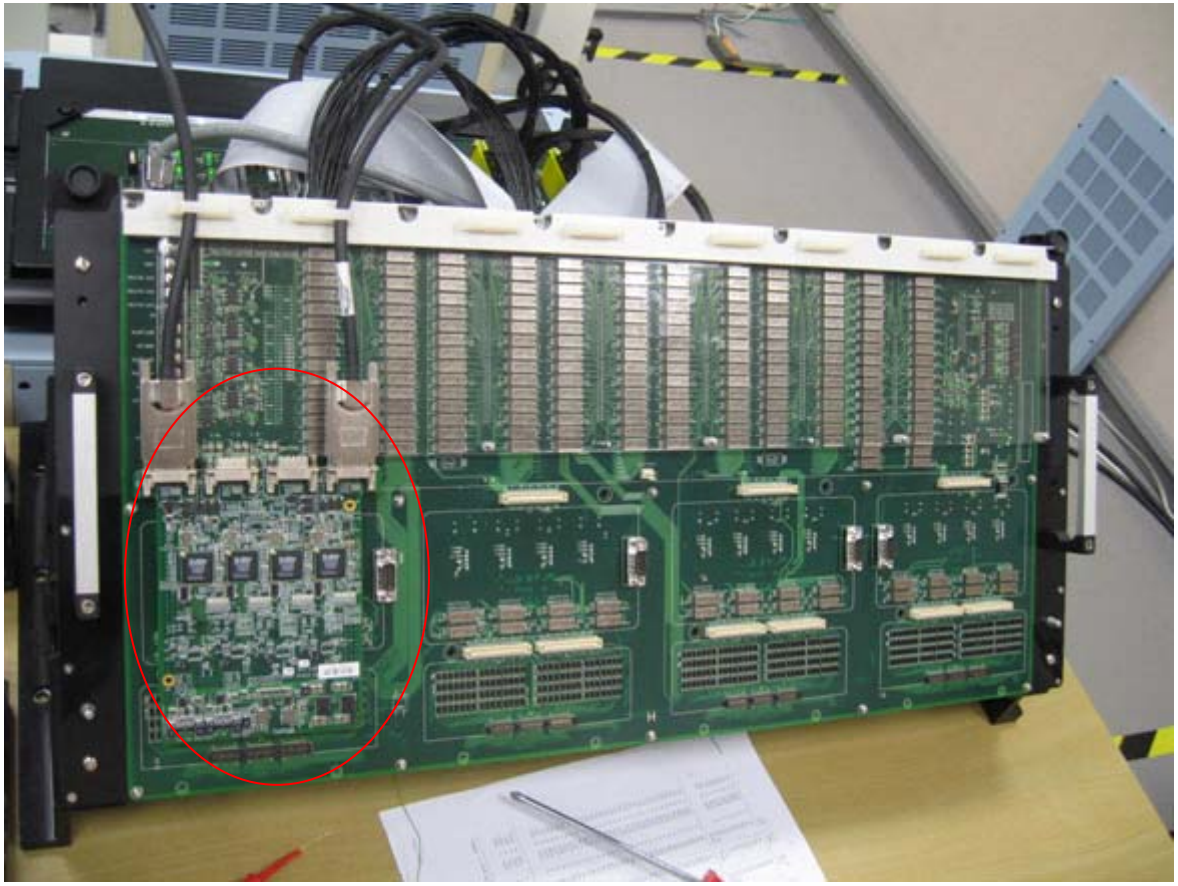
应用二：CIS 测试机台 – DFE 转接板 1+2



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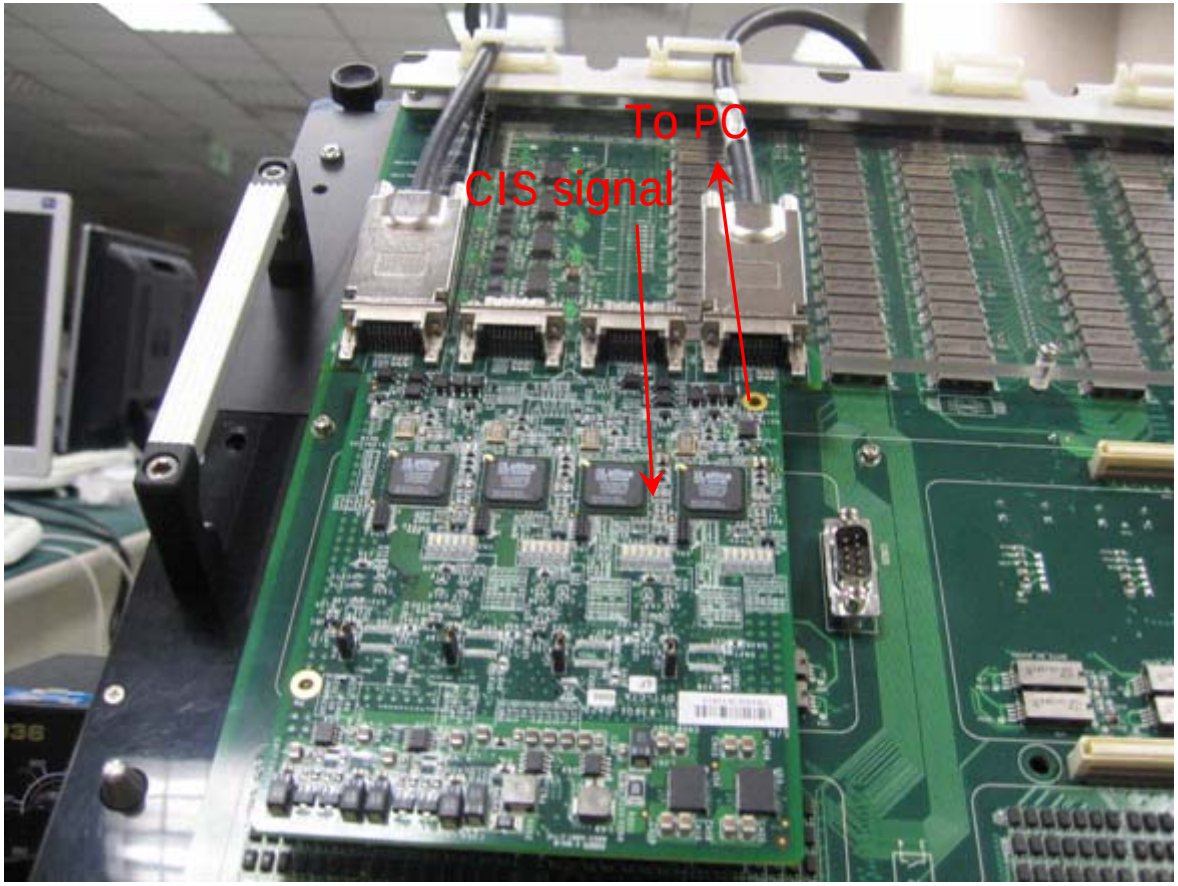
应用二：CIS 测试机台 – DFE 转接板 1+2



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客制化CIS Data capture Card Spec.

- PCIe x1 I/O extension
- Extension cable can be 1~3 meter
- Support Image data format
  - **YUV & RAW**
  - **JPEG – un-fixed** data length
- Data width : **8-bit/10-bit/16-bit**
- Data rate : **up to 112Mbytes/s** , or more
- Support different CIS VCC I/O voltage level
  - From 1.2V to 3.3V
- Support programmable Clock source
  - Up to 112Mhz
- Support I^2C configuration interface
  - Different I/O voltage level form 1.2 to 3.3V
  - SCL : up to 400Khz

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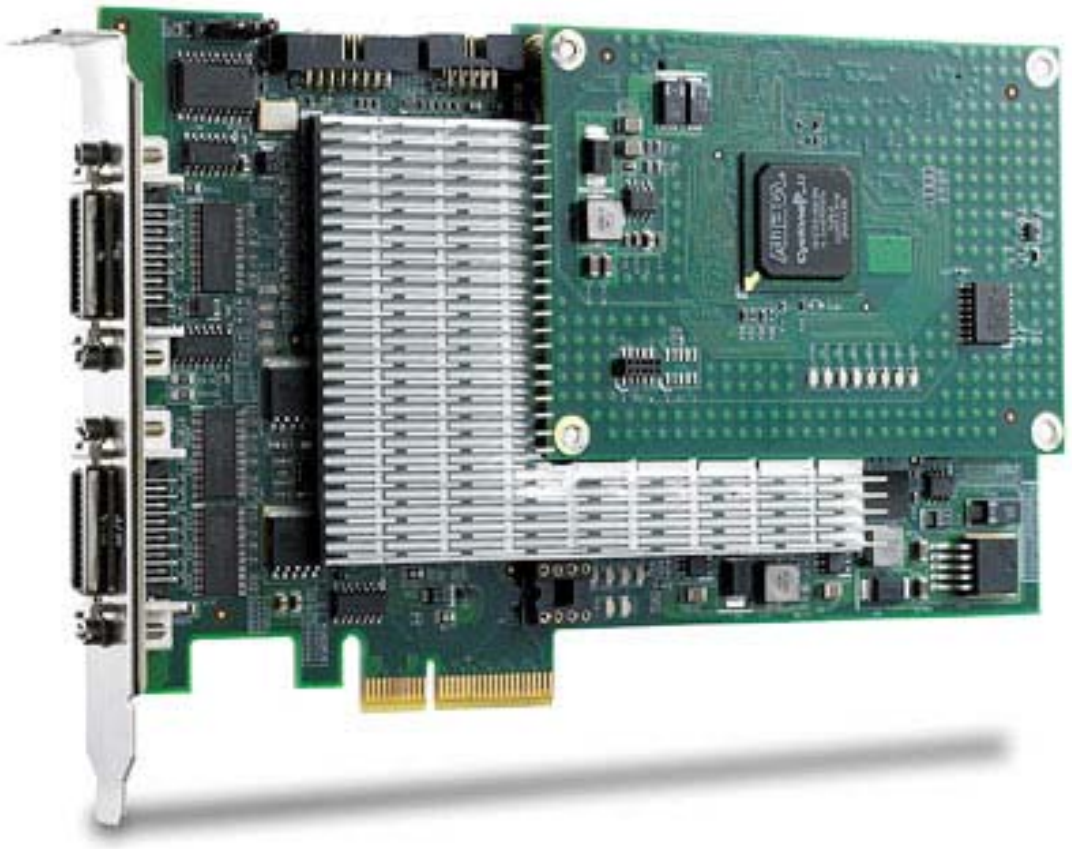
(C) PCIe-CML64F



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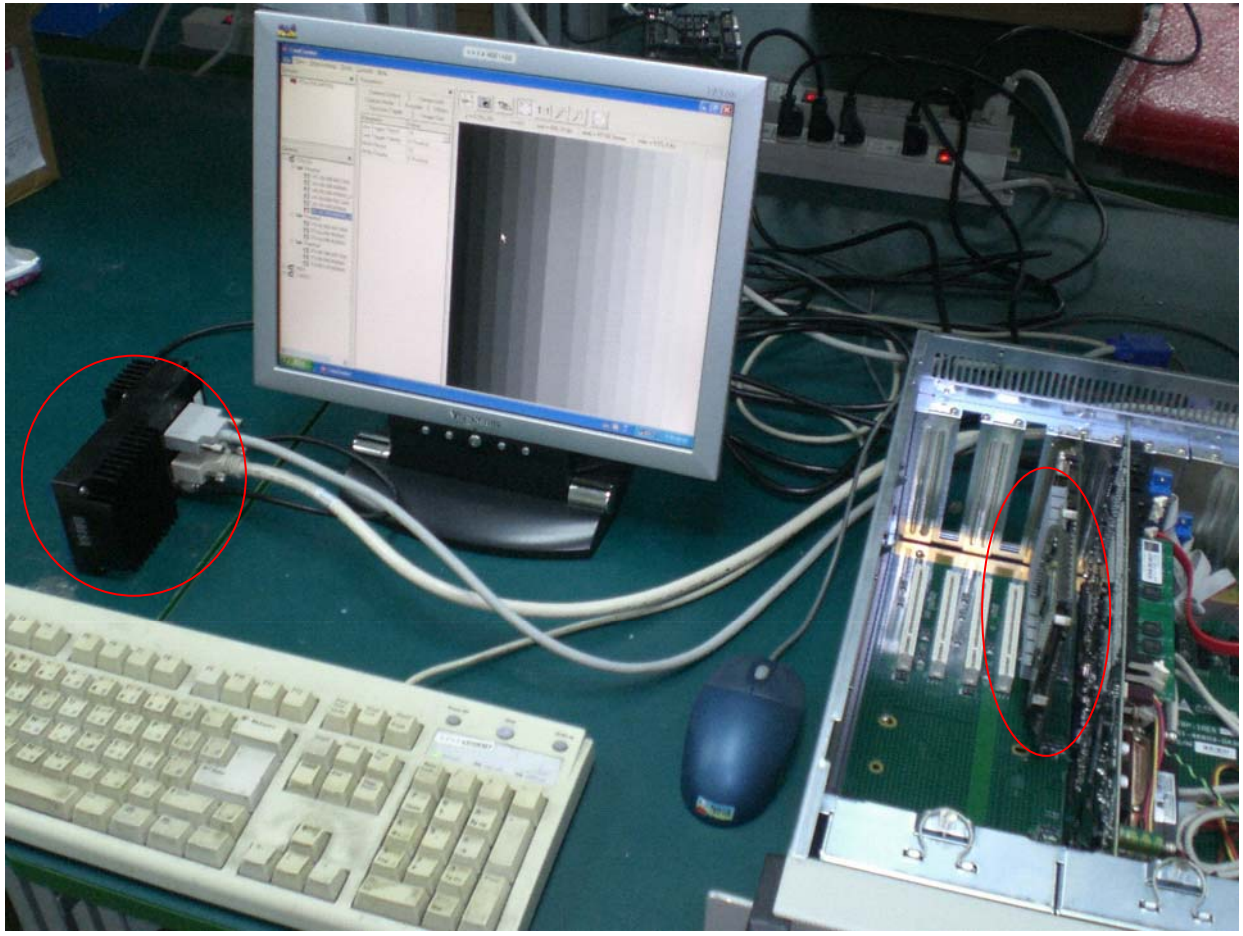
应用一：CCD camera: DALSA HS-80-08k80

8K, 8 tap line sensor CCD, max. line rate 68K

Through put: (8KB/per line)x68K= 544MB/s



应用二：CCD+ PCIe-CML64 line scan AOI

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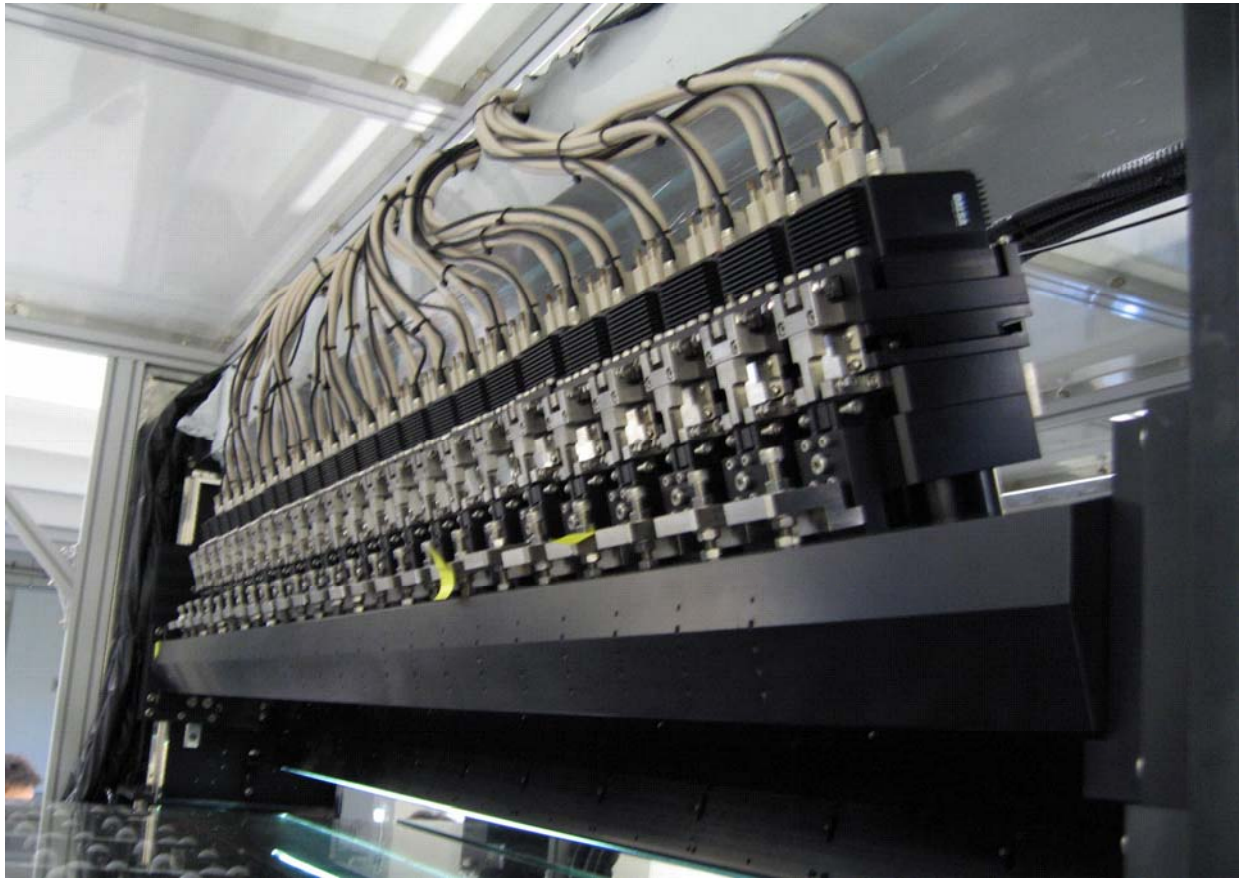
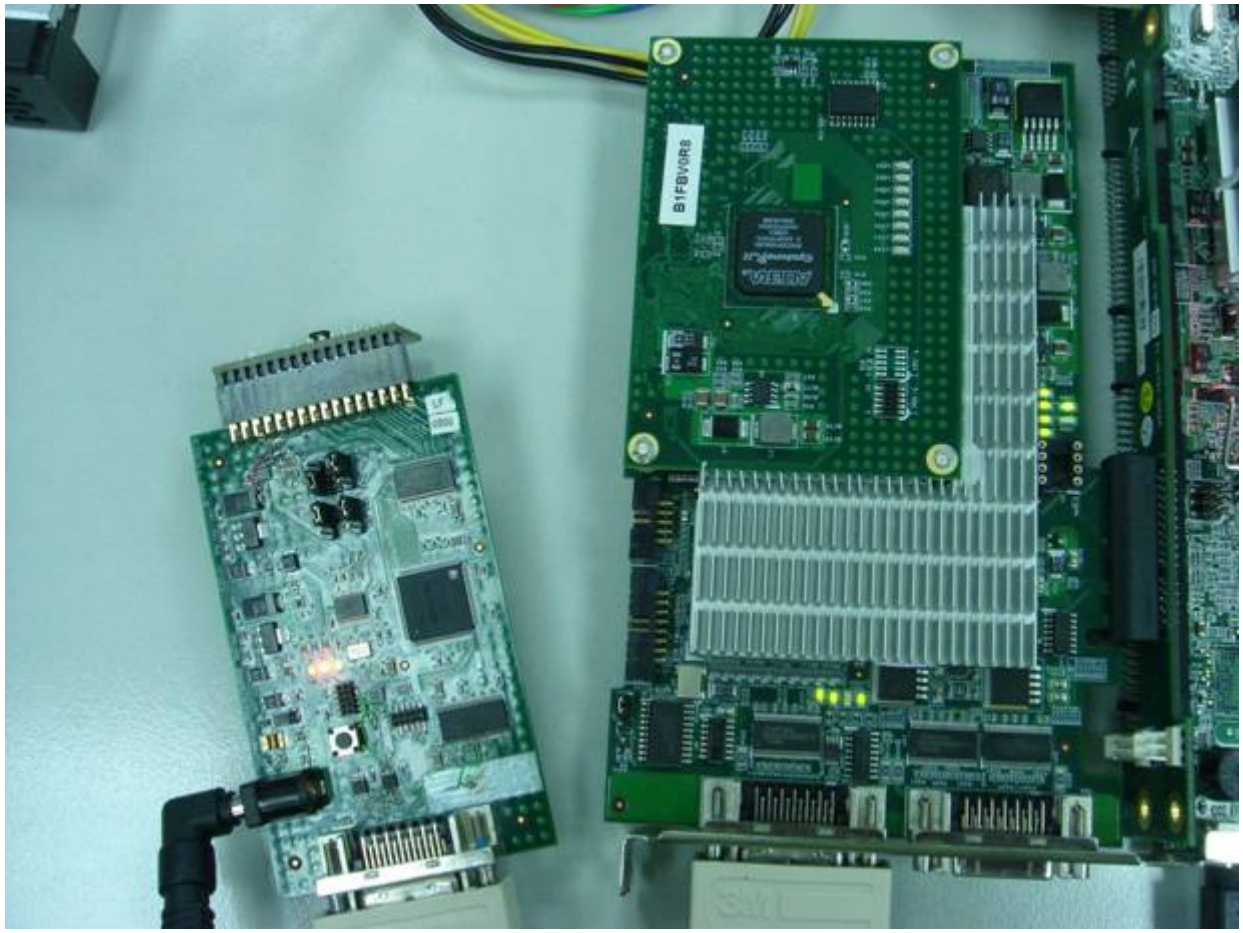
应用二：CCD+ PCIe-CML64 line scan AOI



应用三：CMOS+ CML 转接板 +PCIe-CML64

- 客制化CML转接板
  - 数据格式不同
  - 低成本
- 使用标准CML卡
  - 后处理影像软件完善

应用三：CMOS+ CML 转接板 +PCIe-CML64 – 实际系统



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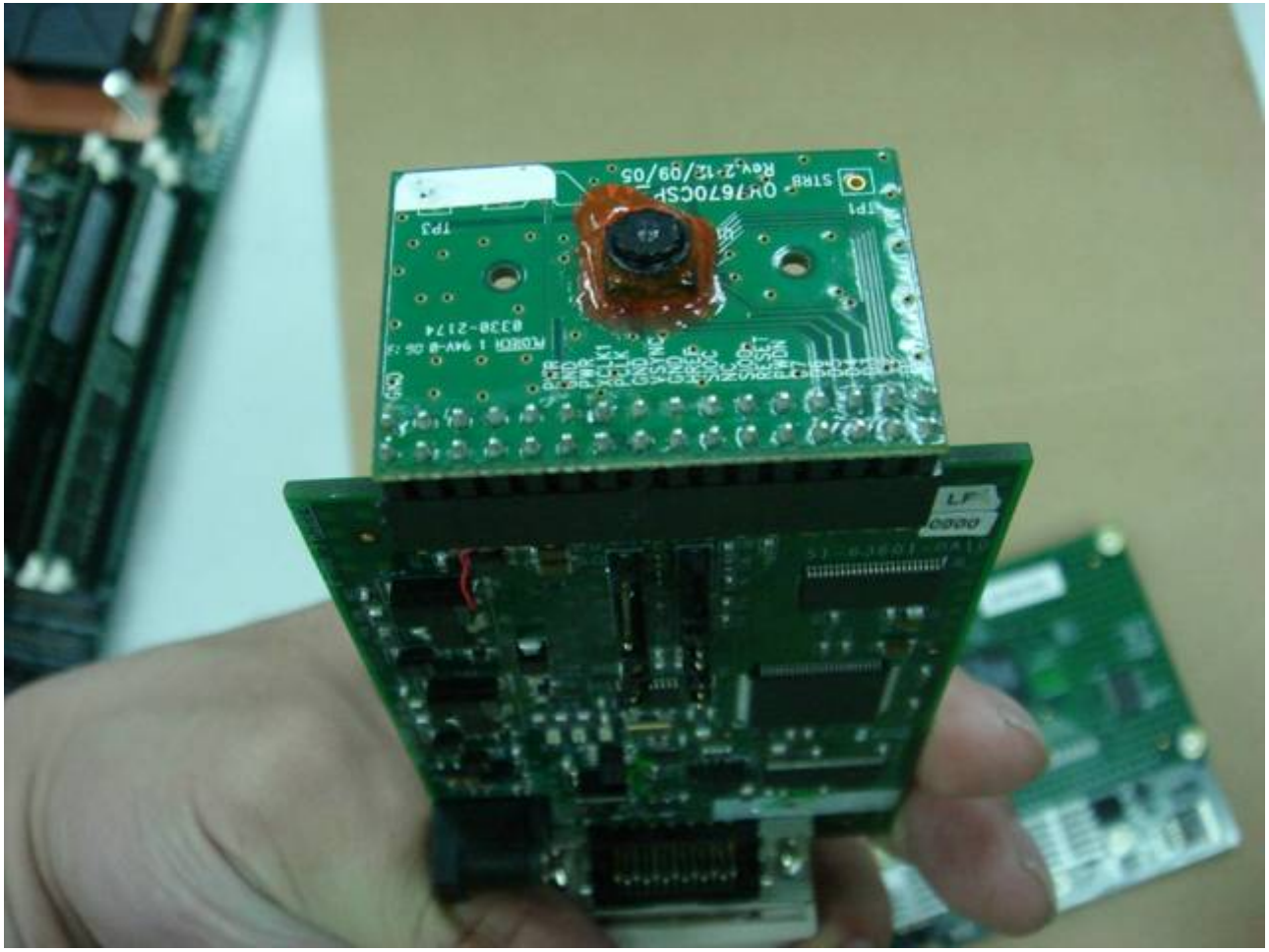
应用三：CMOS+ CML 转接板 +PCIe-CML64 – VGA CMOS



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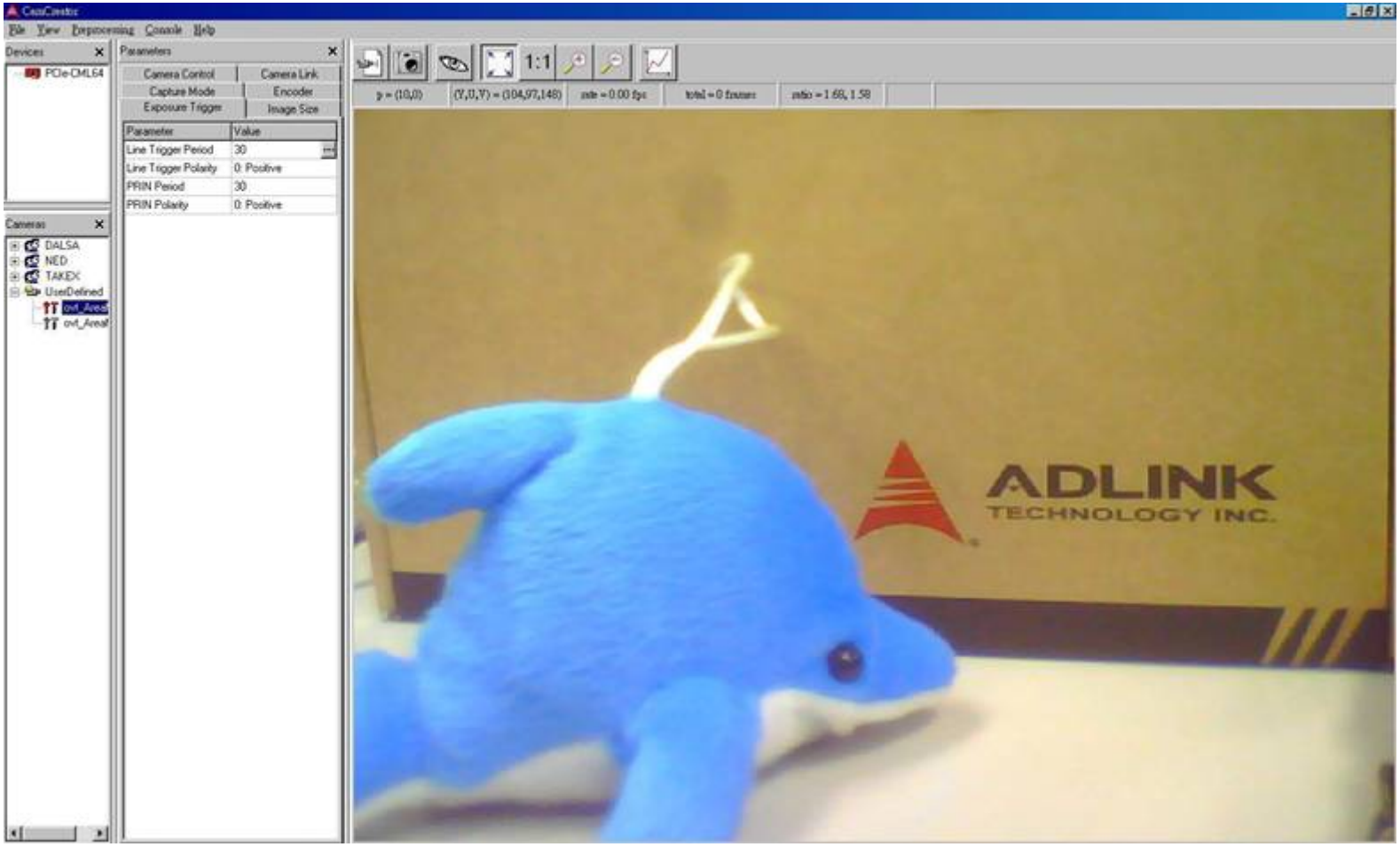
应用三：CMOS+ CML 转接板 +PCIe-CML64 – 实际图像



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CIS 测试的未来挑战

- 影像画素越来越高 (08’ 2M -> 3M; 未來8M)
  - Pixel CLK 112MHz -> up to 200MHz
  - 传输的频宽需求增加:
    - 3M =>需求 112 MB/s => PCIe x1 (250MB/s)
    - 8M =>需求 300 MB/s => PCIe x4 (1GB/s)
- 用嵌入式架构做前处理 **(FPGA解JPEG,做FFT)**
  - 降低 CPU负担
  - 减少测试工时

- Q&A