



MIPI Alliance Standard for Display Pixel Interface (DPI-2)

Version 2.00 – 15 September 2005

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36 Contents

37	Version 2.00 – 15 September 2005	i
38	1 Overview	4
39	1.1 Scope	4
40	1.2 Purpose	4
41	2 Terminology	5
42	2.1 Definitions	5
43	2.2 Abbreviations	5
44	2.3 Acronyms	6
45	3 References	7
46	4 Display Architectures and Interface Constructions	8
47	4.1 Display Architectures	8
48	5 Display Pixel Interface Interoperability.....	13
49	6 Interface Signal Description	15
50	6.1 Power Supply Connections.....	15
51	6.2 Interface Signals	15
52	7 Programmable Timing Parameters	16
53	8 Interface Color Coding.....	18
54	9 Interface Electrical Characteristics	20
55	9.1 Electrical Characteristics	20
56	10 DPI Timing Parameter Examples	23
57	11 Type 2 and Type 3 Display Architecture Control Interfaces	30
58	12 Type 4 Architecture Shutdown and Color Mode Signals	31
59	12.1 Shutdown for Type 4 Architecture	31
60	12.2 Color Mode for Type 4 Architecture	33
61	13 Command Set	34

62 **MIPI Alliance Standard for Display Pixel Interface**

63 **1 Overview**

64 This document describes Display Pixel Interface (DPI), which is used for Active-Matrix LCD displays for
65 handheld devices. The interface may be configured with data path of 16, 18 or 24 parallel data bits, and
66 several control signals.

67 This document specifies the interface requirements for both ends (host and display) of the link, including
68 the following attributes:

- 69 • Electrical
- 70 • Timing
- 71 • Pixel formats (mapping of pixel bits to data signals)
- 72 • Command set to control display behaviors

73 **1.1 Scope**

74 The scope of this document is to specify an electrical and logical interface between a host system
75 (processor or controller) and an active-matrix (AM) display module. The specification is intended for
76 display modules in mobile devices, with display resolution up to 800x480 pixels. This specification does
77 not apply to passive-matrix display modules.

78 Included, and within the scope of this specification, is the power supply for interface signaling between the
79 host processor and the display module. However, power supply for other functions in the display module
80 are beyond the scope of this specification.

81 **1.2 Purpose**

82 The Display Pixel Interface specification is used by manufacturers to design products that adhere to MIPI
83 specifications for mobile device processor, camera and display interfaces.

84 Implementing the DPI standard reduces the time-to-market and design cost of mobile devices by
85 simplifying the interconnection of products from different manufacturers. In addition, adding new features
86 such as larger or additional displays to mobile devices is simplified due to the extensible nature of the MIPI
87 specifications.

88 2 Terminology

89 2.1 Definitions

90 **Command:** Digital information used to control display behavior and to identify the connected display
91 module

92 **Data:** Digital image data stored in the frame memory or numerical information to define the display
93 module behavior accompanied with a command

94 **Display Controller:** Isolated IC silicon chip or integrated functional block in the host processor to control
95 a display module; may or may not include frame memory

96 **Display Device:** Functional device which can show image, such as Liquid Crystal Displays

97 **Display Driver IC:** IC silicon chip in a display module used to control the display device; may or may not
98 include frame memory

99 **Display Glass:** Same as display device, coming from material name

100 **Display Module:** Functional module to show image on it, can consists of display device, display driver IC,
101 other peripheral components and circuits and display interface

102 **Display Panel:** Same as Display Device, coming from the physical outward appearance of the display
103 device

104 **Frame Memory:** Memory device integrated in a display driver IC or display controller in order to provide
105 image data for refreshing the display device. Full-frame memory provides a full screen area of image data
106 while partial-frame memory only provides memory for a portion of the screen area.

107 **Type 1 Display Architecture:** One of the defined display module architectures. In DSI, DBI, DPI, and
108 DCS, a display module architecture in which a display module includes a display device, display driver IC,
109 full-frame memory, registers, timing controller, non-volatile memory and control interface.

110 **Type 2 Display Architecture:** One of the defined display module architectures. In DSI, DBI, DPI, and
111 DCS, a display module architecture in which a display module includes a display device, display driver IC,
112 partial-frame memory, registers, timing controller, non-volatile memory, control interface and video stream
113 interface.

114 **Type 3 Display Architecture:** One of the defined display module architectures. In DSI, DBI, DPI, and
115 DCS, a display module architecture in which a display module includes a display device, display driver IC,
116 registers, timing controller, non-volatile memory, control interface and video stream interface.

117 **Type 4 Display Architecture:** One of the defined display module architectures. In DSI, DBI, DPI, and
118 DCS, a display module architecture in which a display module includes a display device, display driver IC,
119 registers, timing controller, control lines and video stream interface.

120 2.2 Abbreviations

121 High-Z High Impedance

122 H-Sync Horizontal Synchronization

- 123 Ta Ambient Temperature
- 124 VDD Power Supply
- 125 V_{DDI} Logic Level Supply
- 126 V-Sync Vertical Synchronization

127 **2.3 Acronyms**

- 128 AGND Analog ground, for power connection
- 129 AM Active Matrix
- 130 ASIC Application Specific Integrated Circuit
- 131 CM Color Mode
- 132 CMOS Complementary Metal Oxide Semiconductor
- 133 DBI Display Bus Interface
- 134 DCS Display Command Set
- 135 DE Data Enable
- 136 DGND Logic ground, for power connection
- 137 DOI Dependent On Implementation
- 138 HBP Horizontal Back Porch
- 139 HFP Horizontal Front Porch
- 140 I/O Input/Output
- 141 LCD Liquid Crystal Display
- 142 LSB Least Significant Bit
- 143 MIPI Mobile Industry Processor Interface
- 144 MSB Most Significant Bit
- 145 PCLK Pixel Clock
- 146 SD Shutdown
- 147 VBP Vertical Back Porch
- 148 VFP Vertical Front Porch

149 **3 References**

- 150 [1] MIPI Alliance Standard for Display Command Set, version 0.36, June 2005
- 151 [2] MIPI Alliance Standard for Display Bus Interface, version 0.xx, August 2005

152 **4 Display Architectures and Interface Constructions**

153 **4.1 Display Architectures**

154 The display module shall be based on Type 1, Type 2, Type 3 or Type 4 display architecture.

155 The Type 1 Display Architecture should consist of the following functional blocks:

156 Display Device. Used to show the image data.

157 Display Driver. May be one or more devices used to drive the display device.

158 Full-frame memory. Used to hold the image data; can be integrated in the display driver.

159 Registers. Used to configure the display module behavior and hold identification information; can
160 be integrated in the display driver.

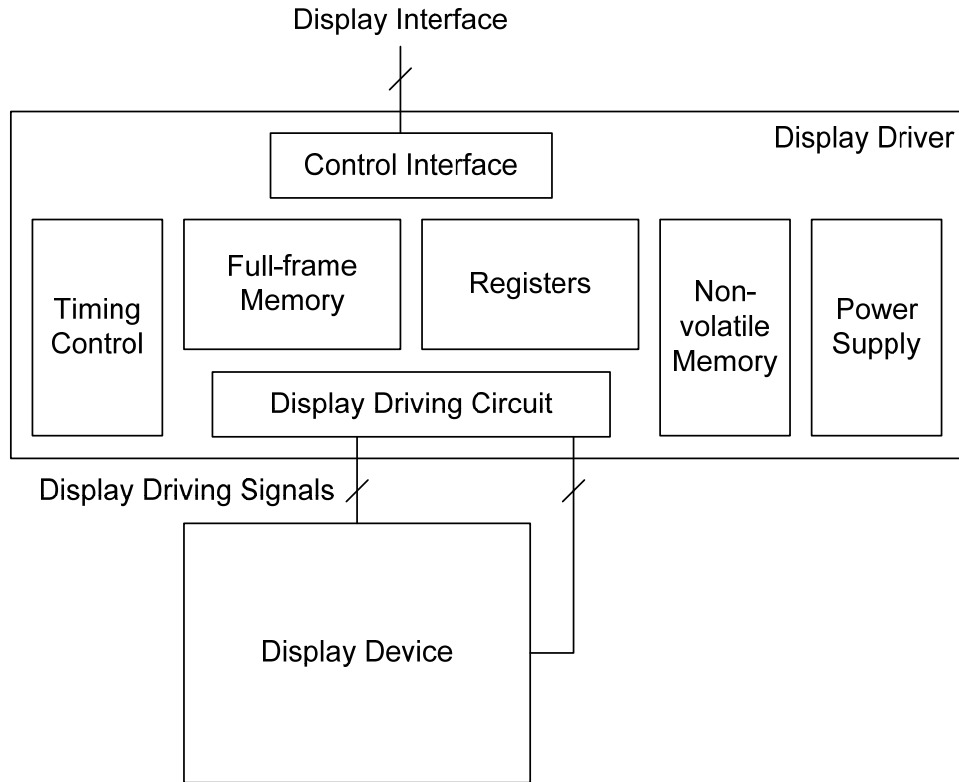
161 Timing Controller. Provides timing signals to control the display device and display driver based
162 on configuration information; can be integrated in the display driver.

163 Non-volatile memory. Used to store default register and configuration values; can be integrated in
164 the display driver.

165 Control Interface. Provides the interface between the host processor and the display driver; can be
166 integrated in the display driver.

167 Display Driving Circuit. As a part of display driver, used to convert timing signals and voltages to
168 signals appropriate to drive the display device.

169 Power Supply. Used to convert system voltages to levels usable by the display device and display
170 driver; can be integrated in the display driver.



171

172

Figure 1 Type 1 Display Architecture Block Diagram

173 The Type 2 Display Architecture should consist of the following functional blocks:

174 Display Device. Used to show image data.

175 Display Driver. May be one or more devices used to drive the display device.

176 Partial-frame memory. Used to hold image data. Can be integrated in the display driver.

177 Registers. Used to configure the display module behavior and hold identification information; can
178 be integrated in the display driver.

179 Timing Controller. Provides timing signals to control the display device and display driver based
180 on configuration information; can be integrated in the display driver.

181 Non-volatile memory. Used to store default register and configuration values; can be integrated in
182 the display driver.

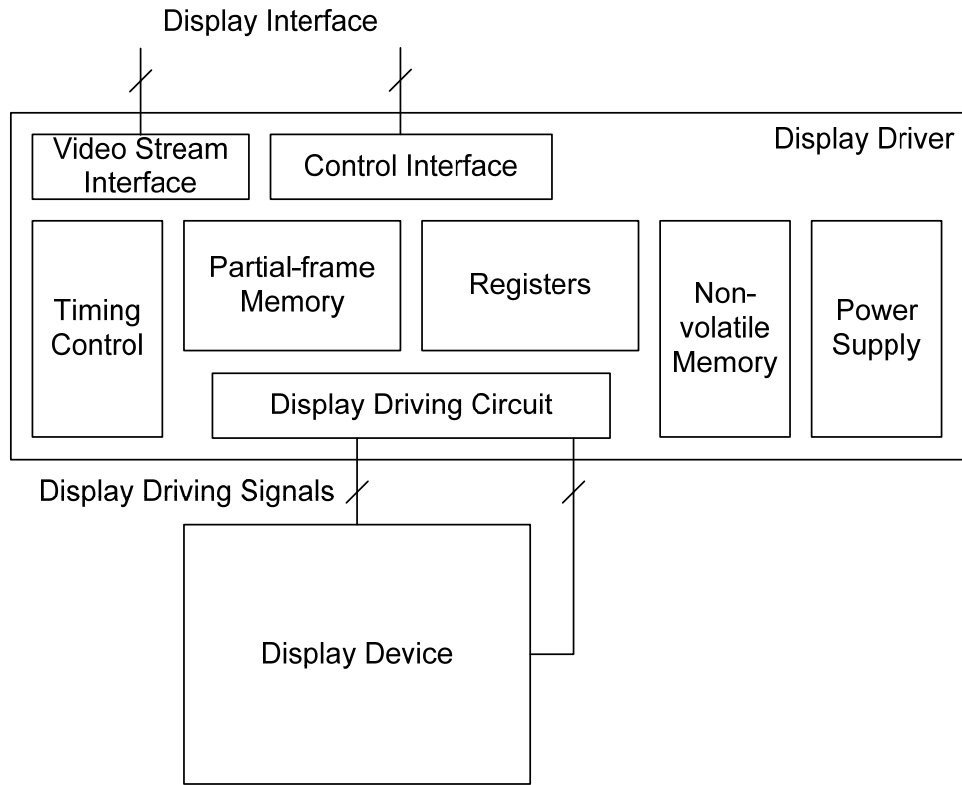
183 Control Interface. Provides the interface between the host processor and the display driver; can be
184 integrated in the display driver.

185 Display Driving Circuit. As a part of display driver, used to convert timing signals and voltages to
186 signals appropriate to drive the display device.

187 Power Supply. Used to convert system voltages to levels usable by the display device and display
188 driver; can be integrated in the display driver.

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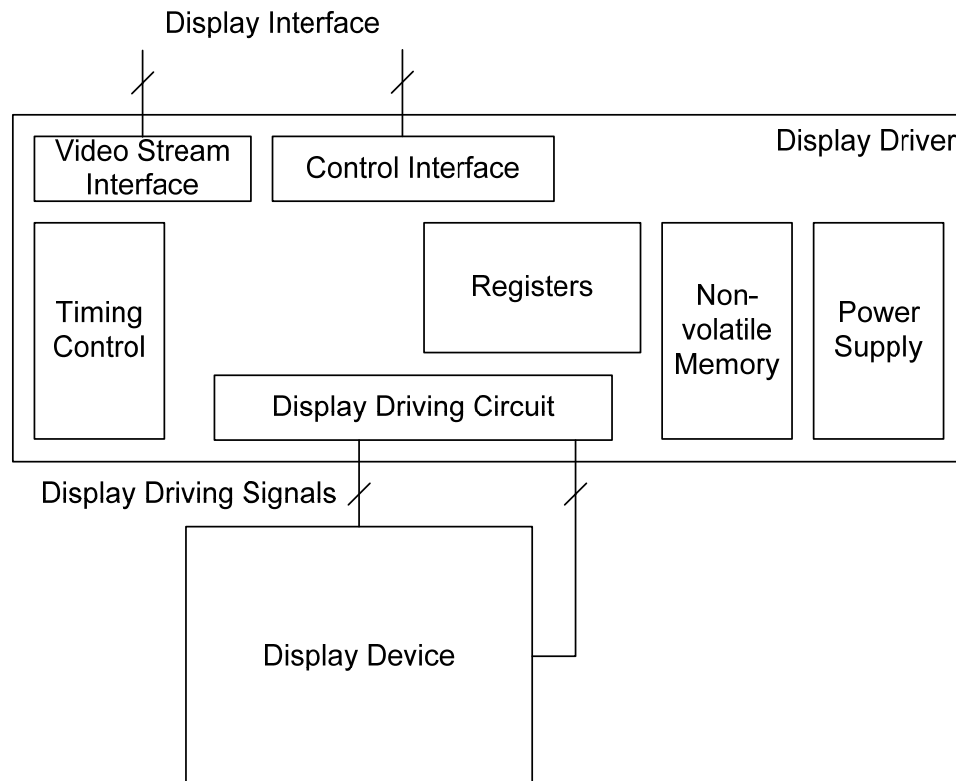
Video Stream Interface. Used to receive video image data and timing signals from the host processor.



191
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Figure 2 Type 2 Display Architecture Block Diagram

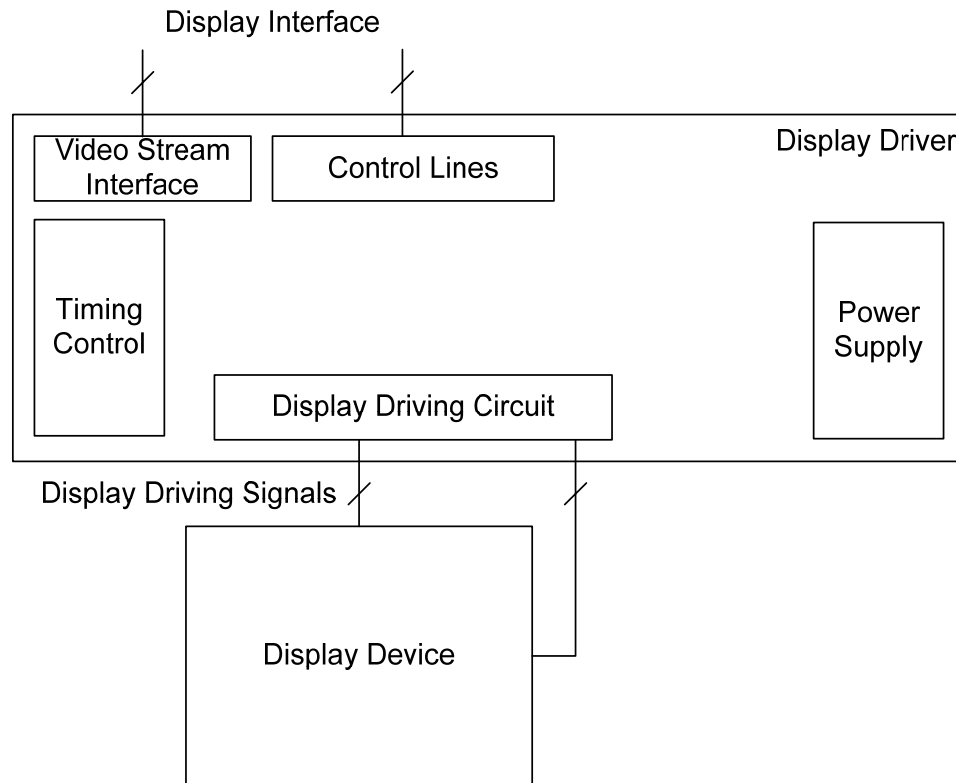
- 193 The Type 3 Display Architecture should consist of the following functional blocks:
- 194 Display Device. Used to show image data.
- 195 Display Driver. May be one or more devices used to drive the display device.
- 196 Registers. Used to configure the display module behavior and hold identification information; can
197 be integrated in the display driver.
- 198 Timing Controller. Provides timing signals to control the display device and display driver based
199 on configuration information; can be integrated in the display driver.
- 200 Non-volatile memory. Used to store default register and configuration values; can be integrated in
201 the display driver.
- 202 Control Interface. Provides the interface between the host processor and the display driver; can be
203 integrated in the display driver.
- 204 Display Driving Circuit. As a part of display driver, used to convert timing signals and voltages to
205 signals appropriate to drive the display device.
- 206 Power Supply. Used to convert system voltages to levels usable by the display device and display
207 driver; can be integrated in the display driver.
- 208 Video Stream Interface. Used to receive video image data and timing signals from the host
209 processor.



210
211

Figure 3 Type 3 Display Architecture Block Diagram

- 212 The Type 4 Display Architecture should consist of the following functional blocks
- 213 Display Device. Used to show image data.
- 214 Display Driver. May be one or more devices used to drive the display device.
- 215 Timing Controller. Provides timing signals to control the display device and display driver based
216 on configuration information; can be integrated in the display driver.
- 217 Control Lines. Used to receive display behavior control information from the host processor.
- 218 Display Driving Circuit. As a part of display driver, used to convert timing signals and voltages to
219 signals appropriate to drive the display device.
- 220 Power Supply. Used to convert system voltages to levels usable by the display device and display
221 driver; can be integrated in the display driver.
- 222 Video Stream Interface. Used to receive video image data and timing signals from the host
223 processor.



224

225

Figure 4 Type 4 Display Architecture Block Diagram

226 The power supply functional block should be controlled by the display driver for all applicable display
227 architectures.

228 DPI-2 specifies the video stream interface for Type 2, 3 and 4 display architectures in a parallel
229 implementation.

230 The control pins of the Type 4 display architecture shall be the control signals of DPI-2.

231 5 Display Pixel Interface Interoperability

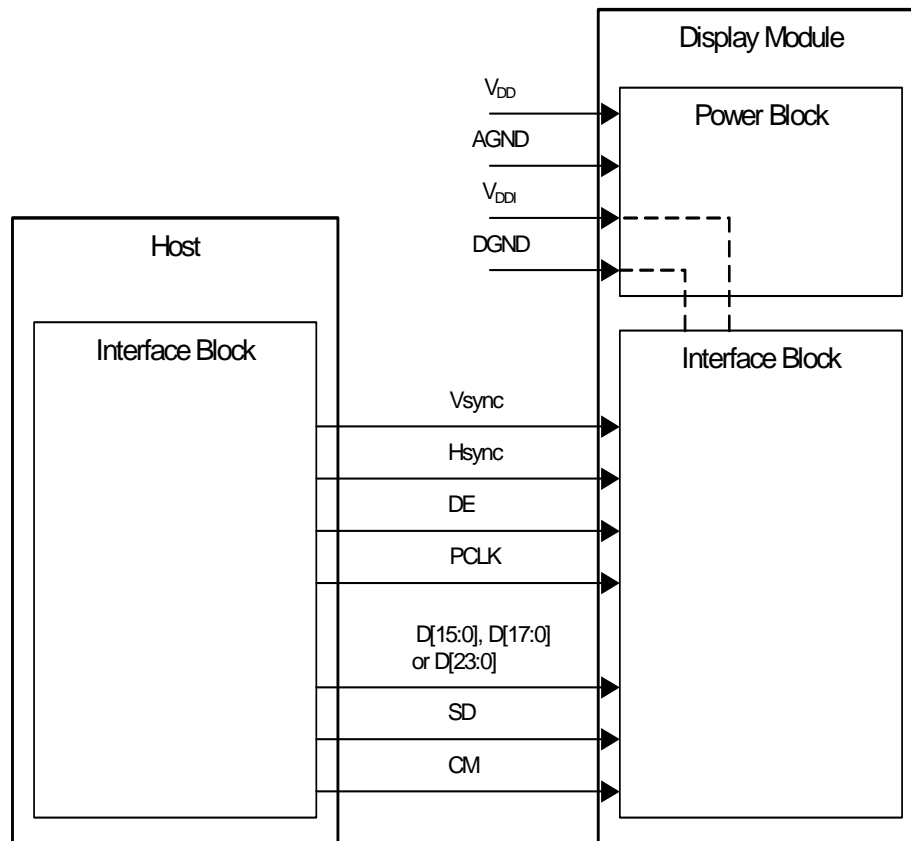
232 There are two types of electrical connections between the host processor and the display module.

233 • Power Signals. Power is supplied from either the host processor or from a power management unit
234 that is controlled by the host processor.

235 • Interface Signals. Pixel data, commands, and control information are transferred between the host
236 processor and display module using the interface signals.

237 The host processor interface shall implement a 24-bit data width and accompanying control and timing
238 signals, as specified in section 6. The host processor interface shall be capable of transferring data as 16-bit,
239 18-bit, or 24-bit words.

240 The display module interface shall be implemented with a 16-bit, 18-bit, or 24-bit data width.



241

242

Figure 5 DPI Interface Signals and Power Connections

243 The host processor shall support all control signals for Type 2, Type 3, and Type 4 display architectures as
244 shown in Figure 5. SD and CM are required control signals for Type 4 compliant display modules only.

245 Host processors shall support all timing parameter sets described in section 10. If a display module supports
246 a display resolution in section 10 then it shall support the timing parameters as described for that resolution.
247 Both the host processor and display module may operate over a range of values that include the given
248 timing parameters.

249 Manufacturers shall document a DPI-2 device's parameter ranges for the parameters listed in section 10.

250 **6 Interface Signal Description**251 **6.1 Power Supply Connections**252 **Table 1 Power supply connections**

Symbol	Name	Description
V _{DD}	Power supply	Power supply for display module
V _{DDI}	I/F logic level supply	Logic level supply for interface signals
AGND	Power Ground	Analog GND for display-panel power supply
DGND	Logic level ground	Logic GND for logic functions on display panel

253 **6.2 Interface Signals**254 **Table 2 Interface Signals for DPI**

Symbol	Name	I/O	Description
Vsync	Vertical sync	O	Vertical synchronization timing signal
Hsync	Horizontal sync	O	Horizontal synchronization timing signal
DE	Data enable	O	Data enable signal (assertion indicates valid pixels)
PCLK	Pixel Clock	O	Pixel clock for capturing pixels at display interface
D[15:0], D[17:0] or D[23:0]	Pixel Data	O	Pixel data in 16-bit, 18-bit, or 24-bit format
SD	Shutdown	O	Control pin to shut down display (used for Type 4 architecture only)
CM	Color Mode	O	Control pin for switching between normal color and reduced-color mode (used for Type 4 architecture only)

255 Note: I/O directions are defined from the host processor perspective

256 The host processor shall implement a 24-bit pixel-data bus width. The host processor interface can be
257 configured for 16-bit or 18-bit data bus width.

258 The display module shall implement a 16-bit, 18-bit or 24-bit pixel-data bus width.

259 7 Programmable Timing Parameters

260 In normal operation, systems based on DPI architecture rely on the host processor to continuously provide
 261 complete frames of image data at a sufficient frame rate to avoid flicker or other visible artifacts.

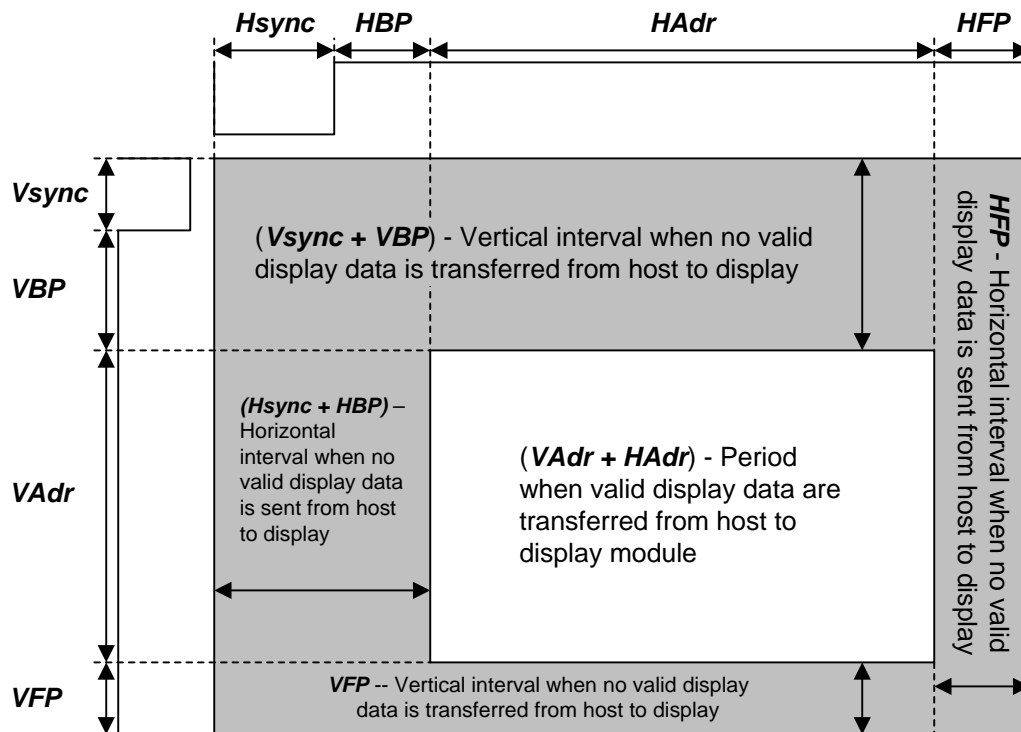
262 The displayed image, or *frame*, is comprised of a rectangular array of pixels. The frame is transmitted from
 263 the host processor to a display module as a sequence of pixels, with each horizontal line of the image data
 264 sent as a group of consecutive pixels.

265 Vsync indicates the beginning of each frame of the displayed image.

266 Hsync signals the beginning of each horizontal line of pixels.

267 Each pixel value (16-, 18-, or 24-bit data) is transferred from the host processor to the display module
 268 during one pixel period. The rising edge of PCLK is used by the display module to capture pixel data. Since
 269 PCLK runs continuously, control signal DE is required to indicate when valid pixel data is being
 270 transmitted on the pixel data signals.

271 Figure 6 defines timing parameters for DPI operation.



272

273

Figure 6 DPI Timing Parameters

274 Table 3 specifies requirements for DPI timing parameters. The host processor shall support the range
 275 specified in this table.

276

Table 3 DPI Programmable Parameters

Parameters	Symbols	Conditions	Min.	Step	Max.	Unit
Horizontal Synchronization	Hsync		1	1	-	PCLKCYC
Horizontal Back Porch	HBP		1	1	-	PCLKCYC
Horizontal Address	HAdr		176	1	800	PCLKCYC
Horizontal Front Porch	HFP		1	1	-	PCLKCYC
Vertical Synchronization	Vsync		1	1	-	Line
Vertical Back Porch	VBP		1	1	-	Line
Vertical Address	VAdr		208	1	480	Line
Vertical Front Porch	VFP		1	1	-	Line

277 Notes

- 278 1. Vertical period (one frame) shall be equal to the sum of Vsync + VBP + VAdr + VFP.
- 279 2. Horizontal period (one line) shall be equal to the sum of Hsync + HBP + HAdr + HFP.
- 280 3. Control signals PCLK and Hsync shall be transmitted as specified at all times while valid pixels
- 281 are transferred between the host processor and the display module.

282 **8 Interface Color Coding**

283 Table 4 specifies the mapping of data bits, as components of primary pixel color values R, G, and B, to
 284 signal lines at the interface. Host processors shall implement all color-coding configurations in Table 4.
 285 Peripherals shall implement one or more of the configurations in Table 4.

286

Table 4 Interface Color Coding

Signal Line	16-bit			18-bit		24-bit
	Configuration 1	Configuration 2	Configuration 3	Configuration 1	Configuration 2	
D23	(not used)	(not used)	(not used)	(not used)	(not used)	R7
D22	(not used)	(not used)	(not used)	(not used)	(not used)	R6
D21	(not used)	(not used)	R4	(not used)	R5	R5
D20	(not used)	R4	R3	(not used)	R4	R4
D19	(not used)	R3	R2	(not used)	R3	R3
D18	(not used)	R2	R1	(not used)	R2	R2
D17	(not used)	R1	R0	R5	R1	R1
D16	(not used)	R0	(not used)	R4	R0	R0
D15	R4	(not used)	(not used)	R3	(not used)	G7
D14	R3	(not used)	(not used)	R2	(not used)	G6
D13	R2	G5	G5	R1	G5	G5
D12	R1	G4	G4	R0	G4	G4
D11	R0	G3	G3	G5	G3	G3
D10	G5	G2	G2	G4	G2	G2
D9	G4	G1	G1	G3	G1	G1
D8	G3	G0	G0	G2	G0	G0
D7	G2	(not used)	(not used)	G1	(not used)	B7
D6	G1	(not used)	(not used)	G0	(not used)	B6
D5	G0	(not used)	B4	B5	B5	B5

Signal Line	16-bit			18-bit		24-bit
	Configuration 1	Configuration 2	Configuration 3	Configuration 1	Configuration 2	
D4	B4	B4	B3	B4	B4	B4
D3	B3	B3	B2	B3	B3	B3
D2	B2	B2	B1	B2	B2	B2
D1	B1	B1	B0	B1	B1	B1
D0	B0	B0	(not used)	B0	B0	B0

287 There are three mappings for 16-bit pixels to data signals, two mappings for 18-bit pixels to data signals,
 288 and one mapping for 24-bit pixels to data signals.

289 Notes:

- 290 1. Pixel values are specified as triplets for primary color components R, G, and B: R = Red, G =
 291 Green, B = Blue. R0 is the LSB for the red component, G0 is LSB for the green component, etc.
- 292 2. For 16-bit pixels, R primary color MSB is R4, R primary color LSB is R0; G primary color MSB
 293 is G5, G primary color LSB is G0; B primary color MSB is B4 and B primary color LSB is B0.
- 294 3. For 18-bit pixels, R primary color MSB is R5, R primary color LSB is R0; G primary color MSB
 295 is G5, G primary color LSB is G0; B primary color MSB is B5 and B primary color LSB is B0.
- 296 4. For 24-bit pixels, R primary color MSB is R7, R primary color LSB is R0; G primary color MSB
 297 is G7, G primary color LSB is G0; B primary color MSB is B7 and B primary color LSB is B0.

298 **9 Interface Electrical Characteristics**299 **9.1 Electrical Characteristics**300 **9.1.1 Absolute Maximum Ratings**

301

Table 5 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power Supply	V_{DD}	DOI (Depends on Implementation)	V
Logic Level Supply	V_{DDI}	DOI (Depends on Implementation)	V
Logic Signal Input Voltage	V_I	DOI (Depends on Implementation)	V
Logic Signal Output Voltage	V_O	DOI (Depends on Implementation)	V

302 **9.1.2 DC Characteristics**

303

Table 6 DC Characteristics

Parameter	Symbol	Condition	Specification			Unit
			min	typ	max	
Power Supply Voltage	V_{DD}	Operating Voltage		DOI		V
Logic High Level Input Voltage	V_{IH}		$0.7V_{DDI}$		V_{DDI}	V
Logic Low Level Input Voltage	V_{IL}		0.0		$0.3V_{DDI}$	V
Logic High Level Input Current	I_{IH}	Except D[15:0], D[17:0] or D[23:0]			10	μA
	I_{IHD}	D[15:0], D[17:0] or D[23:0]			10	μA
Logic Low Level Input Current	I_{IH}	Except D[15:0], D[17:0] or D[23:0]	-10			μA
	I_{IHD}	D[15:0], D[17:0] or D[23:0]	-10			μA

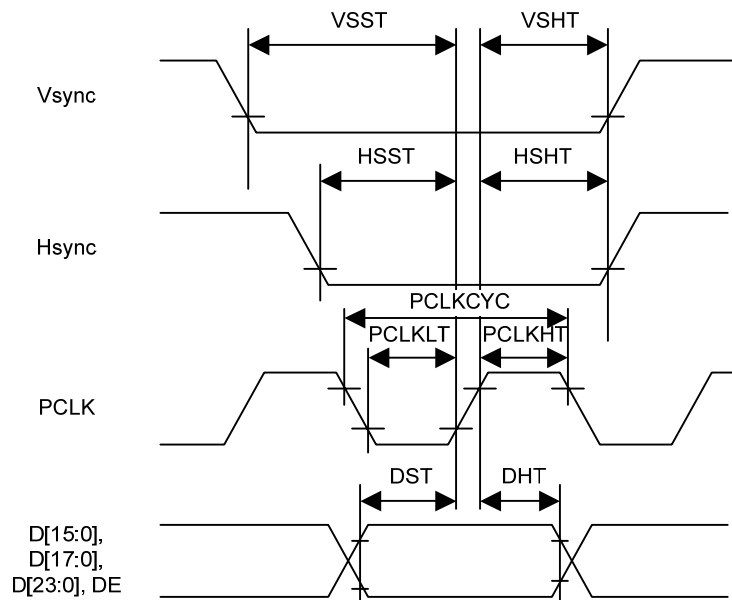
304 Note: $T_a = -30$ to 70 °C

305

Table 7 Logic Level Supply Voltage Classification

Parameter	Symbol	Class	Specification			Unit
			min	typ	max	
Logic Level Supply Voltage	V _{DDI}	1	1.1	1.2	1.3	V
		2	1.4	1.5	1.6	V
		3	1.7	1.8	1.9	V
		4	2.6	2.8	3.0	V

306 Note: Ta = -30 to 70 °C

307 **9.1.3 AC Characteristics**

308

309

310

Figure 7 DPI Signal Timings**Table 8 DPI-2 AC Characteristics**

Parameters	Symbols	Condition	Min.	Max.	Unit
Vsync Setup Time	VSST		T	-	ns
Vsync Hold Time	VSHT		T	-	ns
Hsync Setup Time	HSST		T	-	ns
Hsync Hold Time	HSHT		T	-	ns
Pixel Clock Duty Cycle		PCLKCYC	33	67	%

Parameters	Symbols	Condition	Min.	Max.	Unit
Pixel Clock Low Duration	PCLKLT		T	-	ns
Pixel Clock High Duration	PCLKHT		T	-	ns
Data Setup Time	DST		T	-	ns
Data Hold Time	DHT		T	-	ns

311 Note:

312 1. $T_a = -30$ to 70 °C, $V_{DDI} = 1.1V$ to $1.3V$, $1.4V$ to $1.6V$, $1.7V$ to $1.9V$, $2.6V$ to $3.0V$, $GND = 0V$

313 2. Signal rise and fall times are not included in these values.

314 3. See Table 9 for T-values.

315

Table 9 DPI-2 AC Characteristics, T-value

Total Number of Pixels	Representative Display	T	Unit
Up to 38,720 pixels	176(H)x220(V)	40	ns
Up to 76,800 pixels	240(H)x320(V)	20	ns
Up to 307,200 pixels	640(H)x480(V)	10	ns
Up to 384,000 pixels	800(H)x480(V)	5	ns

316 **10 DPI Timing Parameter Examples**

317 Table 10 through Table 16 provides examples of DPI timing parameters for typical display module sizes.

318 **Table 10 176 Horizontal x 208 Vertical Display Module**

Parameters	Symbols	Conditions	Min.	Typ	Max.	Unit
PCLK Cycle	PCLKCYC			401		ns
Horizontal Synchronization	Hsync			2		PCLKCYC
Horizontal Back Porch	HBP			8		PCLKCYC
Horizontal Address	HAdr		-	176	-	PCLKCYC
Horizontal Front Porch	HFP			10		PCLKCYC
Vertical Synchronization	Vsync			2		Line
Vertical Back Porch	VBP			1		Line
Vertical Address	VAdr		-	208	-	Line
Vertical Front Porch	VFP			30		Line
Vsync Setup Time	VSST	See Table 8 and Table 9.				
Vsync Hold Time	VSHT					
Hsync Setup Time	HSST					
Hsync Hold Time	HSHT					
Data Setup Time	DST					
Data Hold Time	DHT					
Vertical Frequency(*)						
Horizontal Frequency(*)				12.7		KHz
PCLK Frequency(*)				2.49		MHz

319 Note: * marked numbers are reference use only.

320

Table 11 176 Horizontal x 220 Vertical Display Module

Parameters	Symbols	Conditions	Min.	Typ	Max.	Unit
PCLK Cycle	PCLKCYC			379		ns
Horizontal Synchronization	Hsync			2		PCLKCYC
Horizontal Back Porch	HBP			8		PCLKCYC
Horizontal Address	HAdr		-	176	-	PCLKCYC
Horizontal Front Porch	HFP			10		PCLKCYC
Vertical Synchronization	Vsync			2		Line
Vertical Back Porch	VBP			1		Line
Vertical Address	VAdr		-	220	-	Line
Vertical Front Porch	VFP			1		Line
Vsync Setup Time	VSST	See Table 8 and Table 9.				
Vsync Hold Time	VSHT					
Hsync Setup Time	HSST					
Hsync Hold Time	HSHT					
Data Setup Time	DST					
Data Hold Time	DHT					
Vertical Frequency(*)						
Horizontal Frequency(*)				13.5		KHz
PCLK Frequency(*)				2.64		MHz

321 Note: * marked numbers are reference use only.

322

Table 12 240 Horizontal x 320 Vertical Display Module

Parameters	Symbols	Conditions	Min.	Typ	Max.	Unit
PCLK Cycle	PCLKCYC			184		ns
Horizontal Synchronization	Hsync			10		PCLKCYC
Horizontal Back Porch	HBP			20		PCLKCYC
Horizontal Address	HAdr		-	240	-	PCLKCYC
Horizontal Front Porch	HFP			10		PCLKCYC
Vertical Synchronization	Vsync			2		Line
Vertical Back Porch	VBP			2		Line
Vertical Address	VAdr		-	320	-	Line
Vertical Front Porch	VFP			2		Line
Vsync Setup Time	VSST	See Table 8 and Table 9.				
Vsync Hold Time	VSHT					
Hsync Setup Time	HSST					
Hsync Hold Time	HSHT					
Data Setup Time	DST					
Data Hold Time	DHT					
Vertical Frequency(*)						
Horizontal Frequency(*)				19.43		KHz
PCLK Frequency(*)				5.44		MHz

323 Note: * marked numbers are reference use only.

324

Table 13 320 Horizontal x 240 Vertical Display Module

Parameters	Symbols	Conditions	Min.	Typ	Max.	Unit
PCLK Cycle	PCLKCYC			172		ns
Horizontal Synchronization	Hsync			10		PCLKCYC
Horizontal Back Porch	HBP			20		PCLKCYC
Horizontal Address	HAdr		-	320	-	PCLKCYC
Horizontal Front Porch	HFP			40		PCLKCYC
Vertical Synchronization	Vsync			2		Line
Vertical Back Porch	VBP			2		Line
Vertical Address	VAdr		-	240	-	Line
Vertical Front Porch	VFP			4		Line
Vsync Setup Time	VSST	See Table 8 and Table 9.				
Vsync Hold Time	VSHT					
Hsync Setup Time	HSST					
Hsync Hold Time	HSHT					
Data Setup Time	DST					
Data Hold Time	DHT					
Vertical Frequency(*)						
Horizontal Frequency(*)				14.9		KHz
PCLK Frequency(*)				5.8		MHz

325 Note: * marked numbers are reference use only.

326

Table 14 480 Horizontal x 640 Vertical Display Module

Parameters	Symbols	Conditions	Min.	Typ	Max.	Unit
PCLK Cycle	PCLKCYC			50		ns
Horizontal Synchronization	Hsync			8		PCLKCYC
Horizontal Back Porch	HBP			8		PCLKCYC
Horizontal Address	HAdr		-	480	-	PCLKCYC
Horizontal Front Porch	HFP			24		PCLKCYC
Vertical Synchronization	Vsync			2		Line
Vertical Back Porch	VBP			2		Line
Vertical Address	VAdr		-	640	-	Line
Vertical Front Porch	VFP			4		Line
Vsync Setup Time	VSST	See Table 8 and Table 9.				
Vsync Hold Time	VSHT					
Hsync Setup Time	HSST					
Hsync Hold Time	HSHT					
Data Setup Time	DST					
Data Hold Time	DHT					
Vertical Frequency(*)						
Horizontal Frequency(*)				38.5		KHz
PCLK Frequency(*)				20		MHz

327 Note: * marked numbers are reference use only.

328

Table 15 640 Horizontal x 480 Vertical Display Module

Parameters	Symbols	Conditions	Min.	Typ	Max.	Unit
PCLK Cycle	PCLKCYC			47.8		ns
Horizontal Synchronization	Hsync			8		PCLKCYC
Horizontal Back Porch	HBP			8		PCLKCYC
Horizontal Address	HAdr		-	640	-	PCLKCYC
Horizontal Front Porch	HFP			44		PCLKCYC
Vertical Synchronization	Vsync			2		Line
Vertical Back Porch	VBP			2		Line
Vertical Address	VAdr		-	480	-	Line
Vertical Front Porch	VFP			4		Line
Vsync Setup Time	VSST	See Table 8 and Table 9.				
Vsync Hold Time	VSHT					
Hsync Setup Time	HSST					
Hsync Hold Time	HSHT					
Data Setup Time	DST					
Data Hold Time	DHT					
Vertical Frequency(*)						
Horizontal Frequency(*)				29.3		KHz
PCLK Frequency(*)				21		MHz

329 Note: * marked numbers are reference use only.

330

Table 16 800 Horizontal x 480 Vertical Display Module

Parameters	Symbols	Conditions	Min.	Typ	Max.	Unit
PCLK Cycle	PCLKCYC			44.4		ns
Horizontal Synchronization	Hsync			10		PCLKCYC
Horizontal Back Porch	HBP			15		PCLKCYC
Horizontal Address	HAdr		-	800	-	PCLKCYC
Horizontal Front Porch	HFP			15		PCLKCYC
Vertical Synchronization	Vsync			2		Line
Vertical Back Porch	VBP			2		Line
Vertical Address	VAdr		-	480	-	Line
Vertical Front Porch	VFP			4		Line
Vsync Setup Time	VSST	See Table 8 and Table 9.				
Vsync Hold Time	VSHT					
Hsync Setup Time	HSST					
Hsync Hold Time	HSHT					
Data Setup Time	DST					
Data Hold Time	DHT					
Vertical Frequency(*)						
Horizontal Frequency(*)				26.8		KHz
PCLK Frequency(*)				22.6		MHz

331 Note: * marked numbers are reference use only.

332 **11 Type 2 and Type 3 Display Architecture Control Interfaces**

333 The DBI Type C interface shall be used for Type 2 and Type 3 display architectures. See *MIPI Alliance*
334 *Standard for Display Bus Interface* [2] for descriptions of the supported control interfaces.

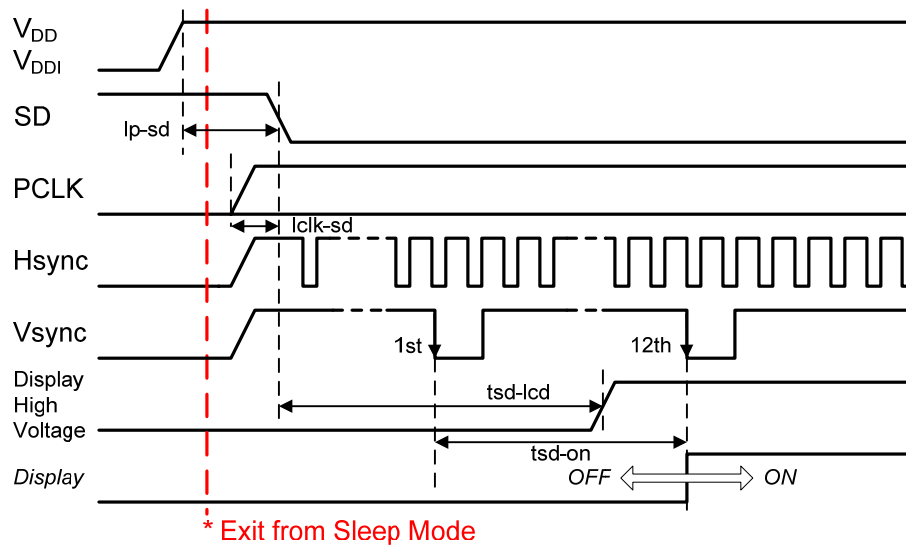
335 12 Type 4 Architecture Shutdown and Color Mode Signals

336 12.1 Shutdown for Type 4 Architecture

337 The Shutdown signal, SD, is used to turn on or turn off the display module.

338 When SD is asserted high, the host processor should stop the video stream data to the display module to
 339 reduce interface signal power consumption. PCLK may also be turned off to further reduce power
 340 consumption.

341 The display module may reduce its power consumption by switching off its internal circuits. The control
 342 interface shall remain powered on.



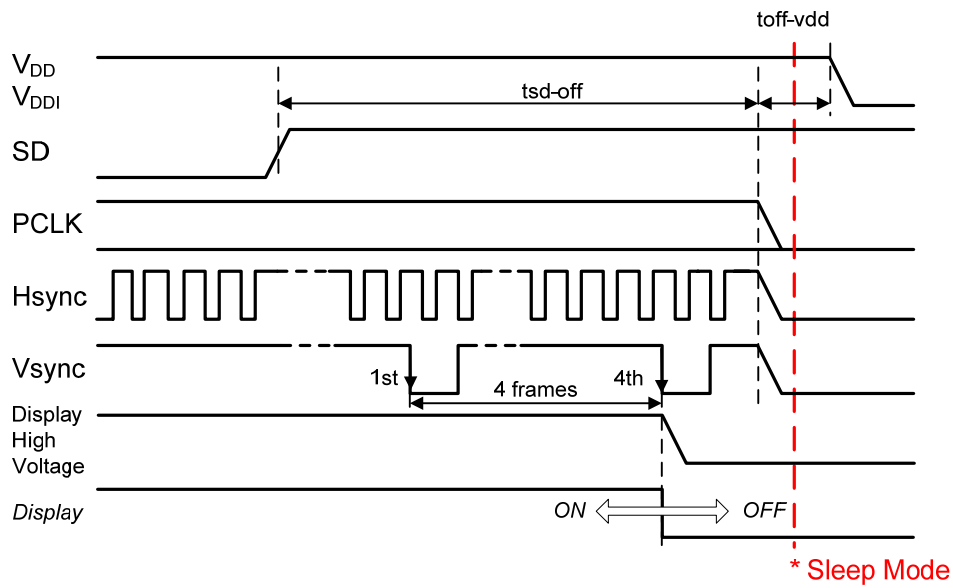
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344 **Figure 8 Power-on and Shutdown Recovery Sequence**

345

Table 17 AC timing for power-on sequence and recovery sequence from shutdown

Parameters	Symbols	Condition	Min.	Typ.	Max.	Unit
V_{DD}/V_{DDI} – on to falling edge of SD	t_{p-sd}		1	-	-	ms
PCLK input to the falling edge of SD	t_{clk-sd}		1	-	-	PCLKCYC
Falling edge of SD to display start	t_{sd-on}		-	12	-	Vertical period



346

347

Figure 9 Power-off and Shutdown Sequence

348

Table 18 AC Timing for power-off sequence and shutdown sequence

Parameters	Symbols	Condition	Min.	Typ.	Max.	Unit
Rising edge of SD to display off	tsd-off		4	-	-	Vertical period
Input-signal-off to V_{DD}/V_{DDI} off	toff-vdd		0	-	-	μ s

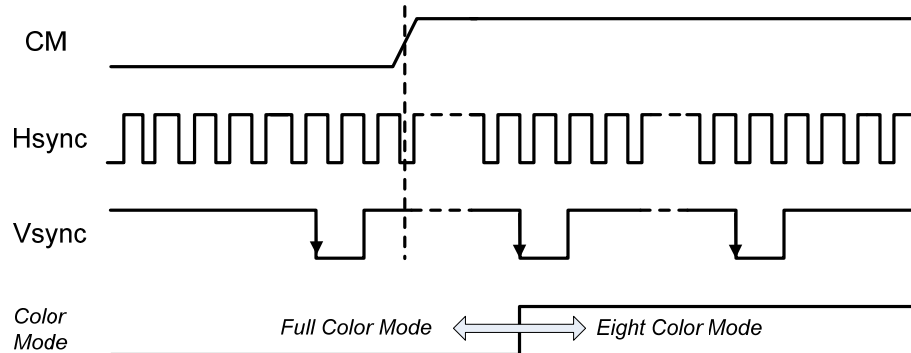
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350 **12.2 Color Mode for Type 4 Architecture**

351 The Color Mode signal, CM, is used to change the displayed number of colors.

352 When CM is asserted high, the display module shall show the image data using eight colors, MSB for each
353 R, G, and B color components. All unnecessary circuits on the display module may be stopped at the same
354 time to reduce display module power consumption.

355 The color mode change sequences are shown in Figure 10 and Figure 11.

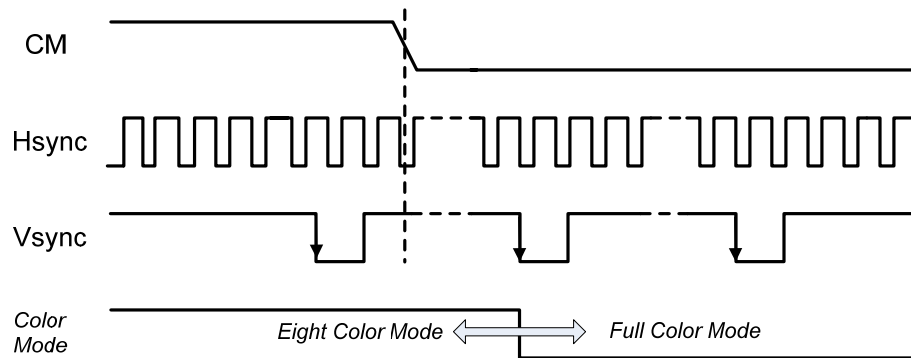


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Figure 10 Full-color to 8-color Mode Transition Sequence

358 Transition from full-color mode to 8-color mode shall occur on the Vsync following a low-to-high
359 transition on CM.



360

361

Figure 11 8-color to Full-color Mode Transition Sequence

362 Transition from 8-color mode to full-color mode shall occur on the Vsync following a high-to-low
363 transition on CM.

364 **13 Command Set**

365 A host processor shall implement all commands specified in *MIPI Alliance Standard for Display Command*
366 *Set* [1].

367 A display module shall implement the commands specific to the display architecture, Type 2 or Type 3, as
368 defined in *MIPI Alliance Standard for Display Command Set* [1].