Physical Layers: M-PHY®, D-PHY, C-PHY

Overview

MIPI Alliance provides a set of specialized physical layers with both complementary and unique features to support a wide variety of application protocols requiring high performance, low-power serial interfaces. MIPI defines camera, display, and chip-to-chip protocol Specifications that each support M-PHY, D-PHY and/or C-PHY; MIPI also cooperates closely with independent partner organizations to create widely adopted industry specifications that use M-PHY.

Each physical layer offers unique advantages and features that collectively address every important aspect of today's integrated handheld mobile devices.

M-PHY (v3.1, June 2014)

M-PHY is an embedded clock serial interface technology with ultra-high bandwidth capabilities, specifically developed for the extreme performance and low power requirements of mobile applications. It's designed for next generation point-to-point interfaces and high speed component networks using dual simplex architectures. M-PHY currently supports seven different protocols, from advanced cameras to high speed memory, where low pin count, lane scalability and power efficiency are paramount requirements. By transmitting in long or short bursts, M-PHY adapts to a wide range of requirements while minimizing power consumption. Additionally, it operates over various media types, including optical interconnects, by supporting Media Converters.

D-PHY (v1.2, September 2014)

D-PHY is a serial interface technology using differential signaling for band-limited channels with scalable data lanes and a source synchronous clock to support power efficient interfaces for streaming applications such as displays and cameras. It offers half-duplex behavior for applications that benefit from bidirectional communication at transmission rates up to 2.5 Gigabit per lane.

C-PHY (v1.0, October 2014)

C-PHY requires few conductors, does not require a separate clock lane, and provides flexibility to assign individual lanes in any combination to any port on the application processor via software control. Due to similarities in basic electrical specifications, C-PHY and D-PHY can be implemented on the same device pins. 3-phase symbol encoding technology delivers approximately 2.28 bits per symbol over a three-wire group of conductors per lane. This enables higher data rates at a lower toggling frequency, further reducing power.

FEATURES

Target Applications

- Mobile Applications
- Camera
- Display
- Chip-to-chip Interconnect
- Storage
- Memory

Key Features

- Low Power
- Low Pin Count
- Minimize interference
- Optional support for optical interconnects (M-PHY)

Key Benefits

- High Performance
- High Scalability
- High Bandwidth
- Unprecedented Flexibility

Support by the Industry

- Shipping in millions of mobile products
- JEDEC Universal Flash Storage
- Mobile PCIexpress
- USB SSIC

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PHY Characteristics

Characteristic	M-PHY v3.1	D-PHY v1.2	C-PHY v1.0
Primary use case	Performance driven, bidirectional packet/ network oriented interface	Efficient unidirectional streaming interface, with low speed in-band reverse channel	Efficient unidirectional streaming interface, with low speed in-band reverse channel
HS clocking method	Embedded Clock	DDR Source-Sync Clock	Embedded Clock
Channel compensation	Equalization	Data skew control relative to clock	Encoding to reduce data toggle rate
Minimum configuration and pins	1 lane per direction, dual-simplex, 2 pins each (4 total)	1 lane plus clock, simplex, 4 pins	1 lane (trio), simplex, 3 pins
Maximum transmitter swing amplitude	SA: 250mV (peak) LA: 500mV (peak)	LP: 1300mV (peak) HS: 360mV (peak)	LP: 1300mV (peak) HS: 425mV (peak)
Data rate per lane (HS)	HS-G1: 1.25, 1.45 Gb/s HS-G2: 2.5, 2.9 Gb/s HS-G3: 5.0, 5.8 Gb/s (Line rates are 8b10b encoded)	80 Mbps to ~2.5 Gbps (aggregate)	80 Msym/s to 2.5 Gsym/s times 2.28 bits/sym, or max 5.7 Gbps (aggregate)
Data rate per lane (LS)	10kbps – 600 Mbps	< 10 Mbps	< 10 Mbps
Bandwidth per Port (3 or 4 lanes)	~ 4.0 – 18.6 Gb/s (aggregate BW)	Max ~10 Gbps per 4-lane port (aggregate)	Max ~ 17.1 Gbps per 3-lane port (aggregate)
Typical pins per Port (3 or 4 lanes)	10 (4 lanes TX, 1 lane RX)	10 (4 lanes, 1 lane clock)	9 (3 lanes)