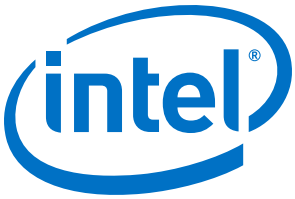


ALTERA_CORDIC IP Core User Guide

UG-20017
2017.05.08

Subscribe

Send Feedback

Contents

1 ALTERA_CORDIC IP Core User Guide..... 3
1.1 ALTERA_CORDIC IP Core Features..... 3
1.2 DSP IP Core Device Family Support..... 3
1.3 ALTERA_CORDIC IP Core Functional Description..... 4
1.3.1 SinCos Function..... 5
1.3.2 Atan2 Function..... 5
1.3.3 Vector Translate Function..... 6
1.3.4 Vector Rotate Function..... 6
1.4 ALTERA_CORDIC IP Core Parameters..... 7
1.5 ALTERA_CORDIC IP Core Signals..... 9

1 ALTERA_CORDIC IP Core User Guide

Use the ALTERA_CORDIC IP core to implement a set of fixed-point functions with the CORDIC algorithm.

ALTERA_CORDIC IP Core Features on page 3

DSP IP Core Device Family Support on page 3
ALTERA_CORDIC IP Core Functional Description on page 4
ALTERA_CORDIC IP Core Parameters on page 7
ALTERA_CORDIC IP Core Signals on page 9

1.1 ALTERA_CORDIC IP Core Features

- Supports fixed-point implementations.
- Supports both latency and frequency driven IP cores.
- Supports both VHDL and Verilog HDL code generation.
- Produces fully unrolled implementations.
- Produces faithfully rounded results to either of the two closest representable numbers in the output.

1.2 DSP IP Core Device Family Support

Intel offers the following device support levels for Intel FPGA IP cores:

Intel Corporation. All rights reserved. Intel, the Intel logo, Altera, Arria, Cyclone, Enpirion, MAX, Nios, Quartus and Stratix words and logos are trademarks of Intel Corporation or its subsidiaries in the U.S. and/or other countries. Intel warrants performance of its FPGA and semiconductor products to current specifications in accordance with Intel's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Intel assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Intel. Intel customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.
*Other names and brands may be claimed as the property of others.

ISO 9001:2008 Registered

- Advance support—the IP core is available for simulation and compilation for this device family. FPGA programming file (`.pof`) support is not available for Quartus Prime Pro Stratix 10 Edition Beta software and as such IP timing closure cannot be guaranteed. Timing models include initial engineering estimates of delays based on early post-layout information. The timing models are subject to change as silicon testing improves the correlation between the actual silicon and the timing models. You can use this IP core for system architecture and resource utilization studies, simulation, pinout, system latency assessments, basic timing assessments (pipeline budgeting), and I/O transfer strategy (data-path width, burst depth, I/O standards tradeoffs).
- Preliminary support—Intel verifies the IP core with preliminary timing models for this device family. The IP core meets all functional requirements, but might still be undergoing timing analysis for the device family. You can use it in production designs with caution.
- Final support—Intelverifies the IP core with final timing models for this device family. The IP core meets all functional and timing requirements for the device family. You can use it in production designs.

Table 1. DSP IP Core Device Family Support

Device Family	Support
Arria® II GX	Final
Arria II GZ	Final
Arria V	Final
Intel® Arria 10	Final
Cyclone® IV	Final
Cyclone V	Final
Intel MAX® 10 FPGA	Final
Stratix® IV GT	Final
Stratix IV GX/E	Final
Stratix V	Final
Intel Stratix 10	Advance
Other device families	No support

1.3 ALTERA_CORDIC IP Core Functional Description

SinCos Function on page 5
Computes the sine and cosine of angle *a*.

Atan2 Function on page 5
Computes the function atan2(*y*, *x*) from inputs y and x.

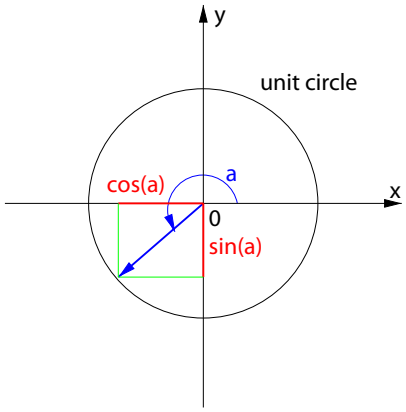
Vector Translate Function on page 6
The vector translate function is an extension of the atan2 function. It outputs the magnitude of the input vector and the angle *a*=atan2(*y*,*x*).

Vector Rotate Function on page 6
The vector rotate function takes a vector $v = (x,y)^T$ given by the two coordinates *x* and *y* and an angle *a*. The function produces a similarity rotation of vector *v* by the angle *a* to produce the vector $v0=(x0,y0)^T$.

1.3.1 SinCos Function

Computes the sine and cosine of angle *a*.

Figure 1. SinCos Function



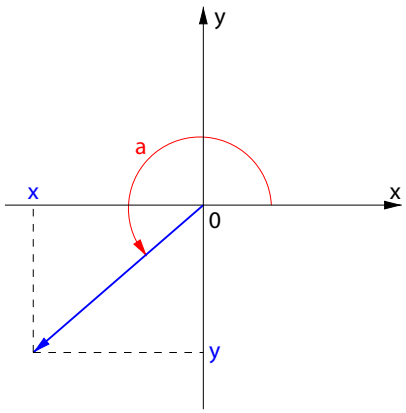
The function supports two configurations, depending on the sign attribute of *a*:

- If *a* is signed, the allowed input range is [-π,+π] and the output range for the sine and cosine is □[−1,1].
- If *a* is unsigned, the IP core restricts the input to [0,+π/2] and restricts the output range to [0,1].

1.3.2 Atan2 Function

Computes the function atan2(*y*, *x*) from inputs y and x.

Figure 2. Atan2 Function

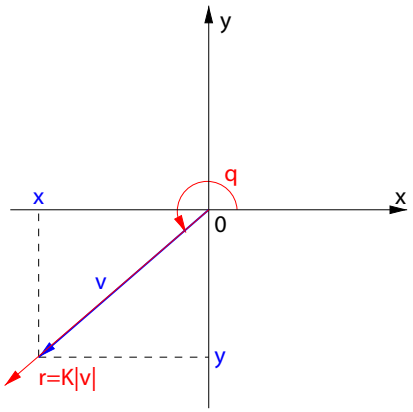


- If *x* and *y* are signed, the IP core determines the input range from the fixed-point formats.
- The output range is [-π,+π].

1.3.3 Vector Translate Function

The vector translate function is an extension of the atan2 function. It outputs the magnitude of the input vector and the angle a=atan2(y,x).

Figure 3. Vector Translate Function



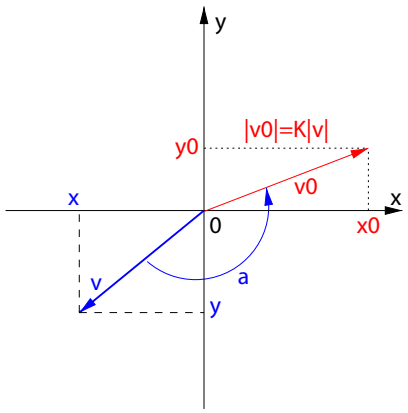
The function takes inputs x and y and outputs a=atan2(y, x) and $M = K(x^2+y^2)^{0.5}$. M is the magnitude of the input vector $v=(x,y)^T$, scaled by a CORDIC specific constant that converges to 1.646760258121, which is transcendental, hence has no fixed value. The functions supports two configurations, depending on the sign attribute of x and y:

- If the inputs are signed, the formats give the allowed input range. In this configuration the output range for a is□[$-\pi,+\pi$]. The output range for M depends on the input range of x and y, according with the magnitude formula.
- If the inputs are unsigned, the IP core restricts the output value for a [0,+π/2]. The magnitude value still depends on the formula.

1.3.4 Vector Rotate Function

The vector rotate function takes a vector $v= (x,y)^T$ given by the two coordinates x and y and an angle a. The function produces a similarity rotation of vector v by the angle a to produce the vector $v0=(x0,y0)^T$.

Figure 4. Vector Rotate Function



The rotation is a similarity rotation because the magnitude of the produced vector *v0* is scaled up by the CORDIC specific constant K(˜1.646760258121). The equations of the coordinates for vector *v*0 are:

- $x0 = K(x\cos(a) - y\sin(a))$
- $y0 = K(x\sin(a) + y\cos(a))$

If you set the sign attribute to true for the *x*,*y* inputs for the function, the IP core restricts their range to [−1,1]. You provide the number of fractional bits. The input angle *a* is allowed in the range [−π,+π], and has the same number of fractional bits as the other inputs. You provide the output fractional bits and the total width of the output is *w*=*wF*+3, signed. For unsigned inputs *x*,*y*, the IP core restricts the range to [0,1], the angle *a* to [0,π].

1.4 ALTERA_CORDIC IP Core Parameters

Table 2. SinCos Parameters

Parameter	Values	Description
Input data widths		
Fraction F	1 to 64	Number of fraction bits.
Width w	Derived	Width of fixed-point data.
Sign	signed or unsigned	The sign of the fixed-point data.
Output data widths		
Fraction	1 to 64, where $F_{OUT} \leq F_{IN}$	Number of fraction bits.
Width	Derived	Width of fixed-point data.
Sign	Derived	The sign of the fixed-point data.
Generate enable port	On or off	Turn on for `enable` signal.

Table 3. Atan2 Parameters

Parameter	Values	Description
Input data widths		
Fraction	1 to 64	Number of fraction bits.
Width	3 to 64	Width of fixed-point data.
Sign	signed or unsigned	The sign of the fixed-point data.
Output data widths		
Fraction		Number of fraction bits.
Width	Derived	Width of fixed-point data.
Sign	Derived	The sign of the fixed-point data.

continued...

Parameter	Values	Description
Generate enable port	On or off	Turn on for enable signal.
LUT Size Optimization		Turn on to move some of the typical CORDIC operations into look up tables to reduce implementation cost.
Manually Specify LUT Size		Turn on to input the LUT size. Larger values (9-11) enable mapping some computations to memory blocks Only when **LUT Size Optimization** is on..

Table 4. Vector Translate Parameters

Parameter	Values	Description
Input data widths		
Fraction	1 to 64	Number of fraction bits.
Width	Signed: 4 to 64; unsigned: F to 65	Width of fixed-point data.
Sign	signed or unsigned	The sign of the fixed-point data
Output data widths		
Fraction	1 to 64	Number of fraction bits.
Width	Derived	Width of fixed-point data.
Sgn	Derived	The sign of the fixed-point data
Generate enable port	On or off	Turn on for enable signal.
Scale factor compensation	On or off	For vector translate, a CORDIC specific constant that converges to 1.6467602... scales the magnitude of the vector $(x^2+y^2)^{0.5}$ so that the value for the magnitude, *M*, is M = $K(x^2+y^2)^{0.5}$. The format of the output depends on the input format. The largest output value occurs when both the inputs are equal to the maximum representable input value, *j*. In this context: $M = K(j^2+j^2)^{0.5}$ $= K(2j^2)^{0.5}$ $= K2^{0.5}(j^2)^{0.5}$ $=K\ 2^{0.5}j \sim 2.32j$ Therefore, two extra bits left of the MSB of *j* are required to ensure *M* is representable. If scale factor compensation is selected, *M* becomes: $M = j^{0.5} \sim 1.41$ j One extra bit is sufficient for representing the range of *M*. Scale factor compensation affects the total width of the output.

Table 5. Vector Rotate Parameters

Parameter	Values	Description
Input data widths		
X,Y inputs		
Fraction	1 to 64	Number of fraction bits.
Width	Derived	Width of fixed-point data.
Sign	signed or unsigned	The sign of the fixed-point data.

continued...

Parameter	Values	Description
Angle input		
Fraction	Derived	-
Width	Derived	-
Sign	Derived	-
Output data widths		
Fraction	1 to 64	Number of fraction bits.
Width	Derived	Width of fixed-point data.
Sign	Derived	The sign of the fixed-point data
Generate enable port	On or off	Turn on for `enable` signal.
Scale factor compensation		Turn on to compensate the CORDIC-specific constant on the magnitude output. For both signed and unsigned inputs, turning on decreases by 1 the weight of the magnitude for `x0` and `y0`. The outputs belong to the interval $[-2^{0.5}, +2^{0.5}]K$. Under default settings, the output interval will therefore be $[-2^{0.5}K , +2^{0.5}K]$ (with $K \sim 1.6467602...$), or $\sim[-2.32, +2.32]$. Representing the values in this interval requires 3 bits left of the binary point, one of which is for the sign. When you turn on **Scale factor compensation**, the output interval becomes $[-2^{0.5}, +2^{0.5}]$ or $\sim[-1.41, 1.41]$, which requires two bits left of the binary point, one of which is for the sign. Scale factor compensation affects the total width of the output.

1.5 ALTERA_CORDIC IP Core Signals

Table 6. Common Signals

Name	Type	Description
clk	Input	Clock.
en	Input	Enable. Only available when you turn on **Generate an enable port**.
areset	Input	Reset.

Table 7. Sin Cos Function Signals

Name	Type	Configuration	Range	Description
a	Input	Signed input	$[-\pi,+\pi]$	Specifies the number of fractional bits (F_{IN}). The total width of this input is F_{IN}+3.Two extra bits are for the range (representing π) and one bit for the sign. Provide the input in two's complement form.
		Unsigned input	$[0,+\pi/2]$	Specifies the number of fractional bits (F_{IN}). The total width of this input is $w_{IN}=F_{IN}+1$. The one extra bit accounts for the range (required to represent π/2).
s, c	Output	Signed input	$[-1,1]$	Computes sin(a) and cos(a) on a user-specified output fraction width(F). The output has width $w_{OUT}= F_{OUT}+2$ and is signed.
		Unsigned input	$[0,1]$	Computes sin(a) and cos(a) on a user-specified output fraction width(F_{OUT}). The output has the width $w_{OUT}= F_{OUT}+1$ and is unsigned.

Table 8. Atan2 Function Signals

Name	Type	Configuration	Range	Details
x, y	Input	Signed input	Given by *w*, *F*	Specifies the total width (*w*) and number fractional bits (*F*) of the input. Provide the inputs in two's complement form.
		Unsigned input		Specifies the total width (*w*) and number fractional bits (*F*) of the input.
a	Ouput	Signed input	$[-\pi,+\pi]$	Computes atan2(y,x) on a user-specified output fraction width (*F*). The output has the width $w_{OUT}= F_{OUT}+2$ and is signed.
		Unsigned input	$[0,+\pi/2]$	Computes atan2(y,x) on output fraction width (F_{OUT}). The output format has the width $w_{OUT} = F_{OUT}+2$ and is signed. However, the output value is unsigned.

Table 9. Vector Translate Functions Signals

Name	Direction	Configuration	Range	Details
x, *y*	Input	Signed input	Given by *w*, *F*	Specifies the total width (*w*) and number fractional bits (*F*) of the input. Provide the inputs in two's complement form.
q	Output		$[-\pi,+\pi]$	Computes atan2(y,x) on a user-specified output fraction width F_q. The output has the width $w_q=F_q+3$ and is signed.
r			Given by *w*, *F*	Computes $K(x^2+y^2)^{0.5}$. The total width of the output is $w_r=F_q+3$, or $w_r=F_q+2$ with scale factor compensation. The number of meaningful bits depends on the number of iterations which depends on F_q. The format of the output depends on the input format. $MSB(M_{OUT})=MSB_{IN}+2$, or $MSB(M_{OUT})=MSB_{IN}+1$ with scale factor compensation
x, y	Input	Unsigned input	Given by *w*,*F*	Specifies the total width (*w*) and number fractional bits (*F*) of the input.
q	Output		$[0,+\pi/2]$	Computes atan2(y,x) on an output fraction width F_q. The output has the width $w_q=F_q+2$ and is signed.
r			Given by *w*,*F*	Computes $K(x^2+y^2)^{0.5}$. The total width of the output is $w_r=F_q+3$, or $w_r=F_q+2$ with scale factor compensation. $MSB(M_{OUT})=MSB_{IN}+2$, or $MSB(M_{OUT})=MSB_{IN}+1$ with scale factor compensation.

Table 10. Vector Rotate Function Signals

Name	Direction	Configuration	Range	Details
x, y	Input	Signed input	$[-1,1]$	Specifies the fraction width (*F*), total number of bits is *w* = *F*+2. Provide the inputs in two's complement form.
		Unsigned input	$[0,1]$	Specifies the fraction width (*F*), total number of bits is *w* = *F*+1.
a	Input	Signed input	$[-\pi,+\pi]$	Number of fractional bits is *F* (provided previously for x and y), total width is w_a = *F*+3.

continued...

Name	Direction	Configuration	Range	Details
		Unsigned input	$[0,+\pi]$	Number of fractional bits is F (provided previously for x and y), total width is $w_a = F+2$.
x0, y0	Output	Signed input	$[-2^{0.5},+2^{0.5}]K$	Number of fractional bits F_{OUT}, where $w_{OUT} = F_{OUT}+3$ or $w_{OUT} = F_{OUT}+2$ with scale factor reduction.
		Unsigned input		