# *Metastable Response in 5-V Logic Circuits*

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## Abstract

This application report describes metastable response in digital circuits. After defining the phenomenon itself, this report describes a test circuit with which the response can be analyzed and gives test results. Using examples, the influence of metastability on the response of asynchronous circuits and measures for improving reliability are assessed.

## 1 Introduction

Designers of digital systems are constantly confronted with the problem of synchronizing two systems that operate at different frequencies. The problem is usually resolved by synchronizing one of the signals with the local clock generator using a flip-flop. But such a solution, of necessity, leads to a violation of the operating conditions for the flip-flops as defined in the data sheets, i.e., in these cases, the setup time and hold time are not maintained. Therefore, a flip-flop can go into a metastable state, endangering the operability of the circuit and, thereby, the reliability of the whole system. The purpose of this report is, first, to acquaint designers with the phenomenon of metastability in dynamic circuits (flip-flops) and, second, to look at test results on the more common bipolar, CMOS, and BiCMOS circuit families. Using these data the designer can determine the influence of metastable states in an application and take any necessary countermeasures.

## 2 Definition of Metastable State

Figure 1 illustrates the internal circuitry of a master/slave D-type flip-flop. Only those parts are shown that are of interest for the purpose of this application report. If there is a low on the CLK input, the emitters of transistors Q1 and Q2 (master flip-flop) go high so that they are turned off. By way of the D input, depending on the logic level applied here, there also is high potential on one of the two bases of the transistors. A positive edge on the CLK input means that, first, gates G2 and G3 are disabled. As a result of hole-storage effects, the outputs of these gates can maintain their output voltage for a certain time. At the same time, the emitters of the transistors go low. The transistor on whose base the higher voltage appeared conducts, while the other transistor remains turned off. The flip-flop composed of the two transistors is held in this stable state by feedback resistors R1 and R2. At the same time, the slave flip-flop consisting of gates G4 and G5 is set to the new state and the new level appears on the Q outputs.

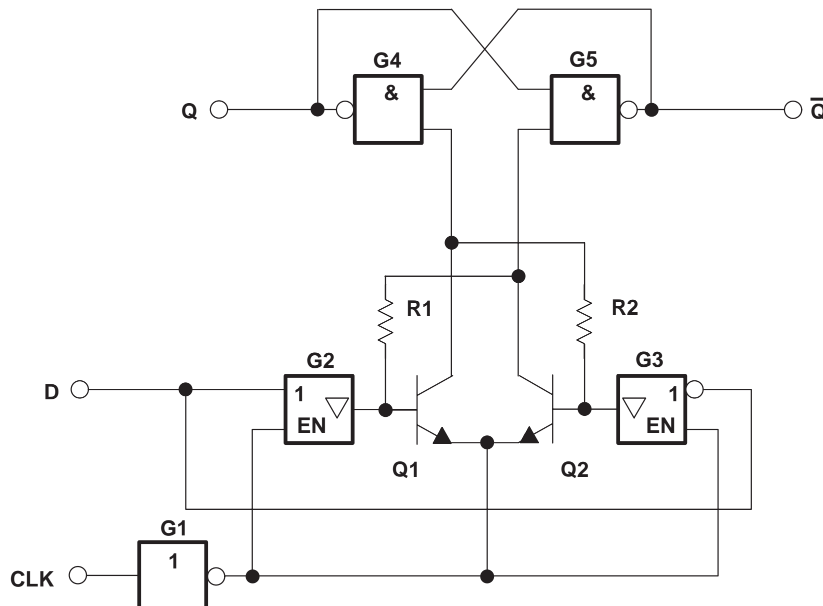


**Figure 1. Bipolar Master-Slave D-Type Flip-Flop**

Flip-flop operation, as described here, can only be ensured if the setup time and the hold time on the D input are maintained (see Figure 2). This means that for a short time before the positive edge on the CLK input (setup time) and a short time afterward (hold time) the level on the D input must not change if the above function is to be executed correctly.

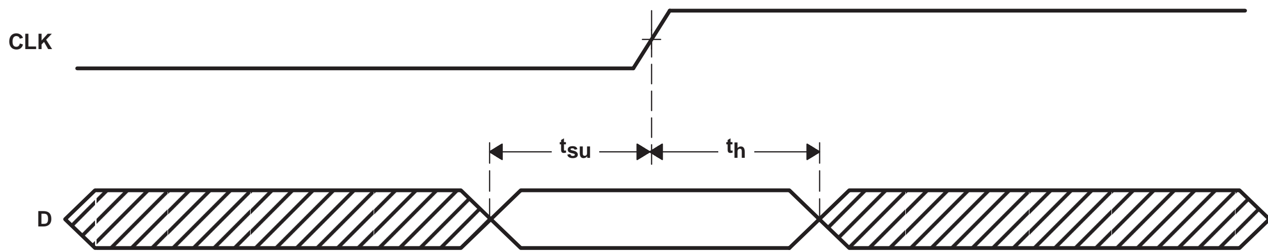


**Figure 2. Timing Conditions of a D-Type Flip-Flop**

In synchronous systems this timing can be maintained easily. But the situation is different with asynchronous circuits, in particular, synchronization circuits. Assume that, because of a change in level on the D input, the voltage on the output of gate G2 goes from low to high, meaning that the voltage on the output of gate G3 goes from high to low, and that the clock signal switches at the same time. If this happens at the instant when the difference in voltage between the two bases of transistors Q1and Q2 is virtually zero, the master flip-flop will not be able to adopt a stable, defined state. The logic state is neither high nor low. This is known as a metastable state. As a consequence, no defined state of the slave flip-flop is ensured under these circumstances.

The output signal of this flip-flop also adopts an unstable or metastable state (see Figure 3). The noise of transistors Q1 and Q2 (the master flip-flop forms a feedback amplifier) and interference penetrating from the exterior ensures that the master flip-flop and, consequently, the slave revert to one of the two possible but unpredictable stable states after a certain time.

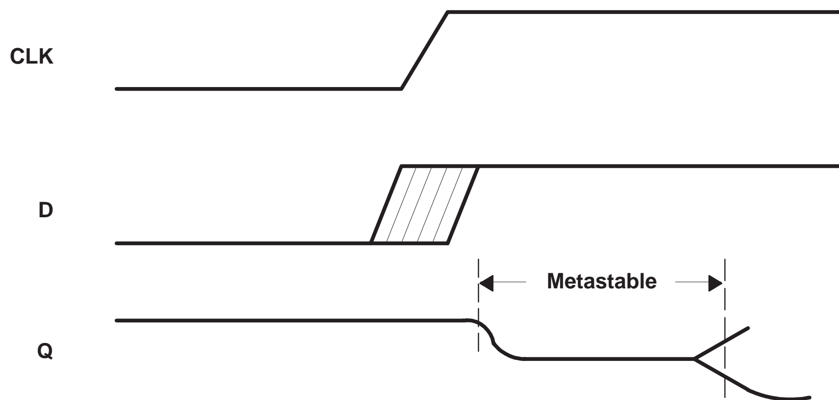


**Figure 3. Timing of Metastable States**

In the case illustrated in Figure 3, output Q or $\overline{Q}$ of the slave flip-flop adopts a level that is between the proper low and high levels. The output is in the metastable state of the master circuit consisting of transistors Q1and Q2. The output voltages of the master flip-flop do not correspond to the normal logic levels in a metastable state, so the internal voltage values can be corrupted through the voltage gain of gates G4 and G5 (slave) to such an extent that the signals shown in Figure 4 are on the output of the flip-flop. Curve A in Figure 4 illustrates the correct output signal. Curve B in Figure 4 shows that the slave, at first, does not recognize the metastable state of the master. It is not until the latter goes out of the unstable state that a reaction can be detected on the output, expressing itself as a very slow output edge and appearing, in practice, as a much longer delay. Curve C in Figure 4 shows that the metastable state of the master first generates a high level on the output of the slave. If the master then reverts to a stable state, a low level will appear again on the output of the flip-flop. The inverted signal shapes can be viewed in the same way. The phenomena shown here are described with reference to a bipolar circuit, but the same effects occur in CMOS and BiCMOS circuits.

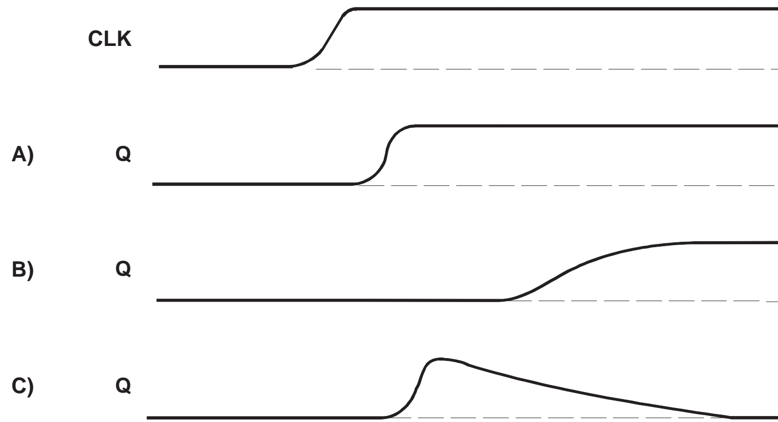


**Figure 4. Different Output Signals in the Metastable State**

Analyzing the metastable state of flip-flops is difficult because the critical time window in which the unstable state described may be generated is extremely short, about 10 to 100 ps.

In a circuit in which an asynchronous signal is synchronized with a clock, the mean time between failures (MTBF) in which a failure (metastable state) occurs is calculated from the frequency of the asynchronous signal ($f_{in}$), the clock frequency ($f_{clk}$), and the duration of the critical time window ($t_d$):

$$MTBF = \frac{1}{f_{in} \times f_{clk} \times t_d} \tag{1}$$

For $f_{clk}$ = 1 MHz, $f_{in}$ = 1 kHz, and $t_d$ = 30 ps, the result is:

$$MTBF = \frac{1}{1 \text{ Hz} \times 1 \text{ MHz} \times 30 \text{ ps}} = 33.3 \text{ s} \tag{2}$$

A designer using a flip-flop to synchronize two signals in this application cannot expect the maximum delays stated in the data sheets. To ensure reliable operation of the system, it is necessary to know how long to wait after the clock pulse before the data can be evaluated. Conventional test equipment is not capable of measuring these parameters. Therefore, a special test circuit is needed to determine the MTBF and the time ($t_x$) between the clock edge and a valid signal on the Q output. Once these parameters are known, the designer can choose the type of flip-flop to be used and after how much time valid data can be expected.

## 3 Description of Test Circuit

The probability of a flip-flop going into a metastable state is at its greatest when the input signal ($f_{in}$) always violates the setup-time and hold-time conditions. This is the case when the state on the D input of a flip-flop changes with each clock edge. Any other relationship between the frequency of the signal on the D input and the clock frequency would reduce the probability of the flip-flop that is to be tested going into a metastable state. The worst case is when the frequency ($f_{in}$) on the D input is precisely one-half the clock frequency ($f_{clk}$).

Figure 5 shows a simplified test circuit for determining the MTBF and $t_x$ for a particular flip-flop. An oscillator (O1) with a frequency of 1 MHz drives flip-flop FF1, which is configured as a 2:1 divider, thus satisfying the condition $f_{in} = 0.5\ f_{clk}$. To increase the probability of the tested flip-flop going into a metastable state, the high/low or low/high transition of the signal on the D input must jitter on the edge at the clock input. The width of this jitter should be equal to or greater than the sum of the setup and hold times of the flip-flop being tested. So the output signal of flip-flop FF1 is applied to an integrator (I) that slows down the rise or fall time to about 30 ns ($t_{su} + t_h$). The signal obtained in this way is impressed on the delta signal of the free-running oscillator O2 (f = 30 kHz) in comparator K1. This produces the data signal for the tested flip-flop FF2 on the output of the comparator, with the positive or negative edge jittering by 30 ns. The signal of oscillator O1 is applied at the same time via delay line DL1 to the clock input of the flip-flop that is to be tested ($f_{CLK1}$). This delay line compensates for the delays of flip-flop FF1, integrator I, and comparator K1. It is chosen so that the jitter on the D input of the flip-flop to be tested covers the setup and hold times stated in the data sheet (see Figure 6).

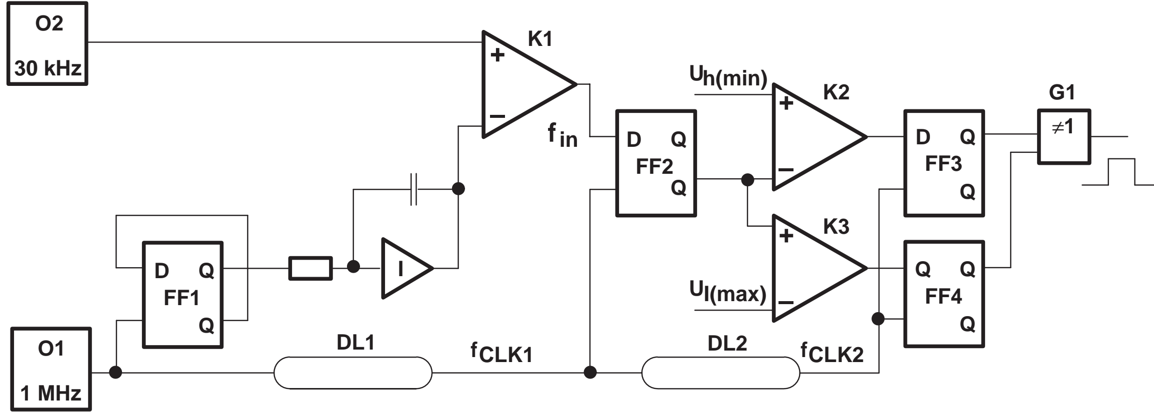


**Figure 5. Test Circuit for Examining the Metastable State**

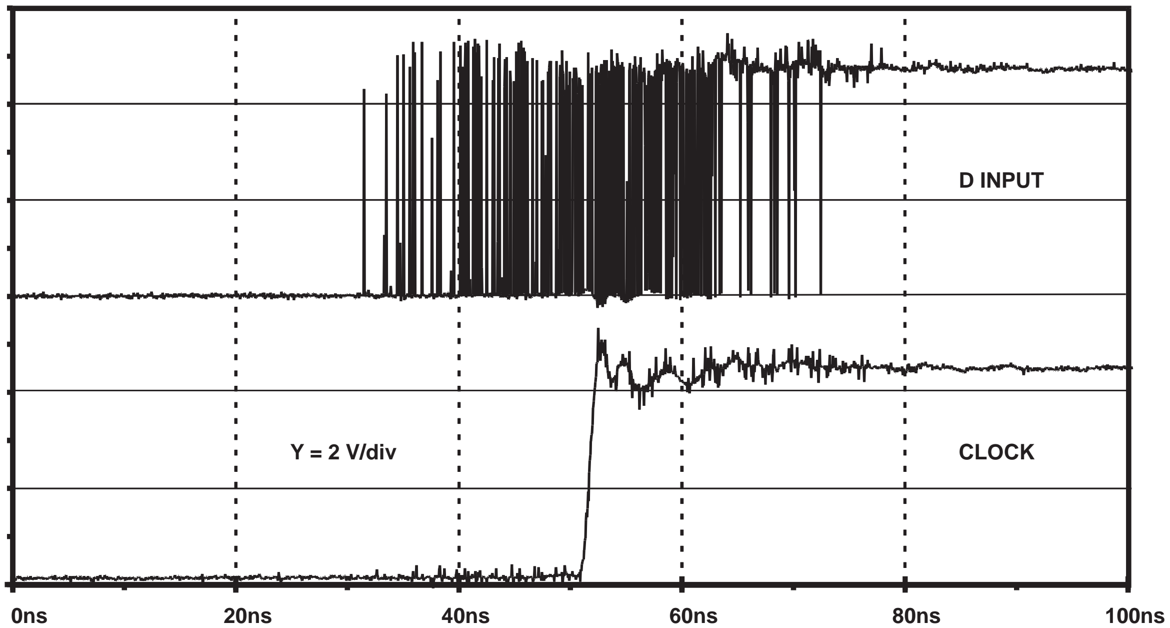


**Figure 6. Oscillogram of Clock and Data Signal on Flip-Flop FF2**

The output of flip-flop FF2 is then applied to comparators K2 and K3, which form a window comparator. Their outputs adopt the same state when there is a valid high or low level on the output of FF2 but adopt different states when the output voltage ($V_O$) of the flip-flop is in an undefined range:

$$V_{IH(min)} > V_O > V_{IL(max)} \tag{3}$$

The clock signal ($f_{CLK2}$), delayed by the time ($t_x$) by delay line DL2, samples the comparator outputs after this same time and sets flip-flops FF3 and FF4 accordingly. If there is a metastable state present at this time, the output of the exclusive-OR gate goes high.

This event is registered by the following counter. From the number N of metastable states detected within a certain time interval (t), it is then possible to determine the mean time between two metastable states according to equation 4:

$$MTBF = \frac{t}{N} \tag{4}$$

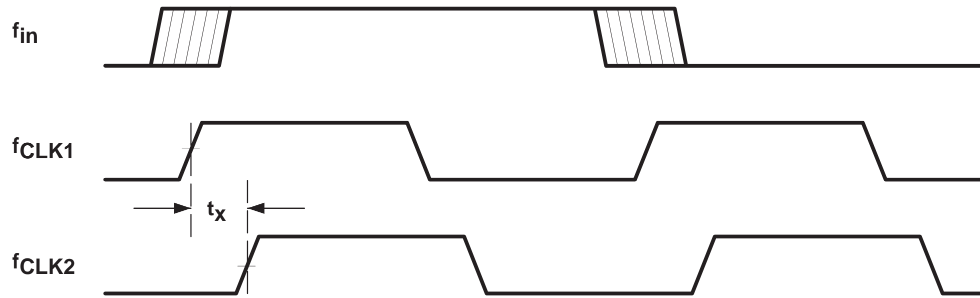


**Figure 7. Timing of Test Signals**

With the circuit described here, it is possible to determine the time between two failures as a function of the time ($t_x$). If this relation is entered on a semilogarithmic scale, the metastable characteristic of the flip-flop being examined for the required frequency of the input signal ($f_{in}$) is obtained.

Before discussing the test results, it is necessary to analyze the limitations of the test circuit, which influence the result. Two things can have a considerable influence on the test results: jitter of the input signal that is not centered on the clock signal and the delay of the evaluating circuit (K2, K3, FF3, and FF4).

If the edge of the input signal ($f_{in}$) does not jitter around the switching edge of the clock signal ($f_{CLK1}$), the probability that the flip-flop FF2 being tested will enter a metastable state is reduced. Care must be taken to ensure that the jitter of the input signal covers the time window formed by the setup and hold times.

In equation 1 it is assumed that the asynchronous signal alters in level randomly distributed over the clock period ($t_{fclk}$ = 1 µs). As shown in Figure 6, the signal on the D input of the device under test changes only in the mentioned time window ($t_j$) of 30 ns. The probability of the examined flip-flop being driven into the metastable state increases by the factor F:

$$F = \frac{t_{fclk}}{t_j} = \frac{1\ \mu s}{30\ ns} \quad (5)$$

The test results give the impression of a somewhat poorer response than can be expected in practice.

The evaluating circuit, consisting of comparators K1 and K2 and flip-flops FF3 and FF4, delays the output signal of the device under test and thus influences the result. For example, the flip-flop being tested might have left the metastable state, but the outputs of comparators K1 and K2 have not yet responded (because of the delay of this part of the circuit) when the edge of the clock signal ($f_{CLK2}$) arrives on flip-flops FF3 and FF4. It is difficult, in practice, to determine the magnitude of these errors precisely. To keep the error as small as possible, extremely fast devices in ECL technology were used in this part of the test circuit. This ensures that the uncertainty resulting from the delay of the comparators and the actual time of their sampling is smaller than 2 ns. When evaluating the test results, this error was taken into consideration by an appropriate horizontal shift of the line in Figure 8.

## 4 Test Results

Using the test circuit in Figure 5, different devices from the major logic families were examined with different values for $t_x$. The frequency of $f_{clk}$ was 1 MHz, the frequency on the data input ($f_{in}$) was 500 kHz. The duration of the test was long enough for a sufficient number of failures to appear. The number of failures was then divided by the test duration. This result is the mean time between failures (MTBF) for a particular time ($t_x$). The result was also recorded on a semilogarithmic scale for further evaluation (see Figure 8).

Basically, circuits from the faster logic families also leave the metastable state faster. Different circuits of a logic family showed virtually the same response, with only very slight deviations. This was to be expected because the same technology and practically identical circuit techniques are used within a logic family. The curves in Figure 8 are typical. In measurements on circuits of the same type but from different fabrication batches, differences were noted that corresponded roughly to the variation of the propagation delay times stated in the data sheets. An allowance for this variation should be made when calculating the worst case for a particular circuit. Also, devices of the same type from different producers exhibited substantial differences.

If other clock frequencies are used for testing, the probability of a metastable state occurring changes. The higher the frequency, the greater is the probability that a metastable state will occur; the probability decreases for lower frequencies. With the data derived from these experiments it is possible to devise an equation that describes the metastable response of a component for any frequencies:

$$\mathrm{MTBF} = \frac{\exp\ (T \times t_x)}{f_{clk} \times f_{in} \times T_O} \tag{6}$$

To produce the worst case during a test, that is, the setup-and-hold timing conditions are violated as often as possible, the frequency ($f_{in}$) of the input signal is, as already mentioned, chosen to be one-half the clock frequency ($f_{in} = 0.5\ f_{clk}$). On the basis of this, equation 6 changes to:

$$\mathrm{MTBF} = \frac{\exp\ (T \times t_x)}{0.5 \times f_{clk}^2 \times T_O} \tag{7}$$

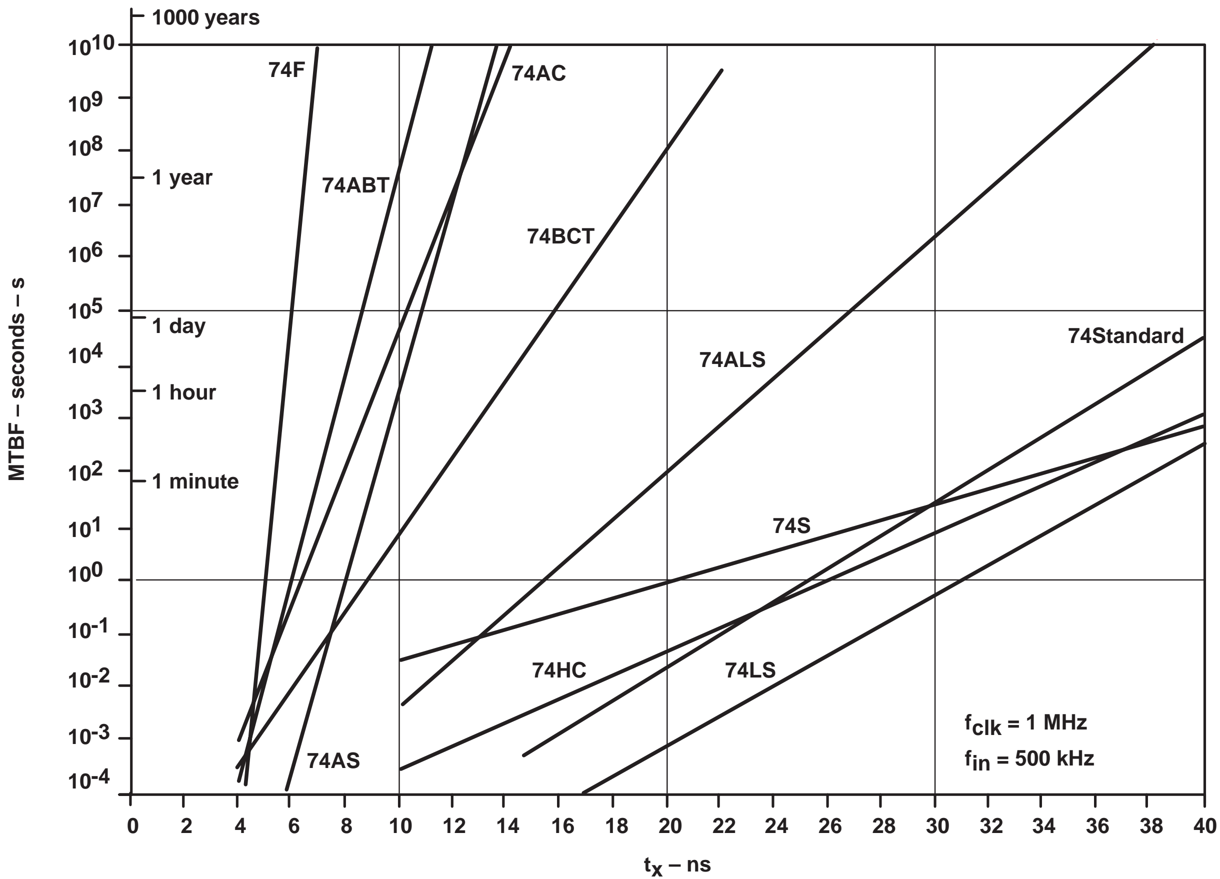


**Figure 8. Metastable Characteristic of Logic Circuits**

Constants $T_O$ and T describe the metastable response of the circuit. These can be calculated for any circuit family from the experimental data in Figure 8. As an example, the values for the ALS family are determined.

Constant T determines the slope of the lines (for a semilogarithmic representation as in Figure 8, the e function appears as a straight line). So the figure can be determined from the following equation:

$$T = \frac{\ln\ \mathrm{MTBF}(2) - \ln\ \mathrm{MTBF}(1)}{t_{x(2)} - t_{x(1)}} \tag{8}$$

And in this case:

$$T = \frac{\ln\ 10^2 - \ln\ 10^{-2}}{19.5\ \mathrm{ns} - 10.5\ \mathrm{ns}} = 1.02/\mathrm{ns} \tag{9}$$

To calculate constant $T_O$, solve equation 7 for $T_O$:

$$T_O = \frac{2 \times \exp(T \times t_x)}{MTBF \times f_{clk}^2} \tag{10}$$

So, in this case:

$$T_O = \frac{2 \times \exp(1.02 \times 19.5)}{100 \times 10^{12}} \tag{11}$$

By including the figures found for T and $T_O$ in equation 6, the equation that describes the metastable response of ALS circuits is:

$$MTBF = \frac{\exp(1.02 \times t_x)}{f_{in} \times f_{clk} \times 8.7 \times 10^{-6}} \tag{12}$$

With this equation, describing the worst case, a designer can calculate the metastable response of ALS circuits for any given input and clock frequencies. The corresponding equations for other digital circuits can be determined by the same method. The values of constants (T) and ($T_O$) for the most popular logic circuits are listed in Table 1.

**Table 1. Constants Describing the Metastable Behavior**

| Family | T (1/ns) | $T_O$ (s) |
|---|---|---|
| Std-TTL | 0.74 | $2.9 \times 10^{-4}$ |
| LS | 0.74 | $4.8 \times 10^{-3}$ |
| S | 0.36 | $1.3 \times 10^{-9}$ |
| ALS | 1.0 | $8.7 \times 10^{-6}$ |
| AS | 4.0 | $1.4 \times 10^{3}$ |
| F | 9.2 | $1.9 \times 10^{8}$ |
| BCT | 1.51 | $1.14 \times 10^{-6}$ |
| ABT | 3.61 | $33 \times 10^{-3}$ |
| HC | 0.55 | $1.46 \times 10^{-6}$ |
| AC | 2.8 | $1.1 \times 10^{-4}$ |

First, equation 7 is logarithmized:

$$\ln MTBF = t_x \times T - \ln T_O - \ln\left(0.5 \times f_{clk}^2\right) \tag{13}$$

This shows that the constant (T) determines the slope of the lines and, consequently, has the greatest influence on the failure rate that can be expected. Constant (T) is in the exponent in equation 7, so it has a more than proportional effect on the probability that the output of a synchronization circuit will adopt a stable state. This means, in turn, that those logic circuits are best suited for this purpose where the constant (T) is a high figure, as in AC, AS, ABT, and F circuits. The circuits of the other families come into question when the circuit has a sufficiently long settling time. Constant ($T_O$) has a much smaller influence on the characteristics of the circuits. It produces a parallel shift of the lines in the diagram in Figure 8. Although the figures for this constant differ by several powers of ten in the different circuit families, the influence of the constant T is still far more dominant.

## 5 Circuitry Measures

It is not possible to prevent metastability in flip-flops, so systems must be designed so that, to a sufficient degree of probability, no malfunctions appear in the circuitry. The possible errors and how to avoid them are explained with reference to the circuit in Figure 9. The circuit in question is the interrupt input of a computer system. External interrupts are normally asynchronous to the timing of a system, so an appropriate synchronization stage (FF1) must be provided. If this flip-flop goes into a metastable state, for the reasons mentioned, the voltage levels on its output are no longer defined; in extreme cases they are close to the threshold voltages of the following circuit. Assume that gate G1, which collects the interrupt signals of different sources and signals the presence of an interrupt to the state control of the computer, accepts the metastable level as a valid interrupt signal. But the priority encoder, which is responsible for generating the appropriate interrupt vector, does not recognize this signal

(in such a case differences in the threshold voltage of the individual circuits of just a few millivolts are enough to create the situation described here). The result is that the interrupt is triggered in the state control, but the wrong interrupt vector is generated, causing a dramatic malfunctioning of the computer. This result is aggravated by the fact that such errors are practically undetectable, even with high-grade instruments like logic analyzers. The sampling clock of the logic analyzer most likely will not sample the signals in question in the examined circuit at the critical moment. It is also highly improbable that the threshold voltage of this test instrument will have exactly the same value as the circuit examined, meaning that the abnormal operating state cannot be detected without a special, cumbersome test setup.

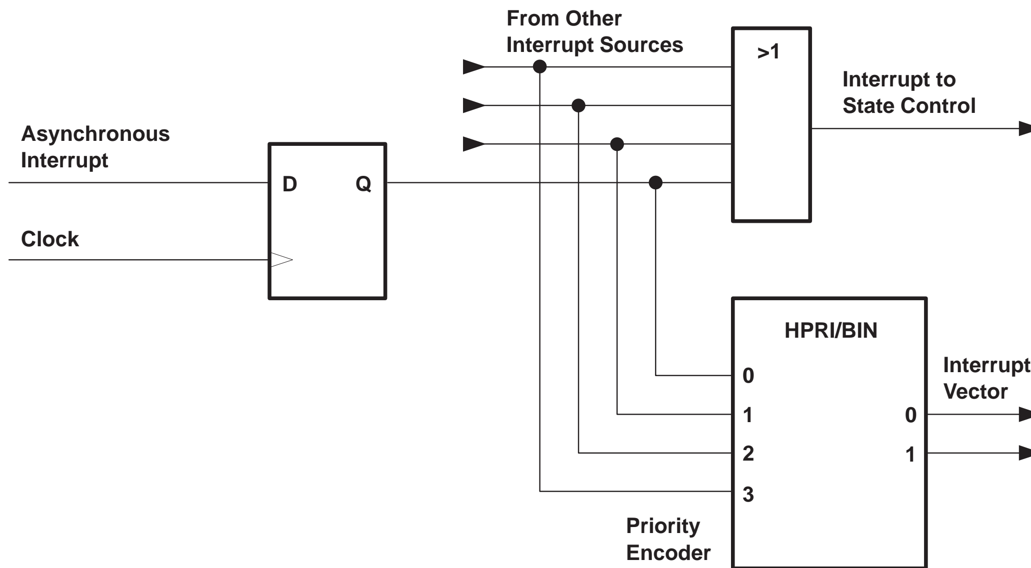


**Figure 9. Interrupt Synchronization**

Actual figures can be used to calculate the reliability or error rate (MTBF) of the above circuit. The data used are:

| | |
|---|---|
| Type of flip-flop | SN74ALS74 |
| Mean frequency of asynchronous interrupt signal | $f_{in}$ = 10 kHz |
| System clock frequency | $f_{clk}$ = 10 MHz |
| Setup time of following circuit | $t_{su}$ = 25 ns |

At the output of the synchronization stage, the settling time ($t_x$) is calculated as follows:

$$t_x = \frac{1}{f_{clk}} - t_{su} \quad (14)$$

$$t_x = \frac{1}{25\ \text{MHz}} - 15\ \text{ns} = 25\ \text{ns} \quad (15)$$

Taking equation 6 and the values of Table 1:

$$\text{MTBF} = \frac{\exp\ (1.0 \times 25\ \text{ns})}{25\ \text{MHz} \times 10\ \text{kHz} \times 8.8 \times 10^{-6}} = 3273\ \text{s} \approx 54\ \text{min} \quad (16)$$

This error rate is much too high. To reduce it, there is, first of all, the possibility of using circuits that exhibit a much shorter settling time and, therefore, leave the metastable state faster. As mentioned previously, these are the components in which the constant (T) is high, e.g., circuits of the SN74AS series. If you make the same calculation for an SN74AS74, the mean time between two failures (MTBF) is 2.4 x $10^{21}$ years, ensuring adequate reliability.

However, there are many applications in which you cannot just switch to a different family of circuits, e.g., where programmable circuits are used and one type of flip-flop is prescribed for all parts of the densely integrated circuitry. One remedy in this case is the use of a two-stage synchronization circuit (see Figure 10).

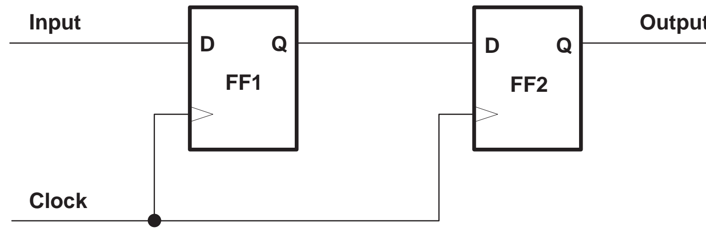


**Figure 10. Two-Stage Synchronization Circuit**

The second flip-flop receives the output signal of the first stage one clock period later and can go into a metastable state only if its input conditions are also violated. That is, the output of the first flip-flop is still metastable during its setup and hold time. So the critical input frequency $f_{in(2)}$ of the second stage is calculated from the reciprocal of the mean time between two failures of the first stage:

$$f_{in(2)} = \frac{1}{MTBF(1)} = \frac{f_{in(1)} \times f_{clk} \times T_O}{\exp\left[T \Big/ \left(\frac{1}{f_{clk} + t_{su}}\right)\right]} \quad \textbf{(17)}$$

If you again take equation 6 and insert the $f_{in(2)}$ value calculated here as the input frequency, the result, assuming that the same type of flip-flop is used in both stages of the synchronization circuit, is:

$$MTBF(2) = \frac{\exp\ (T - t_x)}{f_{in(2)} \times f_{clk} \times T_O} \quad \textbf{(18)}$$

or

$$MTBF(2) = \frac{\exp\ (T \times t_x) \times \exp\left[T \times \left(\frac{1}{f_{clk} - t_{su}}\right)\right]}{f_{in(2)} \times f_{CLK2} \times T_{O(2)}} \quad \textbf{(19)}$$

Now, go back to the synchronization circuit of the interrupt input that was described previously. Using one SN74ALS74 flip-flop, the MTBF was 54 minutes. Again, assuming that the second flip-flop is sampled after 25 ns, the result is:

$$MTBF(2) = \frac{\exp\ (1.0 \times 25ns)}{\left(\frac{1}{54\ min}\right) \times 25\ MHz \times 8.8 \times 10^{-6}} = 2\ million\ years \quad \textbf{(20)}$$

By selecting the right component or the right circuit, excellent reliability can be achieved without any difficulty, even in time-critical applications. In the example shown above, the problem was resolved by incorporating an additional flip-flop stage, and without having to resort to especially fast circuit families. This was possible, for the most part, because an extra delay of one clock period in the interrupt input has no marked effect on system characteristics. In most modern microprocessors there are already appropriate circuits integrated (like the above two-stage synchronization circuit), which is why the engineer only has to take particular measures when designing special interrupt control circuits). With the READY input of a microprocessor, for example, things are different. For this kind of input there are setup and hold times specified in the data sheets for the devices, as with flip-flops, that must be maintained. The integration of an extra flip-flop in the processor, reducing the probability of errors through metastable states, is not wise because such a circuit would extend each bus cycle by one clock period in synchronous systems also and, in most cases, the processor works synchronously with the assigned memory. Such integration is not acceptable. For asynchronous operation an additional synchronization stage must be provided externally (see Figure 12). To arrive at a reliable circuit and avoid unnecessary delays, the critical times must be analyzed closely. This now will be done for the TMS320C25 microprocessor. Figure 11 shows the timing conditions of the READY input and the associated clock signals CLKOUT1 and CLKOUT2.

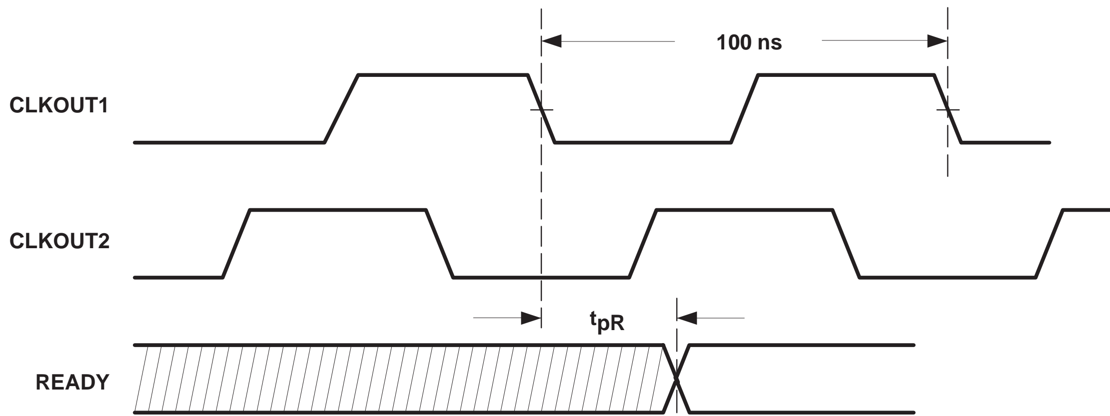


**Figure 11. Timing Conditions of READY Signal in TMS320C25**

For synchronization purposes, the negative edge of the clock CLKOUT1 is used. The READY signal must, when referred to this event, be valid after a time of $t_{pR}$ = 30 ns. A D-type flip-flop, as required in this application, is triggered with the positive edge, so the CLKOUT1 signal has to be inverted. The SN74AS04 inverter that is used for this delays the clock signal by a maximum of $t_{pd}$ = 5 ns. The system clock frequency is $f_{clk}$ = 10 MHz. Assuming that the mean data rate is $f_D$ = 5 MHz and that a flip-flop of the type SN74ALS74 is used, equation 6 and Table 1 produce:

$$\text{MTBF} = \frac{\exp\left[T \times \left(t_{pR} - t_{pd}\right)\right]}{f_{CLKOUT1} \times f_D \times T_O} \tag{21}$$

$$\text{MTBF} = \frac{\exp\ [1.0 \times (30\ \text{ns} - 5\ \text{ns})]}{10\ \text{MHz} \times 5\ \text{MHz} \times 8.8 \times 10^{-6}} = 163\ \text{s} \tag{22}$$

In this case, a synchronization error can be expected about every 2.3 min, which, as experience shows, leads to a crash, making it unacceptable. If you use an SN74AS74 flip-flop instead, the MTBF is more acceptable:

$$\text{MTBF} = \frac{\exp\ [4.03 \times (30\ \text{ns} - 5\ \text{ns})]}{10\ \text{MHz} \times 5\ \text{MHz} \times 1.4 \times 10^{3}} = 2.58 \times 10^{19}\ \text{years} \tag{23}$$

Figure 12 illustrates the circuit in question.

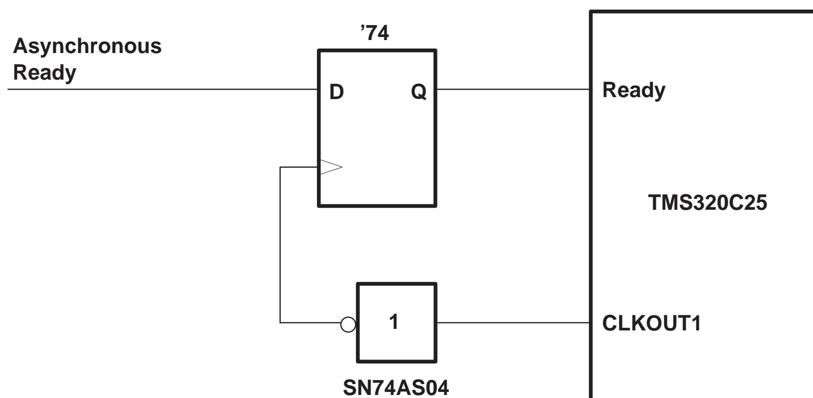


**Figure 12. Synchronization of READY Input**

## 6 Integrated Synchronization Circuits

There is nothing more obvious than integrating the two-stage synchronization devices described previously into one circuit in order to reduce the component count in a system. Figure 13 shows the circuit of such a synchronization stage in an SN74AS4374B.

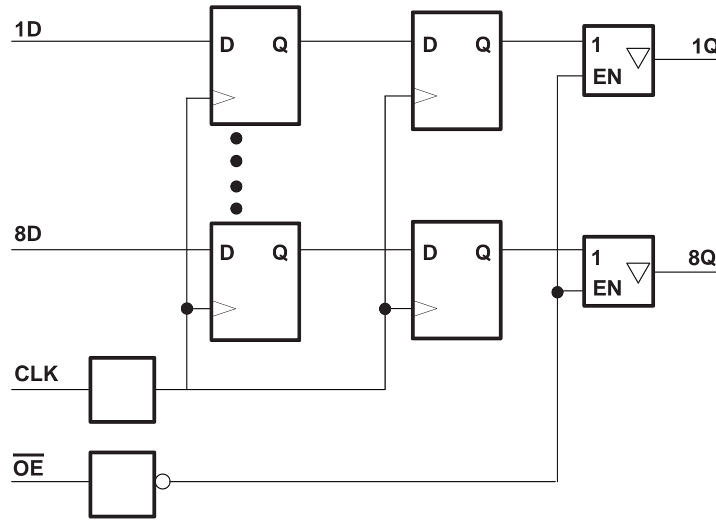


**Figure 13. Logic Diagram of SN74AS4374B Synchronization Circuit**

This integration produces additional advantages in terms of metastable response and, thus, system reliability. The first flip-flop requires no buffer stage at its output, which is largely responsible for the delay of the flip-flop, so its delay is considerably shorter than with an SN74AS74, for example. This time saving (about 1 to 2 ns) is then available in addition for stabilization of the first flip-flop if it goes into a metastable state. Furthermore, the D input of the second flip-flop does not need an input buffer stage, thus reducing the setup time at this point by about 0.5 to 1 ns. The time gained here is also available for stabilization of the first stage after a metastable state.

Constants (T) and ($T_O$) for this flip-flop were derived experimentally and are:

$$T = 2.4 \text{ and } T_O = 3.96 \times 10^{-9} \tag{24}$$

In a two-stage synchronization circuit, as shown in Figure 13, the mean time between two failures is calculated using equation 25:

$$MTBF = \frac{\exp\left[T \times \left(\frac{1}{f_{clk}}\right)\right] \times \exp\left(T \times t_x\right)}{f_{in} \times f_{CLK2} \times T_{O(2)}} \tag{25}$$

For simplicity, it is assumed that the first flip-flop has time to stabilize, which corresponds to precisely the clock period. The time $t_X$ is again the time by which the output of the second flip-flop is evaluated later by the following circuit, that is, the time that the second flip-flop has for stabilization. In most cases, it also corresponds to the period of the clock frequency reduced by the setup time of the following circuit.

## 7 Summary

The metastable characteristic of a flip-flop in a synchronization circuit determines, to a large degree, the reliability of a system. On the basis of what has been said in this report, the designer can decide what type of flip-flop should be used in a given application and to what extent the metastable response will be manifest.

From the experimental data in Figure 8 it can be seen that fast logic circuits, like those of the series SN74AS, SN74F, 74AC, or SN74ABT, exhibit the best metastable response. These devices have a very short setup-and-hold time window, thus reducing the probability that they will go into a metastable state. Apart from this, they return to a stable state much faster if they have gone metastable. But ALS, LS, or HC circuits, for example, can also produce satisfactory results if the clock frequency in the application is low enough. When choosing a flip-flop, the speed requirements of a system must be considered.

## 8 Acknowledgment

The author of this document is Eilhard Haseloff.