Tsinghua Freescale Embedded System Center
www.tsinghua-freescale.net
by Zeng, Ming zengming@tsinghua.edu.cn
Gong, Guanghua ggh@tsinghua.edu.cn
Xue, Tao gbe.tao.xue@gmail.com

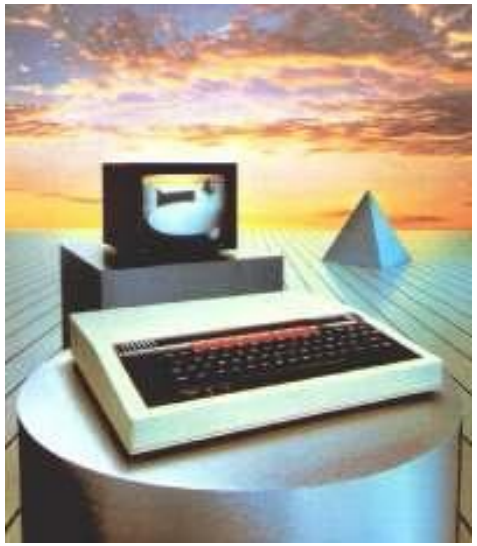
Freescale Kinetis Basic

清华Freescale应用开发研究中心 曾鸣

2012年03月

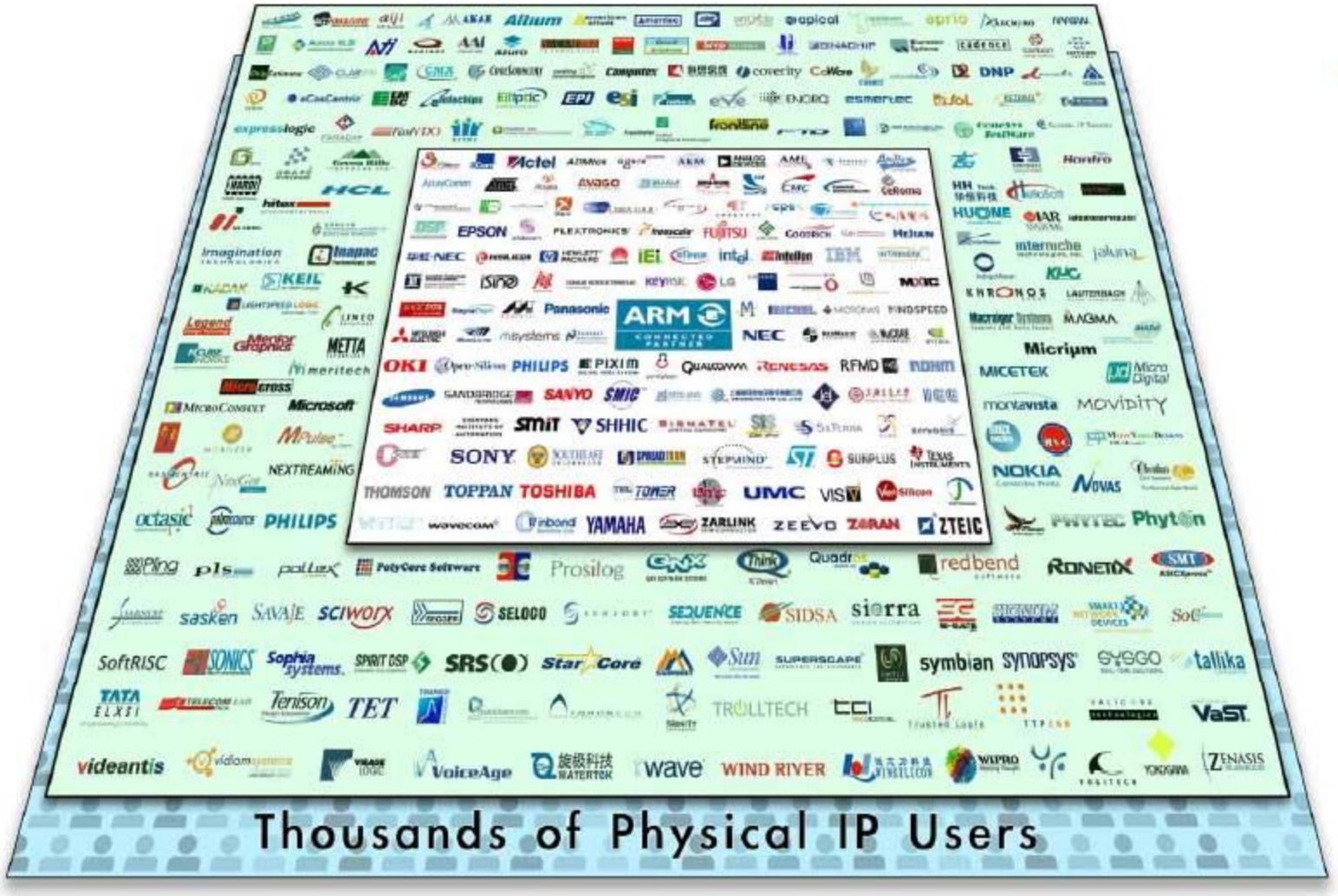
ARM History

- Acorn Computer Group developed world's first RISC processor in 1985
- Roger Wilson and Steve Furber were the principle developers
- ARM (Advanced RISC Machines) was a spin out from Acorn in 1990 with goal of defining a new microprocessor standard



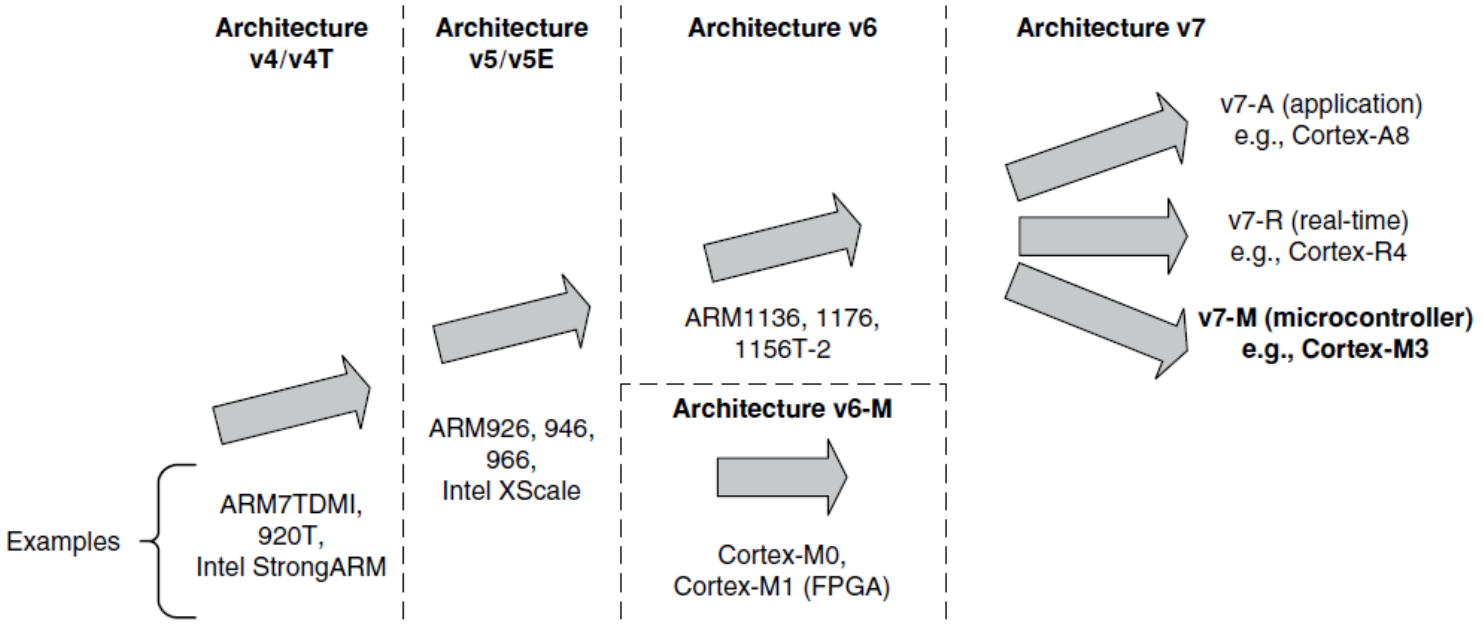
ARM History

- ARM delivered ARM6 in 1991
  - Introduced 32 bit addressing support
  - New instruction for program status registers
  - Variant used in Apple Newton PDA
- By 1996 ARM7 was being widely used
  - Microsoft started port of WinCE to ARM
  - Added multimedia extensions
- Exponential growth from then on…


ARM
Thousands of Physical IP Users

ARM架构进化史

ARM的发展过程



The Evolution of ARM Processor Architecture.

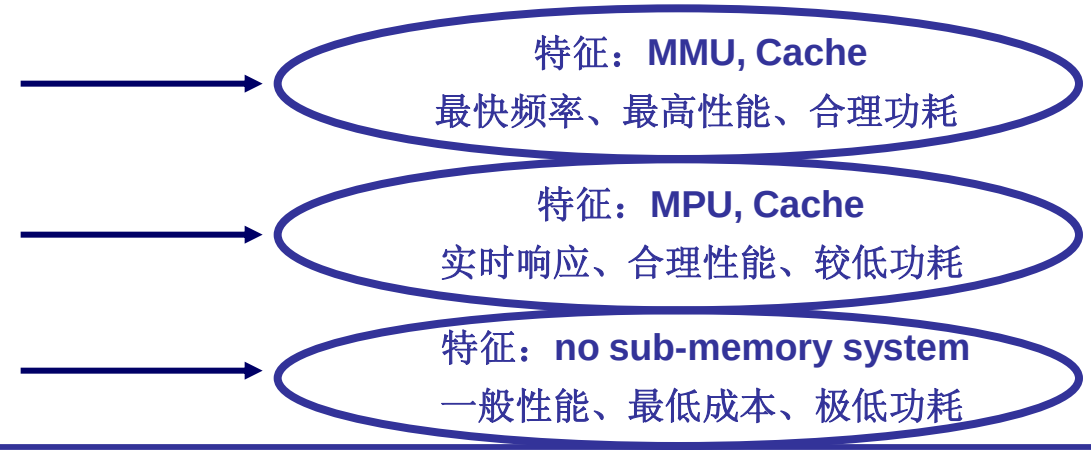
ARM公司只做CPU设计，采用出售IP的方式运营，半导体制造商无需自己设计CPU, 是生产关系的革命，提高了生产力

FESC

ARM处理器的分类

- 结构体系版本（Architecture） • Processor Family
  - ARM v4T → – ARM7
  - ARM v5TE → – ARM9
  - → – ARM10
  - ARM v6 → – ARM11
  - ARM Cortex (v7) → – ARM Cortex

- 按应用特征分类
  - 应用处理器
    - Application Processor
  - 实时控制处理器
    - Real-time Controller
  - 微控制器
    - Micro-controller

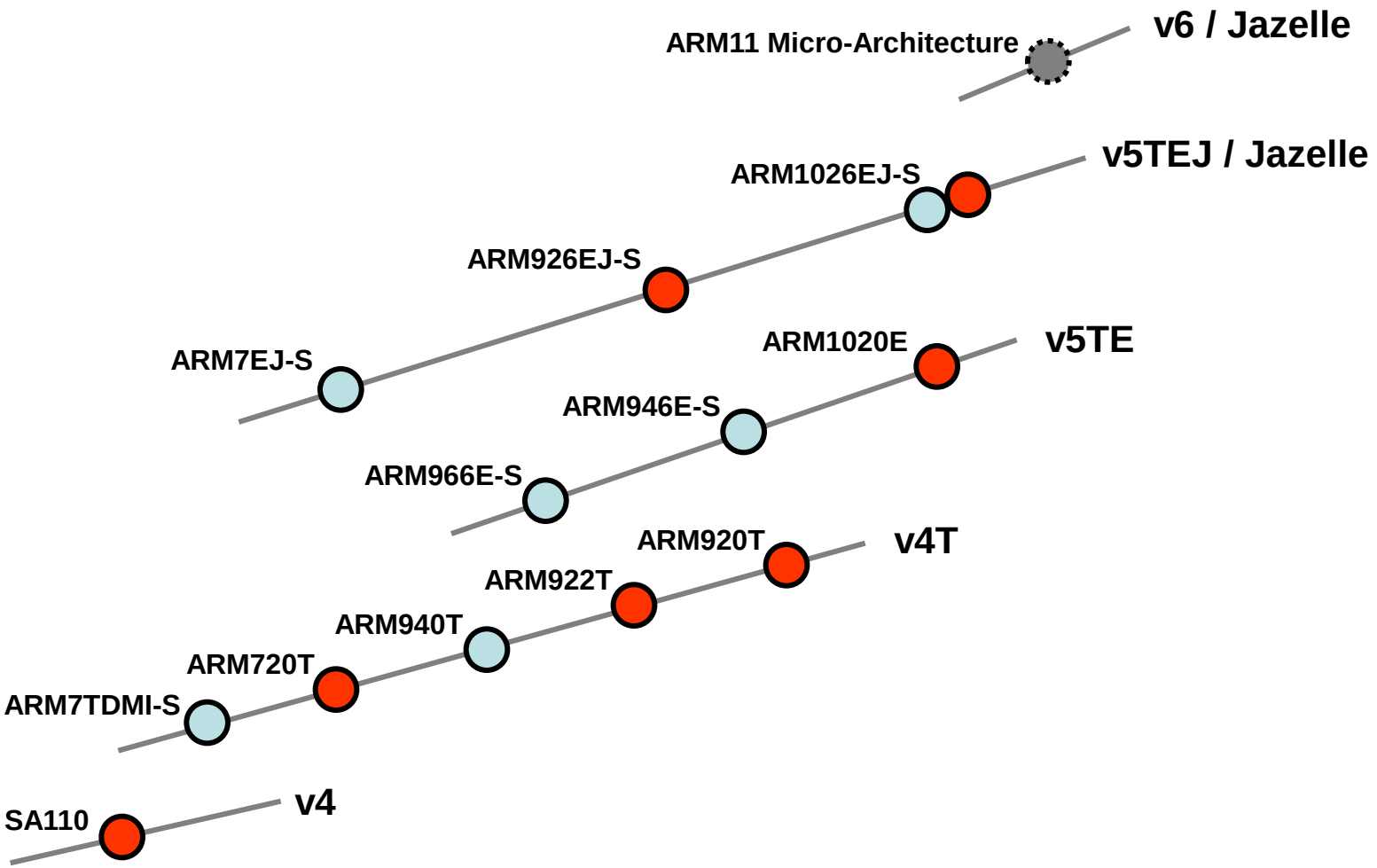


FESC

ARM and StrongARM

- Intel gained certain IP from ARM as part of lawsuit settlement and modified ARM architecture branding it as StrongARM
- StrongARM name was changed to XScale
  - Processor SA1000 , SA1100
- XScale is close to ARMv5 instruction set
- XScale division of Intel was sold to Marvel Inc. in 2006

Roadmap of ARM V4/V5/V6



FESC

ARM V4

- ARMV4是目前支持的最老的架构,是基于32-bit地址空间的32-bit指令集。ARMv4除了支持ARMv3的指令外还扩展了：
  - **支持halfword的存取**
  - **支持byte和halfword的符号扩展读**
  - **支持Thumb指令**
  - **提供Thumb和Normal状态的转换指令**
  - **进一步的明确了会引起Undefined异常的指令**
  - **对以前的26bits体系结构的CPU不再兼容**

ARMv4T

- ARMv4T增加了16-bit Thumb 指令集，这样使得编译器能产生紧凑代码（相对于32-bit代码，内存能节省到35%以上)并保持32-bit系统的好处。
- Thumb在处理器中仍然要扩展为标准的32位ARM指令来运行。用户采用16位Thumb指令集最大的好处就是可以获得更高的代码密度和降低功耗。

ARM V5TE

- 1999年推出ARMv5TE其增强了Thumb体系,增强的Thumb体系增加了一个新的指令同时改进了Thumb/ARM相互作用、编译能力和混合及匹配ARM与Thumb例程，以更好地平衡代码空间和性能
- 并在ARM ISA上扩展了增强的DSP 指令集:
  增强的DSP指令包括支持饱和算术（saturated arithmetic），并且针对Audio DSP应用提高了70%性能。 ‘E’扩展表示在通用的CPU上提供DSP能力。

ARMv5TEJ

- 2000年推出ARMv5TEJ，增加了Jazelle扩展以支持Java加速技术。
- Jazelle技术比仅仅基于软件的JVM性能提高近8倍的性能减少了80%的功耗。

ARMv6

- 2001年推出ARMv6，它在许多方面做了改进如内存系统、异常处理和较好地支持多处理器。
- SIMD扩展使得广大的软件应用如Video和Audio codec的性能提高了4倍。
- Thumb-2和TrustZone 技术也用于ARMv6中。ARMv6第一个实现是2002年春推出的ARM1136J(F)-STM处理器，2003年又推出了 ARM1156T2(F)-S 和ARM1176JZ(F)-S处理器。

ARMv7

- ARMv7定义了3种不同的处理器配置（processor profiles）：
  - **Profile A是面向复杂、基于虚拟内存的OS和应用的**
  - **Profile R是针对实时系统的**
  - **Profile M是针对低成本应用的优化的微控制器的。**
- 所有ARMv7 profiles实现Thumb-2技术，同时还包括了NEON™技术的扩展提高DSP和多媒体处理吞吐量400%，并提供浮点支持以满足下一代3D图形和游戏以及传统嵌入式控制应用的需要。

系列	相应产品	性能特点
ARM7 系列	ARM7TDMI ， ARM7TDMI-S ， ARM720T，ARM7EJ	三级流水 性能： 0.9MIPS/MHz, 可达到130MIPs (Dhrystone2.1)
ARM9 系列	ARM920T， ARM922T	五级流水， 性能： 1.1MIPS/MHz，可达300 MIPS (Dhrystone 2.1)，单32-bit AMBA bus 接口，支持MMU
ARM9E 系列	ARM926EJ-S，RM946E-S, ARM966E-S，ARM968E-S, ARM996HS	五级流水，支持DSP指令。 性能： 1.1MIPS/MHz，可达300 MIPS (Dhrystone 2.1)，高性能AHB, 软核（soft IP）
ARM10 系列	ARM1020E， ARM1022E ARM1026EJ-S	6级流水支持分支预测（branch prediction），支持DSP指令。 性能： 1.35 MIPS/MHz，可达 430+ Dhrystone 2.1 MIPS，，可选支持高性能浮点操作，双64位总线接口，内部64位数据通路

FESC

系列	相应产品	性能特点
ARM11 系列	ARM11MPCore, ARM1136J(F)-S, ARM1156T2(F)-S, ARM1176JZ(F)-S	8级流水线(9级ARM1156T2(F)-S)，独立的load-store和arithmetic流水线，支持分支预测和返回栈（Return Stack）。强大的ARMv6 指令集，支持DSP， SIMD (Single Instruction Multiple Data) 扩展，支持ARM TrustZone 、Thumb-2核心技术。740 Dhrystone 2.1 MIPS，低功耗0.6mW/MHz (0.13μm, 1.2V)
Cortex 系列	Cortex-A8, Cortex-M3, Cortex-R4	Cortex-A系列: 面向用于复杂OS和应用的应用处理器（applications processors），支持ARM, Thumb and Thumb-2指令集。 Cortex-R系列：面向嵌入式实时领域的嵌入式处理器，支持ARM, Thumb,和Thumb-2 指令集。 Cortex-M系列：面向深嵌入式价格敏感的嵌入式处理器，只支持Thumb-2指令集

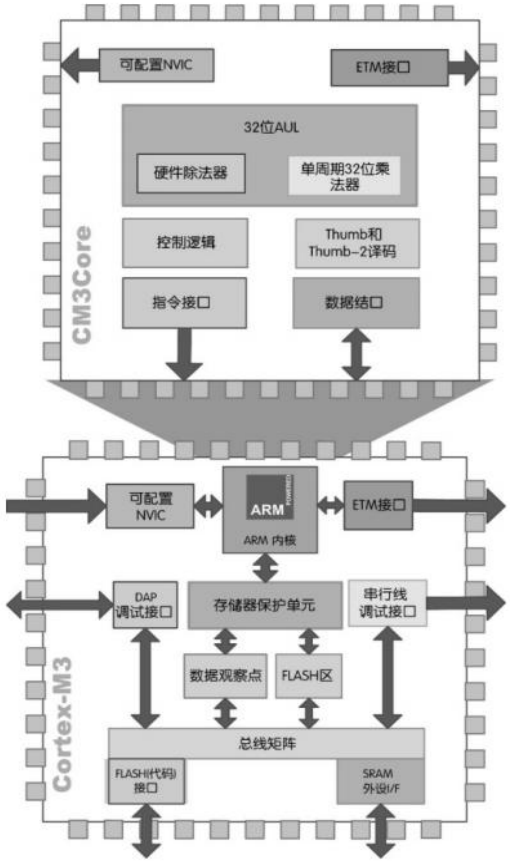
ARM Design Philosophy

- ARM core uses RISC architecture
  - Reduced instruction set
  - Load store architecture
  - Large number of general purpose registers
  - Parallel executions with pipelines
- But some differences from RISC
  - Enhanced instructions for
    - Thumb mode
    - DSP instructions
    - Conditional execution instruction
    - 32 bit barrel shifter

Cortex-M3/4内核主要是**应用于低成本、小管脚数和低功耗的场合，并且具有极高的运算能力和极强的中断响应能力**。

Cortex-M3/4处理器采用纯Thumb2指令的执行方式，使得这个具有32位高性能的ARM内核能够实现8位和16位的代码存储密度。ARM Cortex-M3/4处理器是使用最少门数的ARM CPU，核心门数只有33K，在包含了必要的外设之后的门数也只有60K，使得封装更为小型，成本更加低廉。

Cortex-M3/4采用了ARM V7哈佛架构，具有带分支预测的3级流水线，中断延迟最大只有12个时钟周期，在末尾连锁的时候只需要6个时钟周期。同时具有**1.25DMIPS/MHZ**的性能和**0.19mW/MHZ**的功耗。



Cortex-M3内核框图

FESC

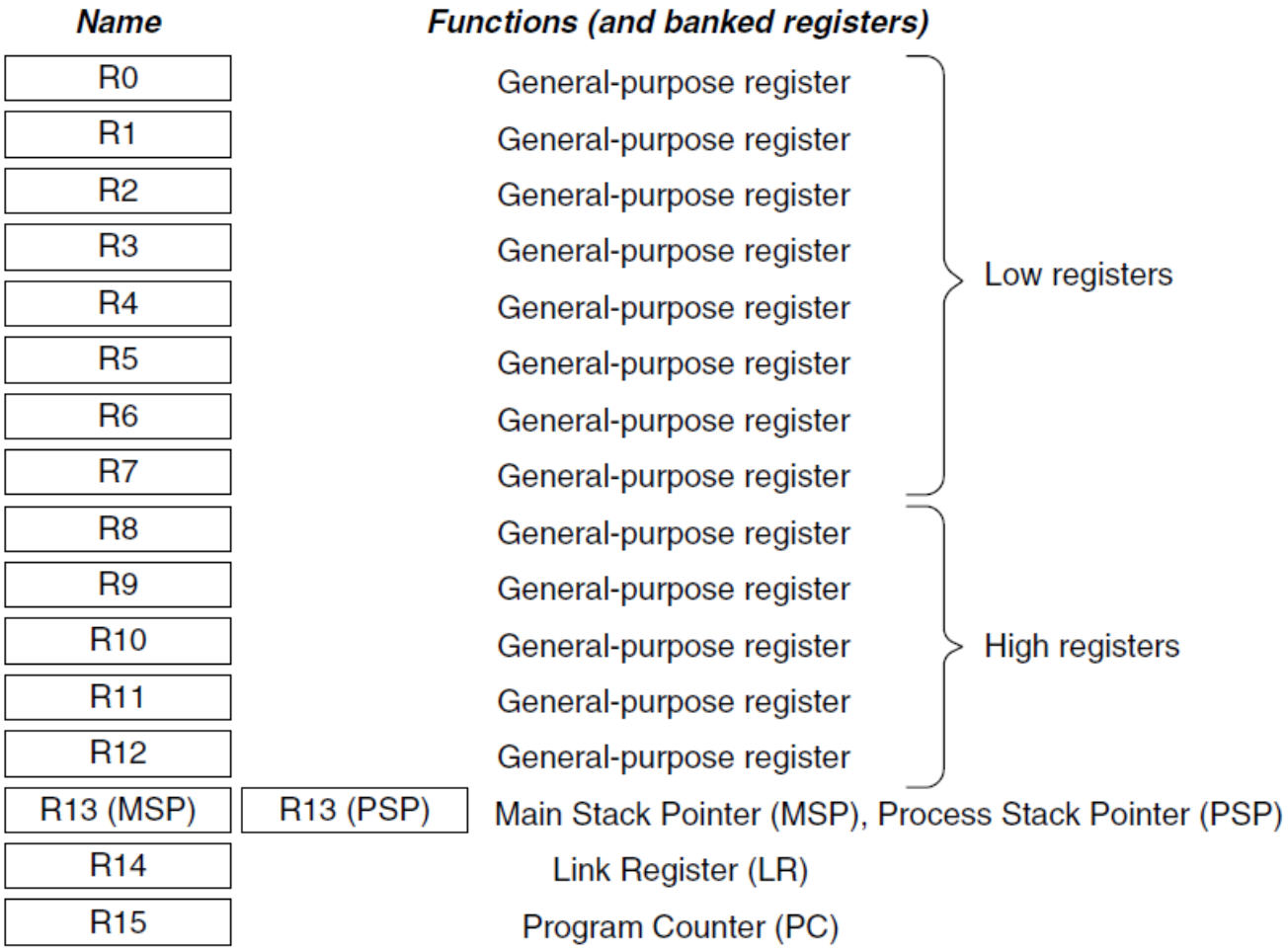
Cortex-M3/4内核：哈佛架构

Cortex-M3/4 中央内核基于哈佛架构，指令和数据各使用一条总线。

与 Cortex-M3/4不同，ARM7 系列处理器使用冯 诺依曼（Von Neumann）架构，指令和数据共用信号总线以及存储器。

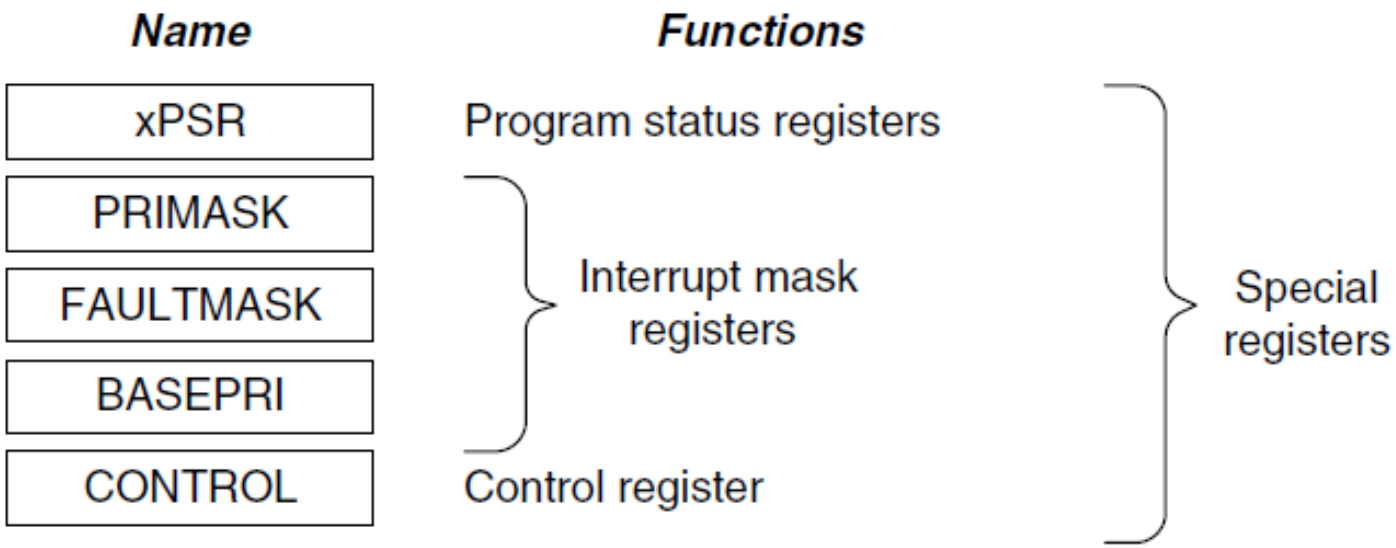
由于指令和数据可以从存储器中同时读取，所以 Cortex-M3/4 处理器对多个操作并行执行，加快了应用程序的执行速度。

Cortex-M3/4内核：寄存器组



FESC

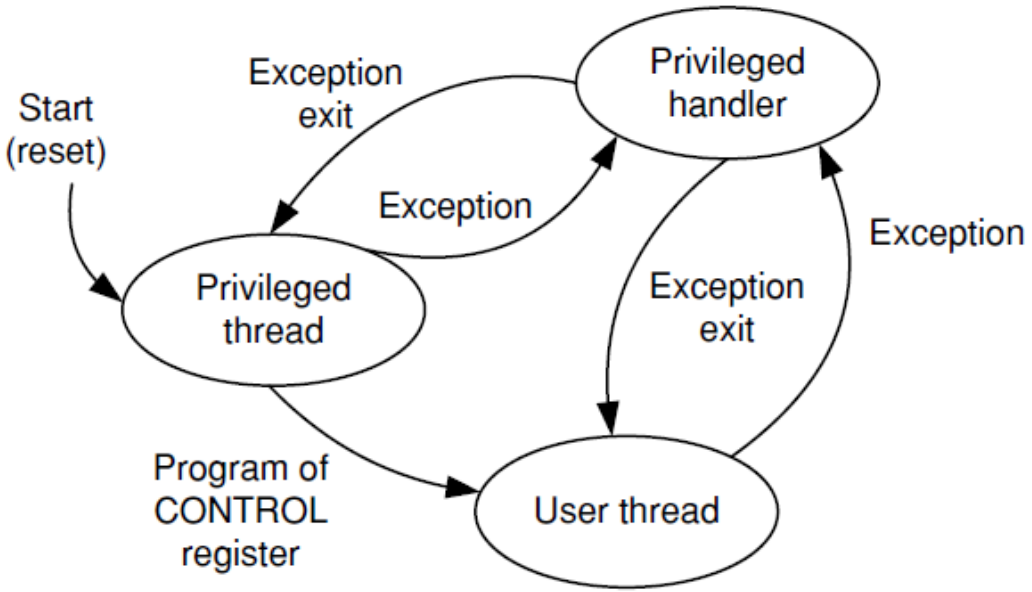
Cortex-M3/4内核：特殊功能寄存器



FESC

Cortex-M3/4内核：特权态和用户态

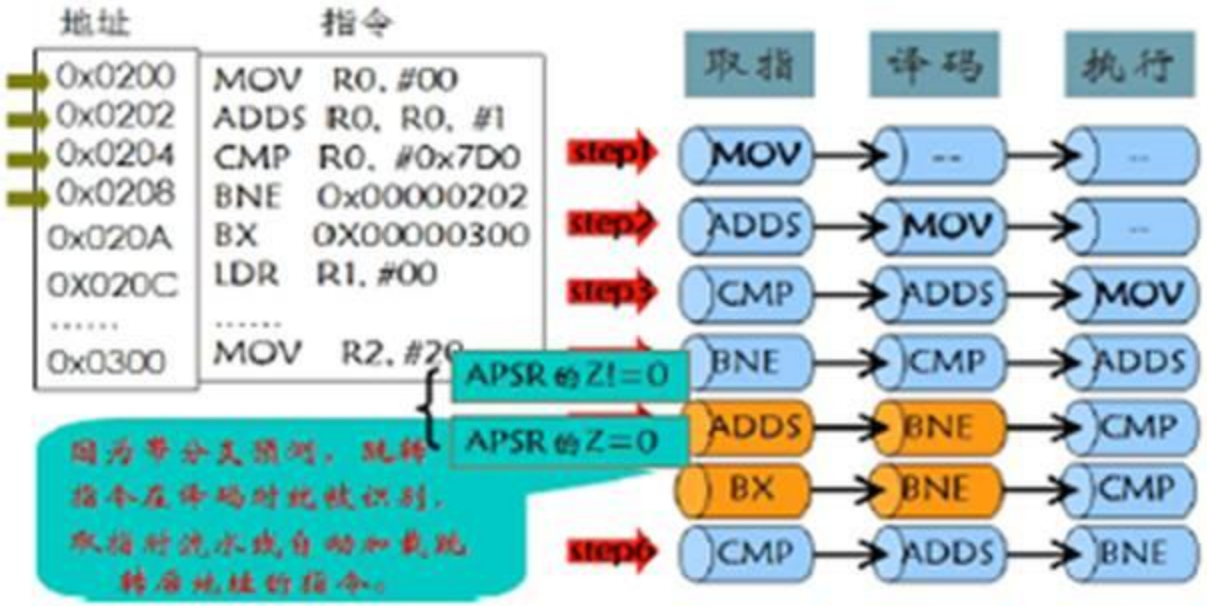
	Privileged	*User*
When running an exception handler	Handler mode	
When not running an exception handler (e.g., main program)	Thread mode	Thread mode



FESC

Cortex-M3/4内核：分支预测的流水线

内核流水线分3个阶段：取指、译码和执行。当遇到分支指令时，译码阶段也包含预测的指令取指，这提高了执行的速度。处理器在译码阶段期间自行对分支目的地指令进行取指。在稍后的执行过程中，处理完分支指令后便知道下一条要执行的指令。如果分支不跳转，那么紧跟着的下一条指令随时可供使用。如果分支跳转，那么在跳转的同时分支指令可供使用，空闲时间限制为一个周期。



FESC

Cortex-M3/4存储器映射

Cortex-M3/4 处理器采用单一存储映射的模式，提供4GB的可寻址存储空间。

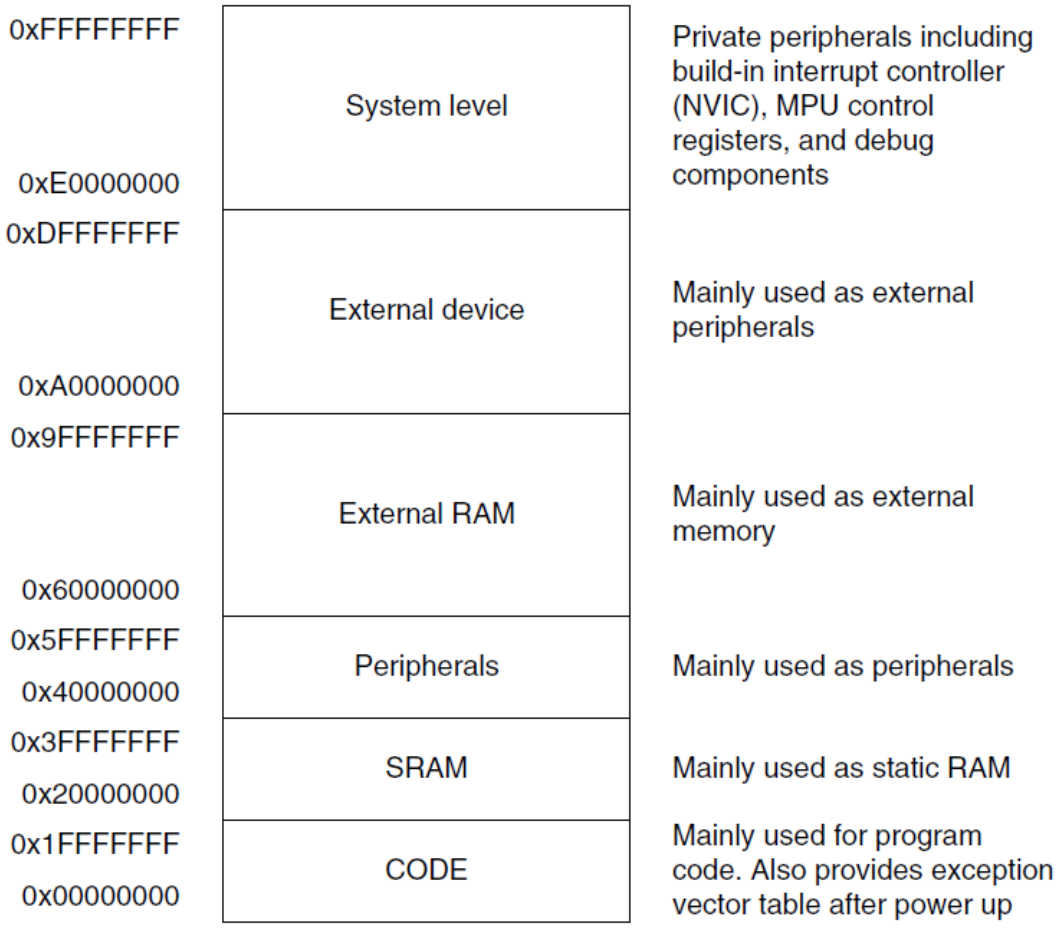
同时，这些空间为代码（代码空间）、SRAM（存储空间），外部存储器/器件和内部/外部外设提供预定义的专用地址。另外，还有一个特殊区域专门供厂家使用。

借助位带操作（bit-banding）技术，Cortex-M3/4 处理器可以在简单系统中直接对数据的单个位进行访问。

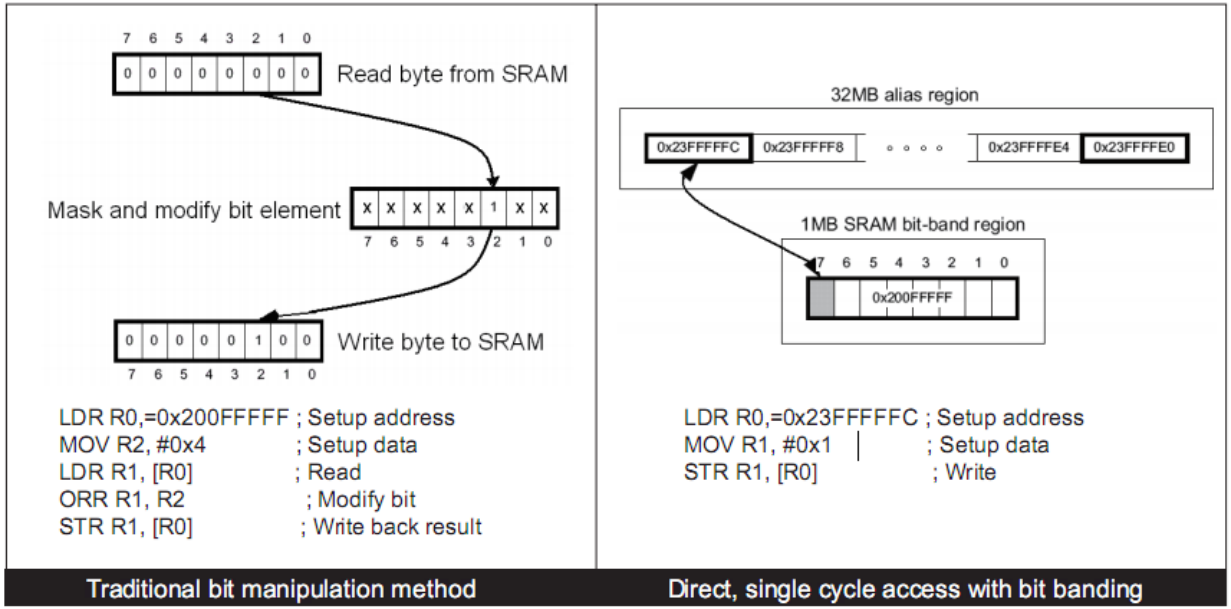
存储器映射包含两个位于SRAM的大小均为1MB的bit-band区域和映射到32MB别名区域的外设空间。在别名区域中，某个地址上的加载/存储操作将直接转化为对被该地址别名的位的操作。对别名区域中的某个地址进行写操作，如果使其最低有效位置位，那么bit-band位为 1，如果使其最低有效位清零，那么bit-band位为零。读别名后的地址将直接返回适当的bit-band位中的值。

除此之外，位带操作（bit-banding）为原子位操作，其他总线活动不能对其中断。

Cortex-M3/4存储器映射



Cortex-M3/4的非对齐数据访问和bit-banding



“传统的位处理方法和 Cortex-M3 bit-banding 的比较”

此外，基于传统ARM7 处理器的系统只支持访问对齐的数据，只有沿着对齐的字边界才可以对数据进行访问和存储。Cortex-M3处理器采用非对齐数据访问方式，使非对齐数据可以在单核访问中进行传输。当使用非对齐传输时，这些传输将转换为多个对齐传输，但这一过程不为程序员所见。

FESC

嵌套向量中断控制器（NVIC）

NVIC 是 Cortex-M3/4 处理器中一个完整的部分。

NVIC最多可支持 240 个外部中断，每个外部中断最多可具有 256 个可重新动态划分的不同优先级别。 它支持优先级别中断源和脉冲中断源。当进入中断时，处理器状态会自动保存在硬盘中，NVIC还支持末尾连锁技术

Cortex-M3/4 处理器使用一个可以重复定位的向量表，表中包含了将要执行的函数的地址，可供具体的中断处理器使用。中断被接受之后，处理器通过指令总线接口从向量表中获取地址。向量表复位时指向零，编程控制寄存器可以使向量表重新定位。

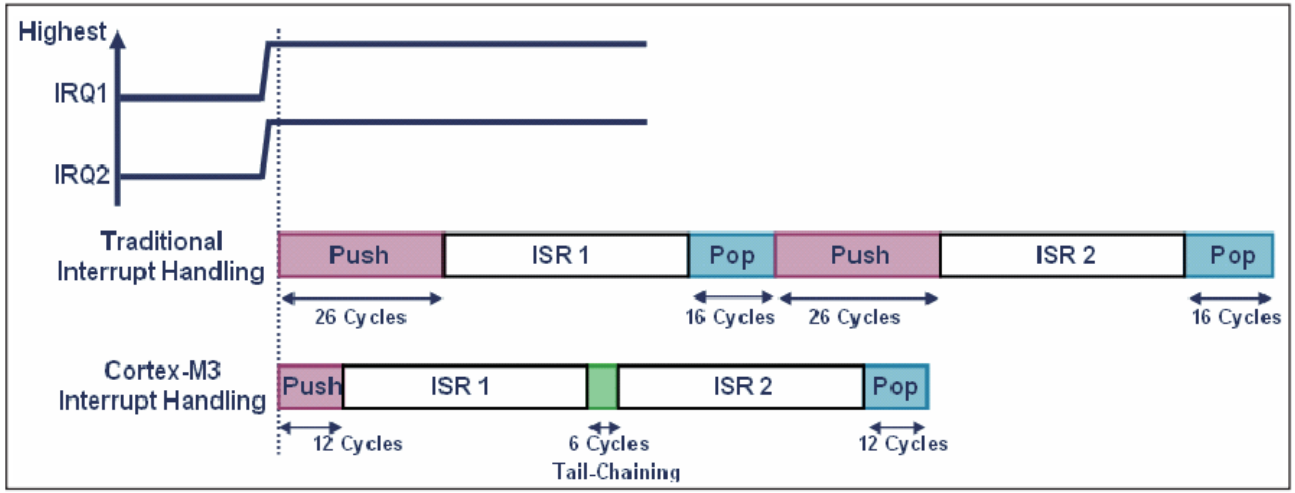
嵌套向量中断控制器（NVIC）

Exception Number	Exception Type	Priority (Default to 0 if Programmable)	Description
0	NA	NA	No exception running
1	Reset	–3 (Highest)	Reset
2	NMI	–2	NMI (external NMI input)
3	Hard fault	–1	All fault conditions, if the corresponding fault handler is not enabled
4	MemManage fault	Programmable	Memory management fault; MPU violation or access to illegal locations
5	Bus fault	Programmable	Bus error (prefetch abort or data abort)
6	Usage fault	Programmable	Program error
7–10	Reserved	NA	Reserved
11	SVCall	Programmable	Supervisor call
12	Debug monitor	Programmable	Debug monitor (break points, watchpoints, or external debug request)
13	Reserved	NA	Reserved
14	PendSV	Programmable	Pendable request for system service
15	SYSTICK	Programmable	System tick timer
16	IRQ #0	Programmable	External interrupt #0
17	IRQ #1	Programmable	External interrupt #1
…	…	…	…
255	IRQ #239	Programmable	External interrupt #239

嵌套向量中断控制器（NVIC）：

可以在硬件中处理堆栈操作，Cortex-M3处理器免去了在传统的 C语言中断服务程序中为了完成堆栈处理所要编写的汇编程序包，这使应用程序的开发变得更加简单。

Cortex-M3/4 处理器使用*末尾连锁（tail-chaining）技术*简化了激活的和未决的中断之间的移动。末尾连锁技术把需要用时 30 个时钟周期才能完成的连续的堆栈弹出和压入操作替换为6个周期就能完成的指令取指，实现了延迟的降低。处理器状态在进入中断时自动保存，在中断退出时自动恢复，比软件执行用时更少，大大提高了频率为 100MHz 的子系统的性能。



▲ 图7 NVIC中的末尾连锁(Tail chaining)技术

FESC

Cortex-M支持的Thumb-2指令：

ARM公司在其Cortex-M内核中嵌入新的Thumb-2指令集。新的Thumb-2内核技术保留了紧凑代码质量并与现有ARM方案的代码兼容性，提供改进的性能和能量效率。

Thumb-2是一种新型混合指令集，融合了16位和32位指令，用于实现密度和性能的最佳平衡。在不对性能进行折中的情况下，节省许多高集成度系统级设计的总体存储成本。

Cortex-M支持的Thumb-2指令

目标：看到一段汇编的代码时，会去查处相关的指令集，读懂代码的意图/作用即可。

Thumb-2指令的优势

- 免去 Thumb和ARM代码的互相切换，对于早期的处理器来说，这种状态切换会降低性能。
- Thumb-2指令集的设计是专门面向C语言的，且包括If/Then结构（预测接下来的四条语句的条件执行）、硬件除法以及本地位域操作。（复位向量有堆栈MSP初值。。。）
- Thumb-2指令集提供CLZ、RBIT指令，计算前导零指令和位反转指令，组合使用很强大
- Thumb-2指令集提供SEV、WFE、WFI指令，发送事件、等待事件、等待中断指令，多核任务同步

Cortex-M 的调试

Cortex-M处理器不再直接提供JTAG接口，而是提供一个DAP调试访问接口，在实际芯片中，可以连接不同的DP调试端口设备，实现包括传统JTAG到串行线的各种调试方式，因而支持多种开发工具：

仿真器

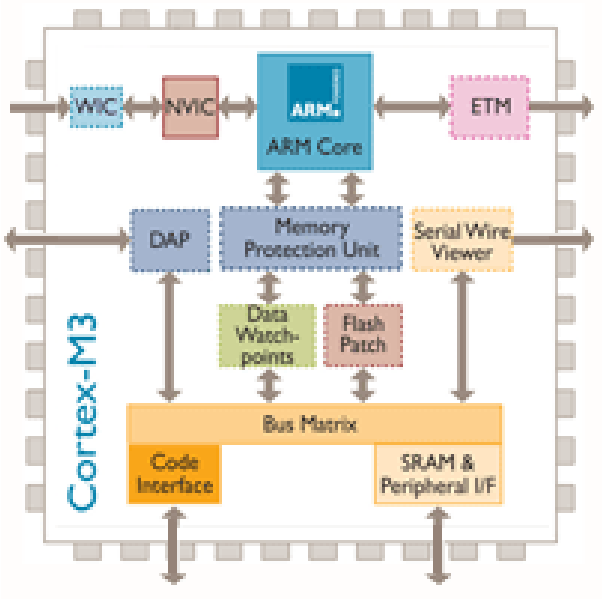
调试器

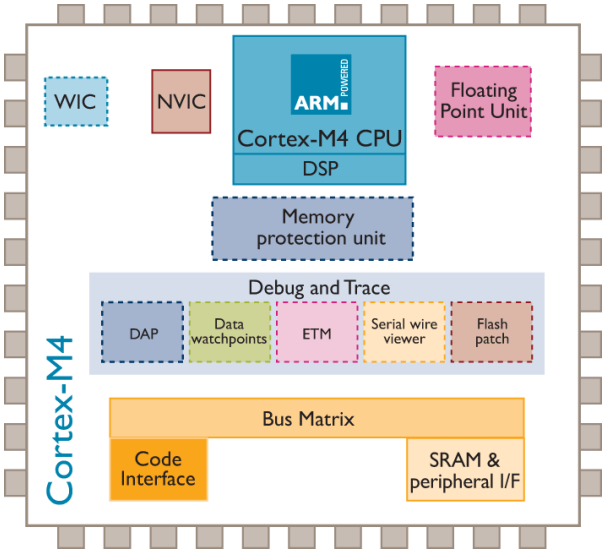
JTAG调试器

调试器


编程器

ARM Cortex M3 to M4





The Cortex-M4 features a single-cycle multiply-accumulate (MAC) unit, optimized single instruction multiple data (SIMD) instructions, saturating arithmetic instructions and an optional single precision Floating-Point Unit (FPU).

FESC

ARM7 vs Cortex-M3

特性	ARM7TDMI-S	Cortex-M3
架构	ARMv4T（冯·诺依曼）	ARMv7-M（哈佛）
ISA 支持	Thumb / ARM	Thumb / Thumb – 2
流水线	3 级	3 级+分支预测
中断	FIQ / IRQ	NMI + 1到 240 个物理中断
中断延迟	24-42 个时钟周期	12 个时钟周期
休眠模式	无	集成
内存保护	无	8 区域内存保护单元
Dhrystone	0.95 DMIPS/MHz（ARM 模式）	1.25 DMIPS/MHz
功耗	0.28mW/MHz	0.19mW/MHz
面积	0.62mm^2（仅内核）	0.86mm^2（内核+外设）*

* 不包含可选系统外设（MPU和ETM）或者集成的部件

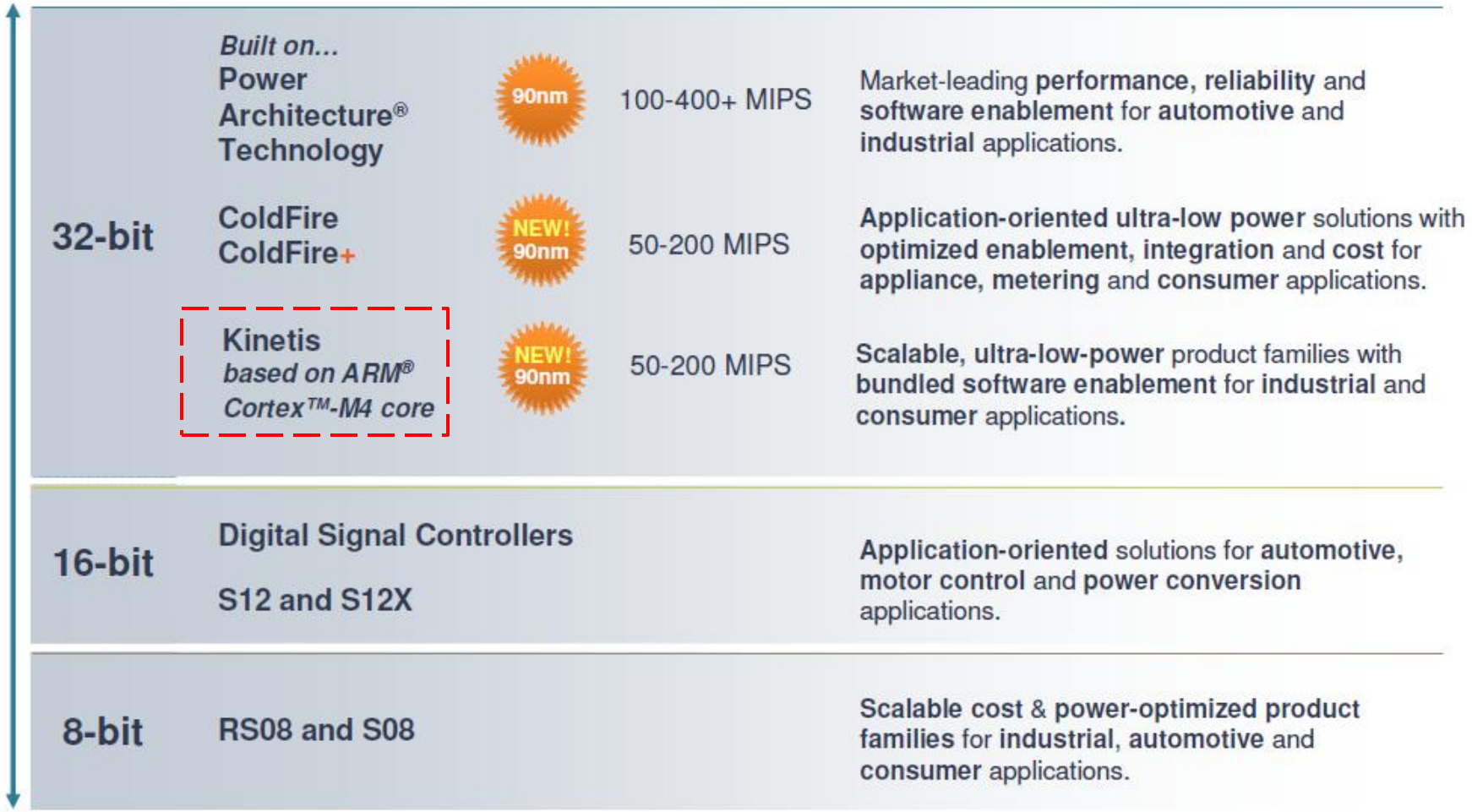
▲ 表 1-1 ARM7TDMI-S和Cortex-M3比较（采用100MHz频率和TSMC 0.18G工艺）

FESC

学习掌握 ARM Cortex 的思路

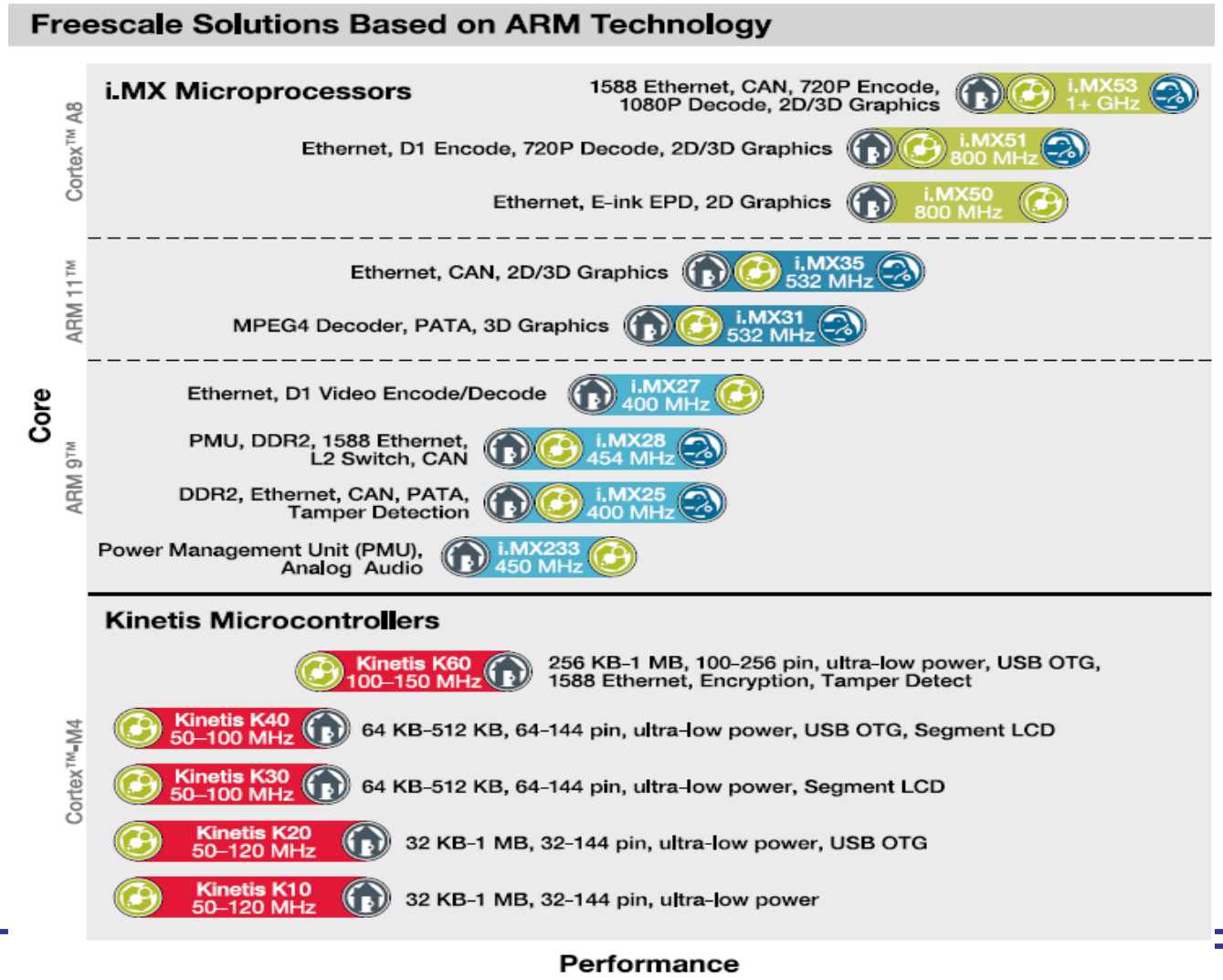
- 自下而上与自上而下
  - 8位MCU教学使用传统自下而上的思路
    - CPU寄存器、指令集、汇编、C……
  - ARM发展到Cortex，相当于从微机到小型机，其CPU设计借鉴了PowerPC、MIPS等面向带多用户操作系统的理念，对其指令集、运行模式等的理解需RTOS方面的知识，如优先级、共享资源、竞争、信号量等
    - 应采用自上而下的思路学习，不妨先介绍一些RTOS方面的基本知识，从掌握开发工具的使用开始，读懂CW中自带的范例程序到自己写C程序，自上而下、循序渐进地理解Cortex

Freescale MCU



FESC

Freescale ARM



FESC

Freescale Kinetis

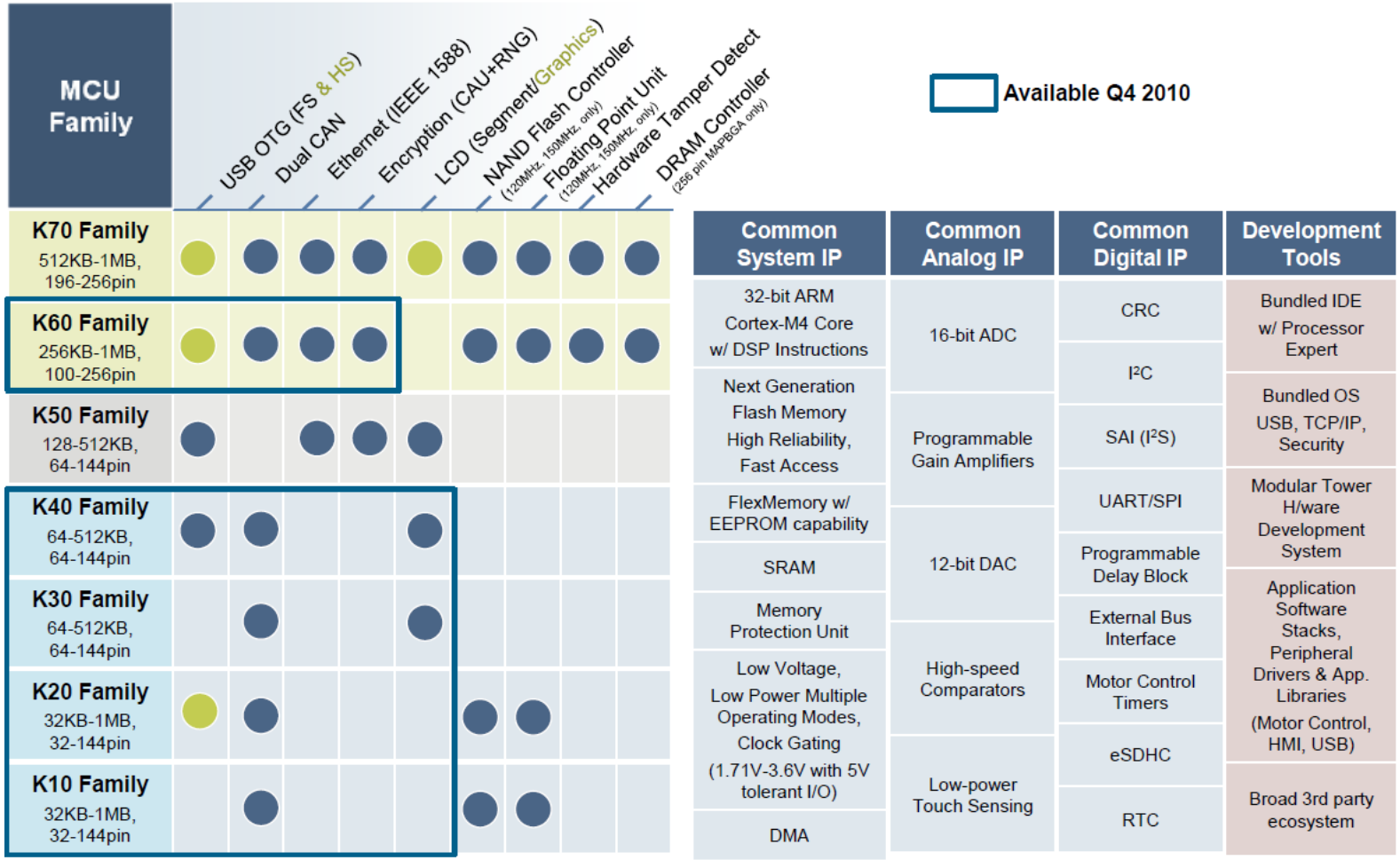
Kinetis

Design Potential. Realized.

- **Scalability** – Over 200 hardware and software compatible ARM® Cortex™-M4 MCUs with multiple low-power, connectivity, communications, HMI and security features
  - ✓"DSP" your design - increase performance and reduce power with no added cost
  - ✓Grow/cost reduce your design with easy migration within/across MCU families
- **Mixed-Signal** – Huge integration with fast 16-bit ADCs, DACs, PGAs and more
  - ✓Powerful, cost-effective signal conversion, conditioning and control capability
- **90nm Technology** – Low-power Thin-Film Storage Flash with innovative FlexMemory
  - ✓Robust, efficient flash memory - maximum on-chip feature integration
  - ✓EEPROM (on-chip!) with unmatched speed, endurance and flexibility
- **Enablement** – *Free* CodeWarrior IDE with Processor Expert and MQX RTOS. Large 3rd party tool chain support from IAR, KEIL and other ARM ecosystem providers
  - ✓*Free* Processor Expert creates application drivers easily and efficiently
  - ✓*Free* MQX RTOS creates stable, upgradeable application code with low/no –cost file system, graphics, connectivity and security plug-ins
  - ✓Reduce integration effort, development cost and time-to-market

FESC

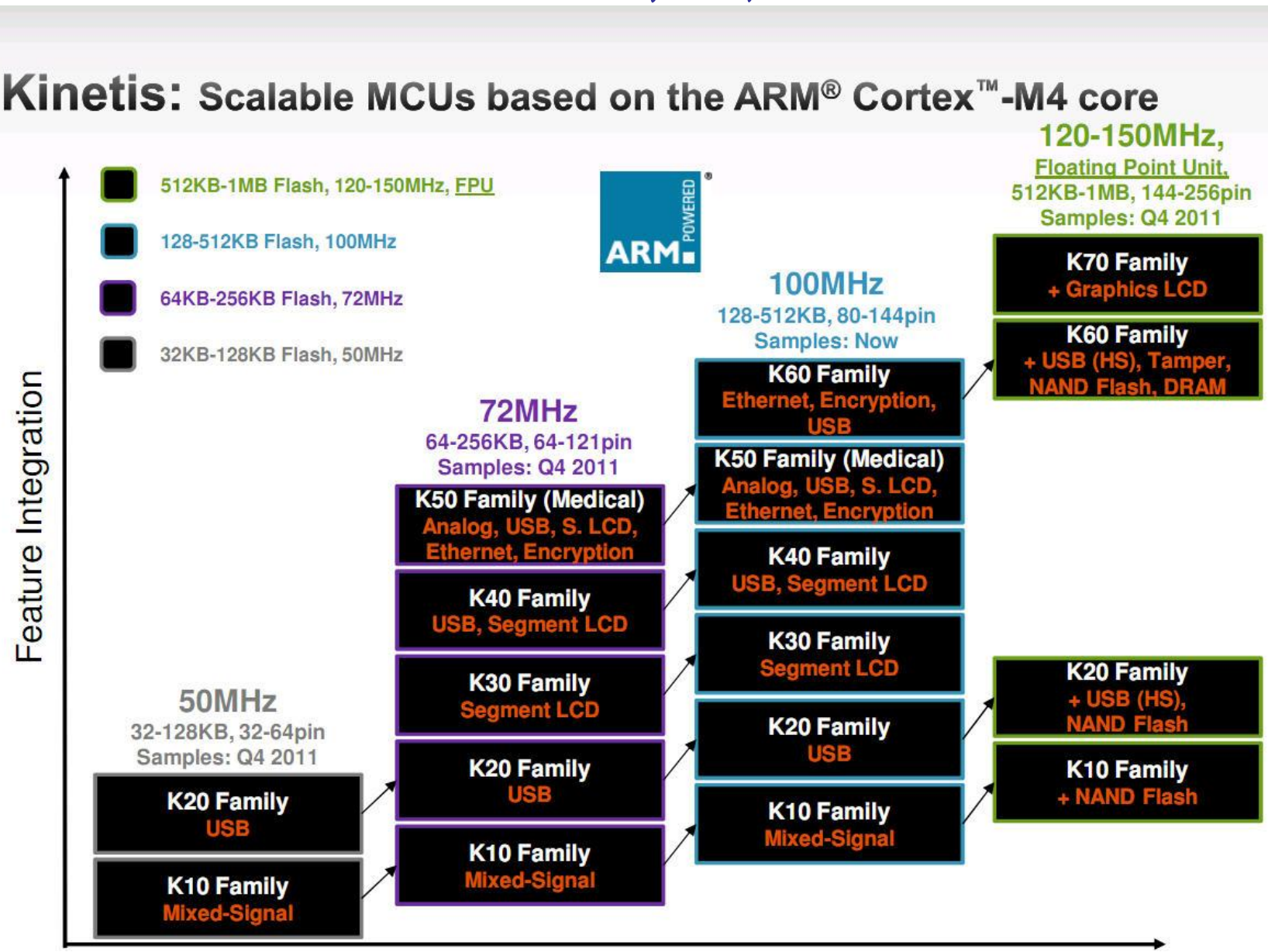
Kinetis 系列



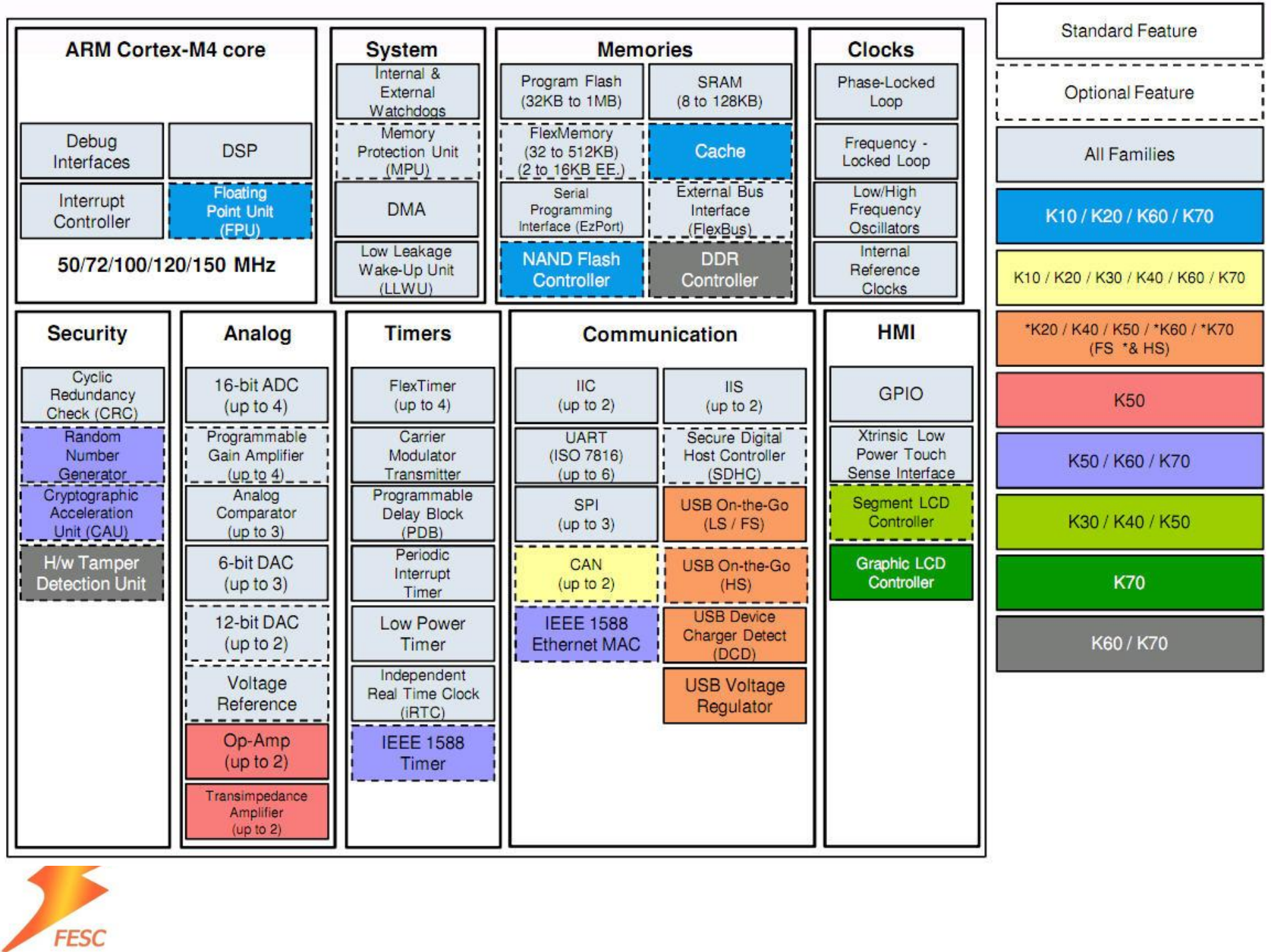
Common System IP	Common Analog IP	Common Digital IP	Development Tools
32-bit ARM Cortex-M4 Core w/ DSP Instructions	16-bit ADC	CRC	Bundled IDE w/ Processor Expert
Next Generation Flash Memory High Reliability, Fast Access	Programmable Gain Amplifiers	I²C	Bundled OS USB, TCP/IP, Security
FlexMemory w/ EEPROM capability	12-bit DAC	SAI (I²S)	Modular Tower H/ware Development System
SRAM	High-speed Comparators	UART/SPI	Application Software Stacks, Peripheral Drivers & App. Libraries (Motor Control, HMI, USB)
Memory Protection Unit	Low-power Touch Sensing	Programmable Delay Block	
Low Voltage, Low Power Multiple Operating Modes, Clock Gating (1.71V-3.6V with 5V tolerant I/O)		External Bus Interface	
DMA		Motor Control Timers	
-40 to 105C		eSDHC	Broad 3rd party ecosystem
		RTC	

FESC

Kinetis 系列



FESC


ARM Cortex-M4 core
Debug Interfaces
DSP
Interrupt Controller
Floating Point Unit (FPU)
50/72/100/120/150 MHz
System
Internal & External Watchdogs
Memory Protection Unit (MPU)
DMA
Low Leakage Wake-Up Unit (LLWU)
Memories
Program Flash (32KB to 1MB)
SRAM (8 to 128KB)
FlexMemory (32 to 512KB) (2 to 16KB EE.)
Cache
Serial Programming Interface (EzPort)
External Bus Interface (FlexBus)
NAND Flash Controller
DDR Controller
Clocks
Phase-Locked Loop
Frequency - Locked Loop
Low/High Frequency Oscillators
Internal Reference Clocks
Security
Cyclic Redundancy Check (CRC)
Random Number Generator
Cryptographic Acceleration Unit (CAU)
H/w Tamper Detection Unit
Analog
16-bit ADC (up to 4)
Programmable Gain Amplifier (up to 4)
Analog Comparator (up to 3)
6-bit DAC (up to 3)
12-bit DAC (up to 2)
Voltage Reference
Op-Amp (up to 2)
Transimpedance Amplifier (up to 2)
Timers
FlexTimer (up to 4)
Carrier Modulator Transmitter
Programmable Delay Block (PDB)
Periodic Interrupt Timer
Low Power Timer
Independent Real Time Clock (iRTC)
IEEE 1588 Timer
Communication
IIC (up to 2)
IIS (up to 2)
UART (ISO 7816) (up to 6)
Secure Digital Host Controller (SDHC)
SPI (up to 3)
USB On-the-Go (LS / FS)
CAN (up to 2)
USB On-the-Go (HS)
IEEE 1588 Ethernet MAC
USB Device Charger Detect (DCD)
USB Voltage Regulator
HMI
GPIO
Xtrinsic Low Power Touch Sense Interface
Segment LCD Controller
Graphic LCD Controller
Standard Feature
Optional Feature
All Families
K10 / K20 / K60 / K70
K10 / K20 / K30 / K40 / K60 / K70
*K20 / K40 / K50 / *K60 / *K70 (FS *& HS)
K50
K50 / K60 / K70
K30 / K40 / K50
K70
K60 / K70

FESC

Kinetis: Package Options

81MAPBGA
8 x 8 mm
0.65mm pitch
(K10/20/30/40/50)

104MAPBGA
8 x 8 mm
0.65mm pitch
(K10/20/30/40/50)

121MAPBGA
8 x 8 mm
0.65mm pitch
(K10/20/30/40/50/60)

144MAPBGA
13 x 13 mm
1.0mm pitch
(K10/20/30/40/50/60)

196MAPBGA
15 x 15 mm
1.0mm pitch
(K60/70)

256MAPBGA
17 x 17 mm
1.0mm pitch
(K60/70)

48LQFP
7 x 7 mm
0.55mm pitch
(K10/20)

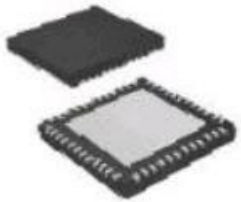
64LQFP
10 x 10 mm
0.5mm pitch
(K10/20/30/40/50)

80LQFP
12 x 12 mm
0.5mm pitch
(K10/20/30/40/50)

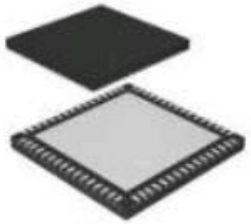
100LQFP
14 x 14 mm
0.5mm pitch
(K10/20/30/40/50/60)

144LQFP
20 x 20 mm
0.5mm pitch
(K10/20/30/40/50/60)

32QFN
5 x 5 mm
0.5mm pitch
(K10/20)



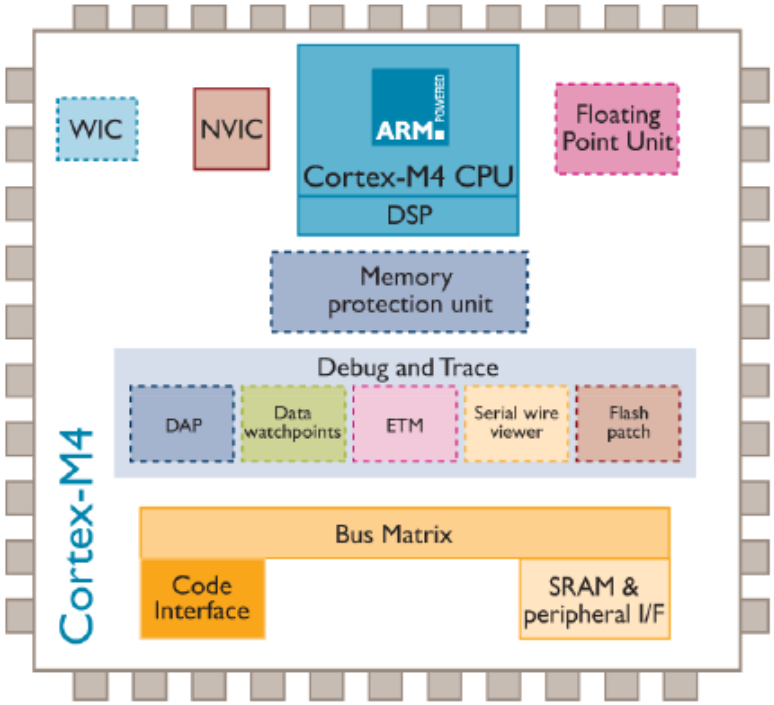
48QFN
7 x 7 mm
0.5mm pitch
(K10/20)



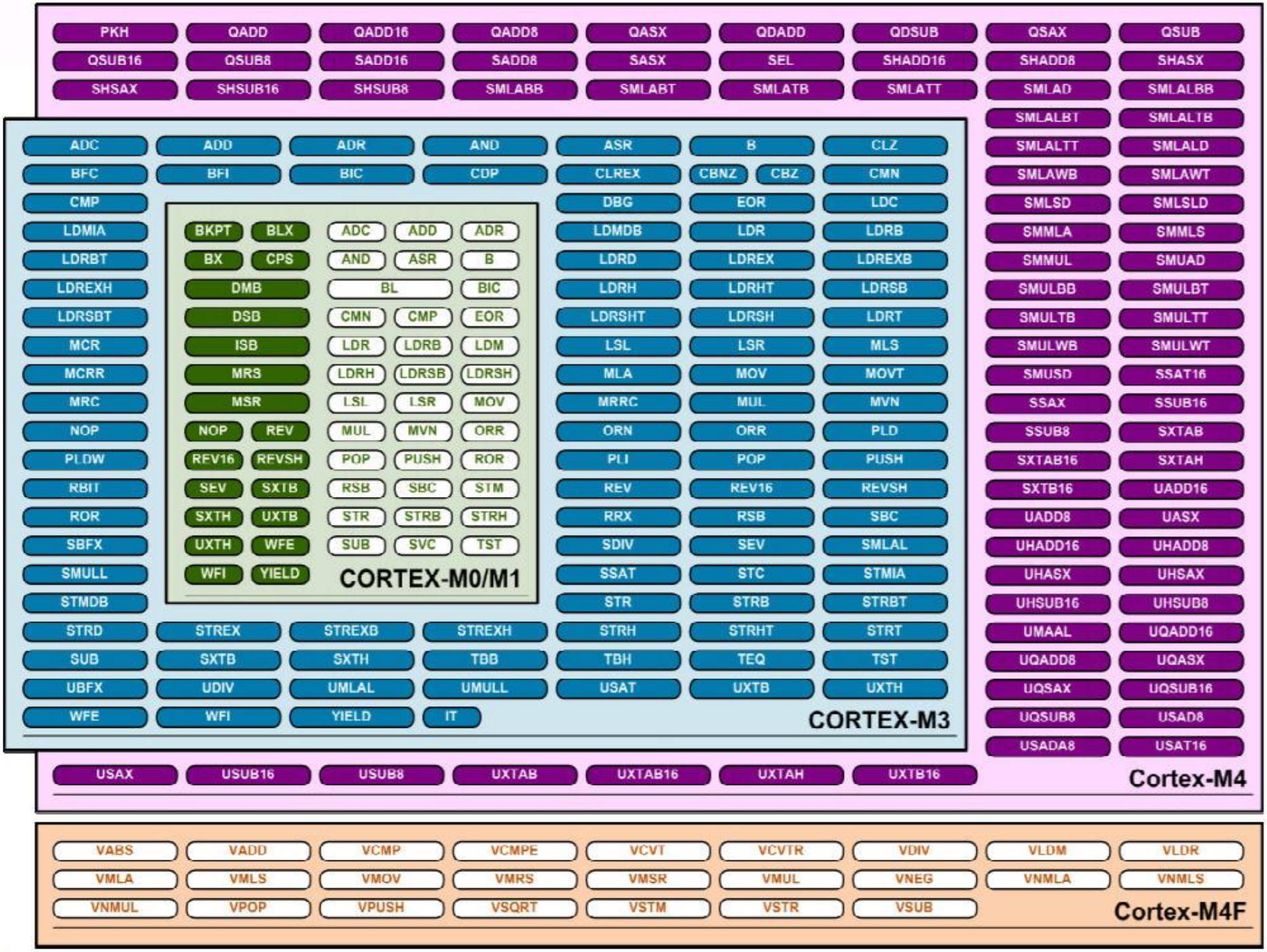
64LQFN
9 x 9 mm
0.5mm pitch
(K10/20/30/40/50)

ARM Cortex-M4 from Freescale

- 向下兼容**ARM Cortex-M3**
- **新特性**
  - 单周期MAC (最高支持32 x 32，结果为32-bit)
  - DSP扩展
  - 单精度浮点处理单元
- **飞思卡尔IP和创新**
  - 片内指令和数据缓存
  - 交换机可用于并发访问多个主设备/从设备
  - 片内DMA用于降低CPU负载
  - Low-leakage唤醒单元为低功耗操作增加了便利
- **为数字信号处理而构建**
  - **电机控制** – 高级算法，长寿命，电源效率
  - **自动控制** – 以较低成本实现高带宽的计算和算法
  - **电源管理** – 为低功耗或电池供电系统而设计
  - **音频和视频** – 提升5倍软件性能，提高电池续航能力



FESC


PKH
QADD
QADD16
QADD8
QASX
QDADD
QDSUB
QSAX
QSUB
QSUB16
QSUB8
SADD16
SADD8
SASX
SEL
SHADD16
SHADD8
SHASX
SHSAX
SHSUB16
SHSUB8
SMLABB
SMLABT
SMLATB
SMLATT
SMLAD
SMLALBB
SMLALBT
SMLALTB
SMLALTT
SMLALD
SMLAWB
SMLAWT
SMLSD
SMLSLD
SMMLA
SMMLS
SMMUL
SMUAD
SMULBB
SMULBT
SMULTB
SMULTT
SMULWB
SMULWT
SMUSD
SSAT16
SSAX
SSUB16
SSUB8
SXTAB
SXTAB16
SXTAH
SXTB16
UADD16
UADD8
UASX
UHADD16
UHADD8
UHASX
UHSAX
UHSUB16
UHSUB8
UMAAL
UQADD16
UQADD8
UQASX
UQSAX
UQSUB16
UQSUB8
USAD8
USADA8
USAT16
ADC
ADD
ADR
AND
ASR
B
CLZ
BFC
BFI
BIC
CDP
CLREX
CBNZ
CBZ
CMN
CMP
DBG
EOR
LDC
LDMIA
LDMDB
LDR
LDRB
LDRBT
LDRD
LDREX
LDREXB
LDREXH
LDRH
LDRHT
LDRSB
LDRSBT
LDRSHT
LDRSH
LDRT
MCR
LSL
LSR
MLS
MCRR
MLA
MOV
MOVT
MRC
MRRC
MUL
MVN
NOP
ORN
ORR
PLD
PLDW
PLI
POP
PUSH
RBIT
REV
REV16
REVSH
ROR
RRX
RSB
SBC
SBFX
SDIV
SEV
SMLAL
SMULL
SSAT
STC
STMIA
STMDB
STR
STRB
STRBT
STRD
STREX
STREXB
STREXH
STRH
STRHT
STRT
SUB
SXTB
SXTH
TBB
TBH
TEQ
TST
UBFX
UDIV
UMLAL
UMULL
USAT
UXTB
UXTH
WFE
WFI
YIELD
IT
CORTEX-M3
BKPT
BLX
ADC
ADD
ADR
BX
CPS
AND
ASR
B
DMB
BL
BIC
DSB
CMN
CMP
EOR
ISB
LDR
LDRB
LDM
MRS
LDRH
LDRSB
LDRSH
MSR
LSL
LSR
MOV
NOP
REV
MUL
MVN
ORR
REV16
REVSH
POP
PUSH
ROR
SEV
SXTB
RSB
SBC
STM
SXTH
UXTB
STR
STRB
STRH
UXTH
WFE
SUB
SVC
TST
WFI
YIELD
CORTEX-M0/M1
USAX
USUB16
USUB8
UXTAB
UXTAB16
UXTAH
UXTB16
Cortex-M4
VABS
VADD
VCMP
VCMPE
VCVT
VCVTR
VDIV
VLDM
VLDR
VMLA
VMLS
VMOV
VMRS
VMSR
VMUL
VNEG
VNMLA
VNMLS
VNMUL
VPOP
VPUSH
VSQRT
VSTM
VSTR
VSUB
Cortex-M4F

Feature set comparison chart

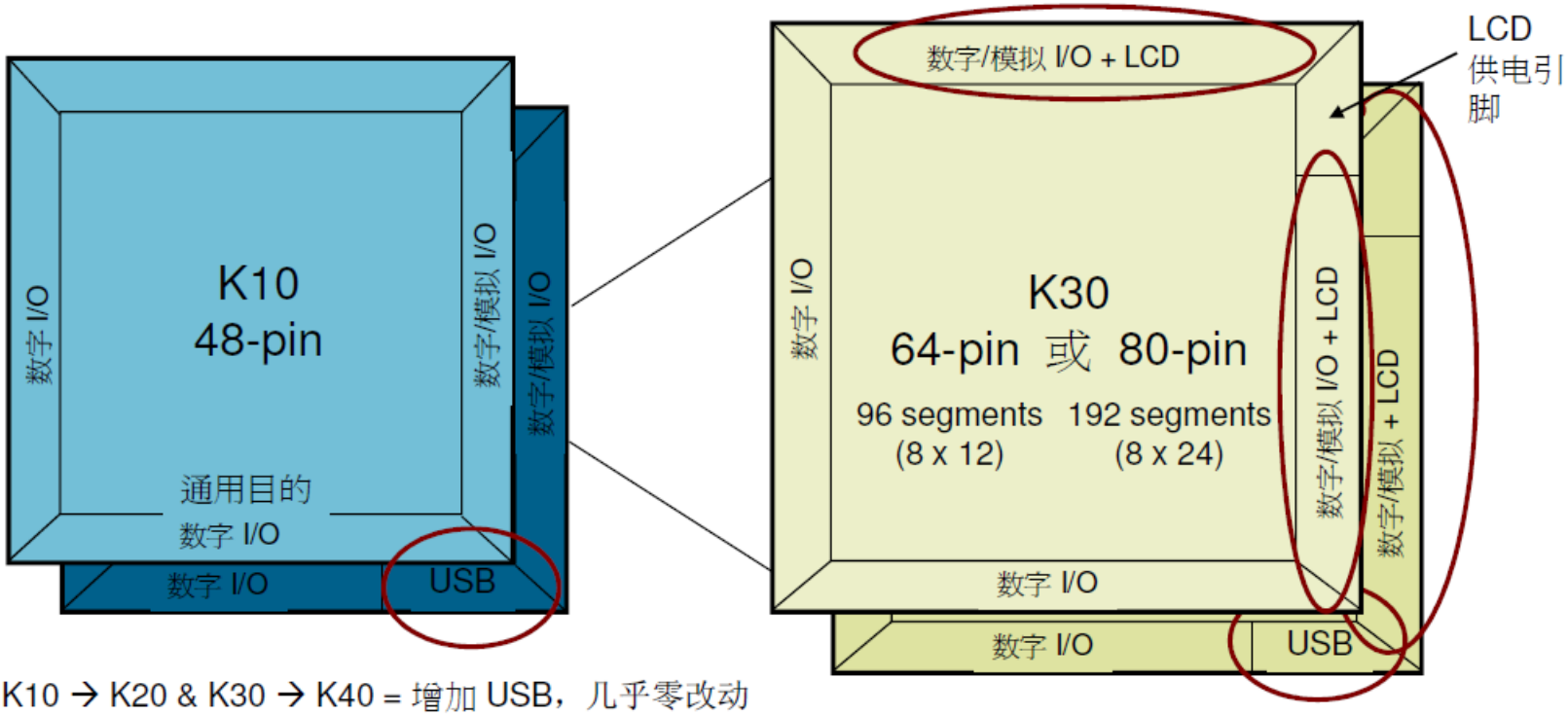
	ARM7TDMI	Cortex-M0	Cortex-M3	Cortex-M4
Architecture Version	v4T	v6-M	v7-M	v7-M
Instruction set architecture	ARM, Thumb	Thumb, Thumb-2 System Instructions	Thumb + Thumb-2	Thumb + Thumb-2, DSP, SIMD, FP
DMIPS/MHz	0.72 (Thumb), 0.95 (ARM)	0.9	1.25	1.25
Bus interfaces	None	1	3	3
Integrated NVIC	No	Yes	Yes	Yes
Number interrupts	2 (IRQ and FIQ)	1-32 + NMI	1-240 + NMI	1-240 + NMI
Interrupt priorities	None	4	8-256	8-256
Breakpoints, Watchpoints	2 Watchpoint Units	4/2/0, 2/1/0	8/4/0, 2/1/0	8/4/0, 2/1/0
Memory Protection Unit (MPU)	No	No	Yes (Option)	Yes (Option)
Integrated trace option (ETM)	Yes (Option)	No	Yes (Option)	Yes (Option)
Fault Robust Interface	No	No	Yes (Option)	No
Single Cycle Multiply	No	Yes (Option)	Yes	Yes
Hardware Divide	No	No	Yes	Yes
WIC Support	No	Yes	Yes	Yes
Bit banding support	No	No	Yes	Yes
Single cycle DSP/SIMD	No	No	No	Yes
Floating point hardware	No	No	No	Yes
Bus protocol	Use AHB bus wrapper	AHB Lite	AHB Lite, APB	AHB Lite, APB
CMSIS Support	No	Yes	Yes	Yes

ARM Cortex-M4 from Freescale

- **16-bit逐次逼近ADC**
  - 1.15V 最小参考电压
  - 差分或单端
  - 1, 4, 8, 16或32次平均
  - 自动比较功能
  - 与DAC同步触发
  - 可配置的精度, 采样时间、采样速度和功耗 (8/10/12/16位精度)
  - 每个ADC转换器最高支持20个通道
- **12-bit DAC**
  - 16字DAC FIFO
  - 硬件或软件触发
- **高速比较器**
  - 可编程迟滞控制和中断触发
  - 可选择的比较输出反转
  - 集成6-bit参考DAC
- **可编程增益放大器**
  - 64倍放大
- **参考电压 (Vref)**
  - 可校准
  - < 33ppm/ºC 温度变化(0° -50° C 温度范围)

FESC

Pin Compatibility Across Families



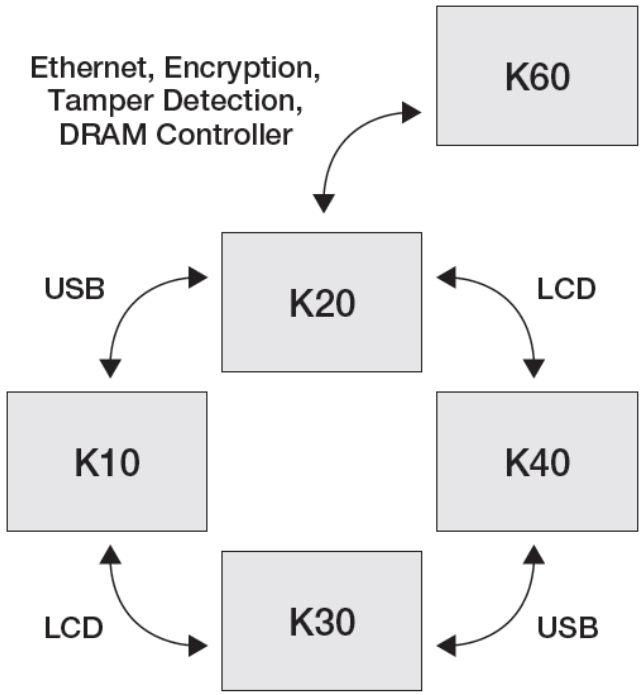
K10 → K20 & K30 → K40 = 增加 USB，几乎零改动
- ✓唯一的区别是增加4个USB引脚和减少4个数字I/O引脚

K10 → K30 & K20 → K40 = 增加段码式LCD，最小的布板改动
- ✓数字和模拟 I/O信号保持不变
- ✓段码式LCD信号与现有的数字模拟 I/O 信号复用
- ✓大多数数字 I/O 信号与段码式LCD信号复用 可通过大封装增加引脚

K20 → K60 = 增加以太网引脚，而无任何改动
- ✓所有以太网信号与现有的数字模拟I/O信号复用

FESC

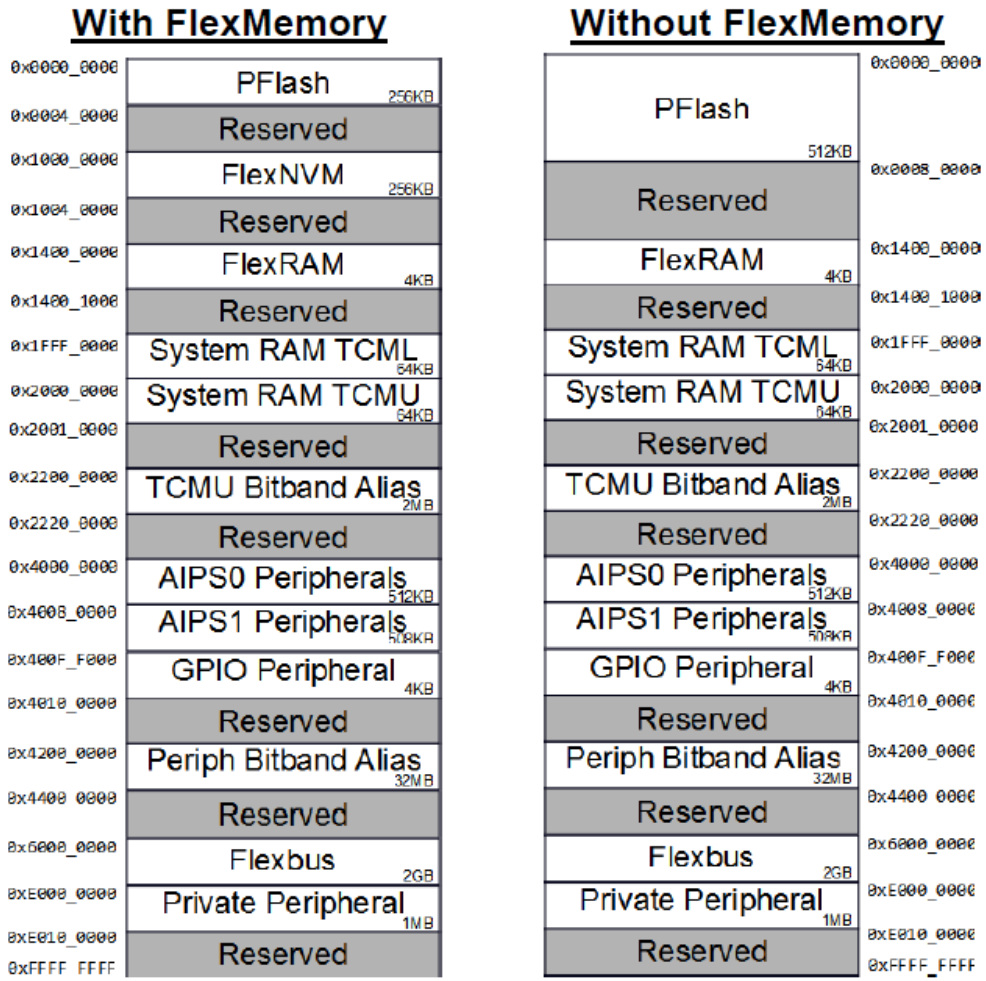
Pin Compatibility Across Families



Type	Body Size	Pitch	Families
32-pin QFN	5 x 5 mm	0.5 mm	K10, K20
48-pin QFN	7 x 7 mm	0.5 mm	K10, K20
48-pin LQFP	7 x 7 mm	0.5 mm	K10, K20
64-pin QFN	9 x 9 mm	0.5 mm	K10, K20, K30, K40
64-pin LQFP	10 x 10 mm	0.5 mm	K10, K20, K30, K40
80-pin LQFP	12 x 12 mm	0.5 mm	K10, K20, K30, K40
81-pin MAPBGA	8 x 8 mm	0.65 mm	K10, K20, K30, K40
100-pin LQFP	14 x 14 mm	0.5 mm	K10, K20, K30, K40, K60
104-pin MAPBGA	8 x 8 mm	0.65 mm	K10, K20, K30, K40, K60
144-pin LQFP	20 x 20 mm	0.5 mm	K10, K20, K30, K40, K60
144-pin MAPBGA	13 x 13 mm	1.0 mm	K10, K20, K30, K40, K60
196-pin MAPBGA	15 x 15 mm	1.0 mm	K60
256-pin MAPBGA	17 x 17 mm	1.0 mm	K60

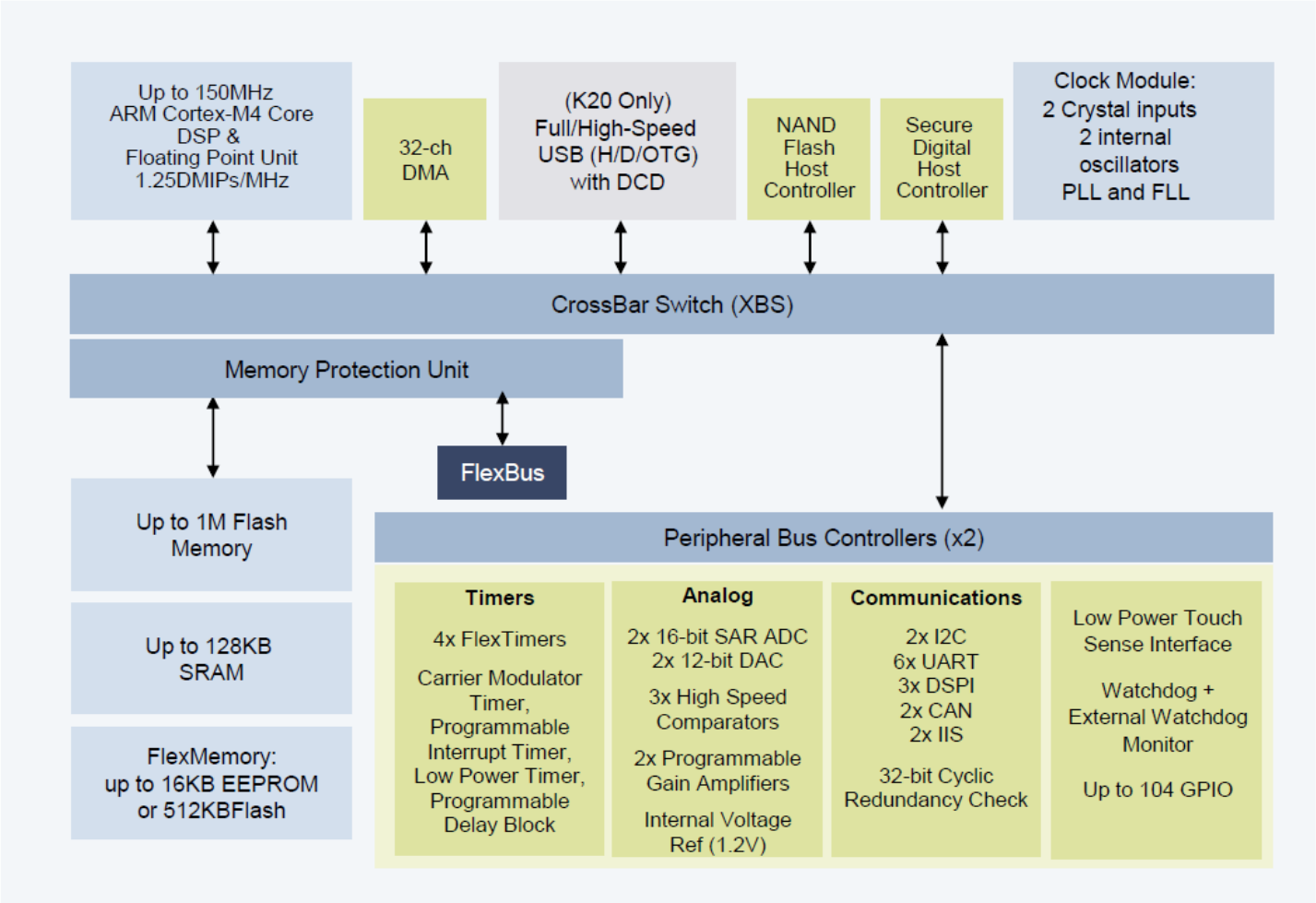
FESC

Memory Map of Kinetis Families



FESC

The K10 Family Block Diagram



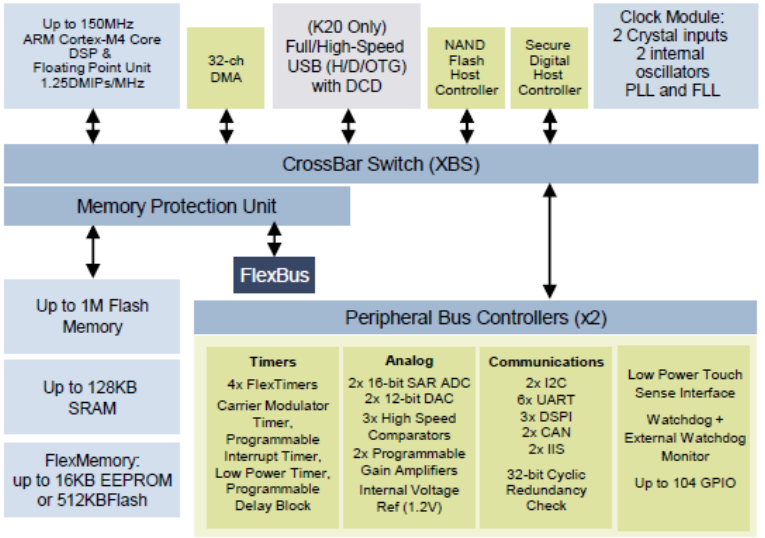
FESC

The K10 Family Overview

High Integration Mixed-Signal MCUs

- **Processing Performance and FlexMemory**
  - Direct Memory Access, Cross Bar Switch, and on-chip Cache maximize bus bandwidth and Flash execution
  - FlexMemory provides on-chip, high-endurance configurable EEPROM and/or additional Flash memory
- **(K20 Only) Connect via USB AND charge a battery**
  - USB 2.0 Full-Speed Device/Host/OTG Controller with integrated transceiver, HS via ULPI interface
  - Includes Device Charge Detector (DCD) and Regulator to supports battery charging via USB for Portable Devices
- **Flexible and Powerful Mixed Signal Capability**
  - 16-bit ADC enables small signal capture for medical/sensing applications, or high speed conversions for motor control.
  - 12-bit DAC, High-Speed Comparator, and Voltage Reference on-chip reduces system cost
- **Ultra-low power with 1.71V operation**
  - Multiple low power modes and Flash & analog operation down to 1.71V – power profile optimization and prolonged battery life
  - Stop Currents <500nA, run currents <200uA/MHz

32KB Flash in 32 pin package starting at $0.99 for 10K SRP



Enablement Bundle

TOWER development system
Complementary MQX RTOS with USB Stack
Eclipse-Based CodeWarrior 10.0 IDE
Processor Expert Rapid Application Development Tool
IAR, Keil and full ARM Ecosystem Support
Motor Control and DSP Libraries

Family	USB OTG + DCD
K10	-
K20	X

FESC

K10 主要性能

- Voltage range: 1.71 to 3.6 V，5 V tolerant GPIO
- Up to 100 MHz(120 MHz) with DSP，instructions ~1.25 Dhrystone MIPS /MHz
- 32~1MB flash/8K~128 KB RAM
- 16-bit ADCs, 12-bit DACs, 增益可编程放大器,电容式触摸键盘接口
- UARTs with ISO7816 and IrDA support, I2S, CAN, I2C and DSPI，Modulator Transmitter for IR waveform generation
- Powerful Flex Timers which support general purpose, PWM, and motor control functions
- Timer for RTOS，
- temperature ranges from -40 °C to 105 °C

FESC

K10 系列可选

引脚：32/48/64/80/100/104/121/144

K10 Family Options

Part Number	Memory					Features									Packages											
	CPU (MHz)	Flash (KB)	Flex NVM (KB)	SRAM (KB)	Cache (KB)	Single Precision Floating Point Unit	Memory Protection	CAN	Secure Digital Host	NAND Flash Controller	External Bus Interface	12-bit DAC	Prog. Gain Amplifier	5V Tolerant I/O	FM	FT	LF	EX	LH	LK	MB	LL	ML	MC	LQ	MD
															32 QFN (5x5)	48QFN (7X7)	48LQFP (7X7)	64QFN (9X9)	64LQFP (10X10)	80LQFP (12X12)	81BGA (8X8)	100LQFP (14X14)	104BGA (8X8)	121BGA (8x8)	144LQFP (20x20)	144BGA (13x13)
MK10DN32Vyy5	50	32		8											√	√	√	√	√							
MK10DN64Vyy5	50	64		16											√	√	√	√	√							
MK10DN128Vyy5	50	128		16											√	√	√	√	√							
MK10DN512Vw10	100	512		128			√	√	√		√	√	√	√						√	√	√		√	√	√
MK10FN1M0Vyy12	120	1 MB		128	16	√	√	√	√	√	√	√	√	√											√	√
MK10DX32Vyy5	50	32	32	8											√	√	√	√	√							
MK10DX64Vyy5	50	64	32	16											√	√	√	√	√							
MK10DX128Vyy5	50	128	32	16											√	√	√	√	√							
MK10DX64Vyy7	72	64	32	16				√			√	√	√	√				√	√	√	√					
MK10DX128Vyy7	72	128	32	32				√			√	√	√	√				√	√	√	√	√	√			
MK10DX256Vyy7	72	256	32	64				√			√	√	√	√				√	√	√	√	√	√			
MK10DX128Vyy10	100	128	128	32			√	√	√		√	√	√	√											√	√
MK10DX256Vyy10	100	256	256	64			√	√	√		√	√	√	√											√	√
MK10FX512Vyy12	120	512	512	128	16	√	√	√	√	√	√	√	√	√											√	√

FESC

Motor Control Use Case

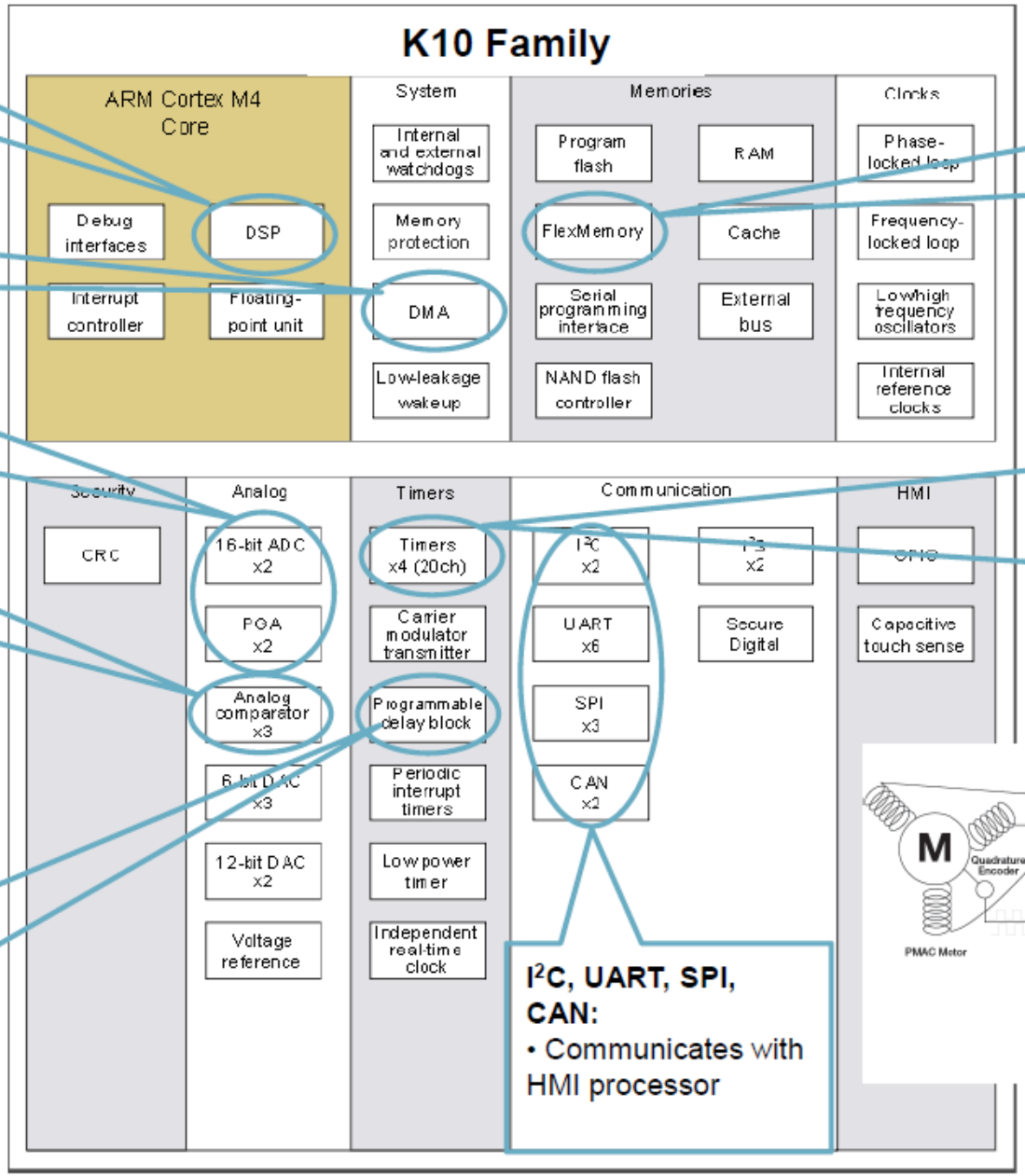
DSP hardware:
► Accelerates motor control calculations

DMA:
► Off loads CPU from repetitive data transfers

16-bit ADC & PGA:
► Measures 3 phase bridge current and voltage

Analog Comparator:
► Detects back EMF
► Monitors over current

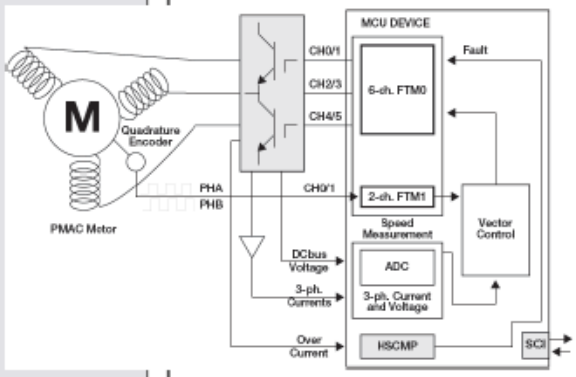
Programmable delay block:
► Schedules delayed ADC conversions relative to Timer triggers



FlexMemory:
► Saving motor calibration data
• Remote update bootloader

Timers:
► Drives various motor types including stepper, BLDC, and PMAC motors with sensor or sensorless algorithms
► Built-in quadrature decoder detects motor speed

I²C, UART, SPI, CAN:
• Communicates with HMI processor



100 Pin K10LL 的I/O

- ~70个I/O端口（GPIO）
  - TSI 16
  - ADC 16
  - DAC 1
  - ACP 3
  - PWM 8
  - UART 4
  - I2C 2
  - I2S 1
  - SPI 3
  - CAN 2

16-bit ADC

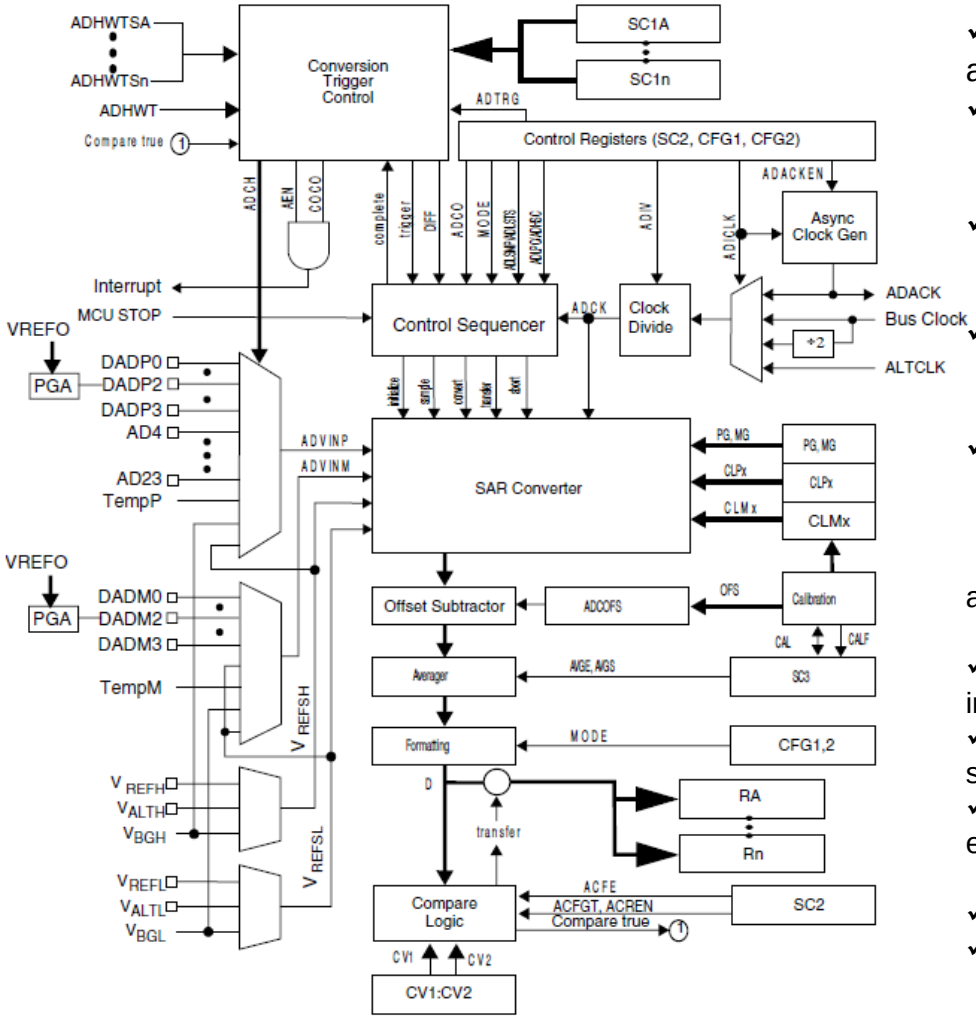


Figure 34-1. ADC block diagram

✓ Up to **4 pairs of differential** and 24 single-ended external analog inputs

✓ Output modes:

- differential 16-bit, 13-bit, 11-bit or 9-bit
- single-ended 16-bit, 12-bit, 10-bit and 8-bit

✓ **Programmable Gain Amplifier** (PGA) : up to **x64** gain

- Amplify low-amplitude signals before they are fed to ADC
- Only work with differential input (range from 0~1.2V ± 10mv)

✓**ADC conversion clk frequency :**

-1~18MHz for ≤ 13-bit mode

- 2~12Mhz for 16-bit mode

✓ **ADC conversion rate:**

18.484~818.33 Ksps for ≤ 13-bit mode

37.037~361.402Ksps for ≤ 13-bit mode

(continous conversion, peripheral clk=50MHz, no ADC hardware averaging)

✓ Conversion complete / hardware average complete flag and interrupt

✓ Selectable hardware conversion trigger with hardware channel select

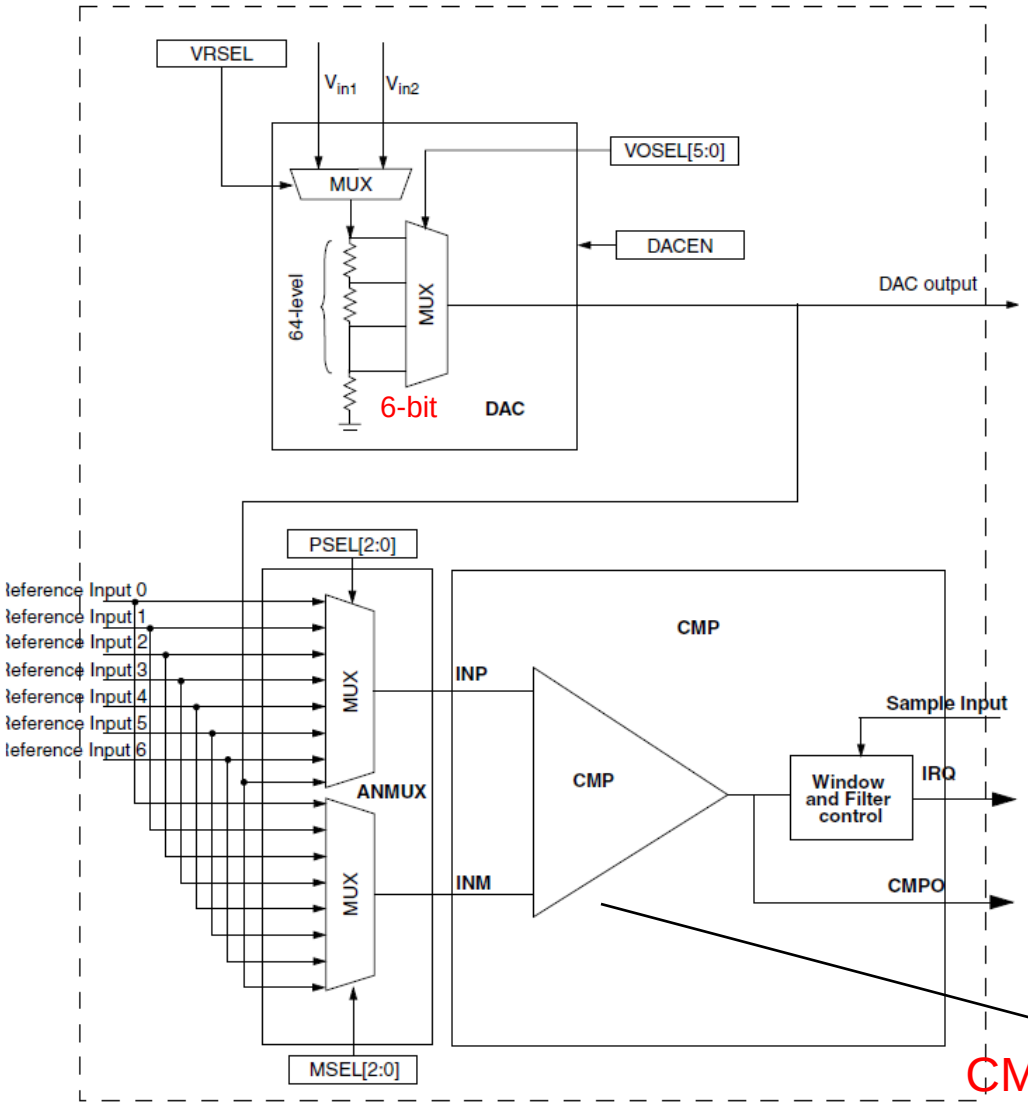
✓ Automatic compare with interrupt for less-than, greater-than or equal-to, within range, or out-of-range, programmable value

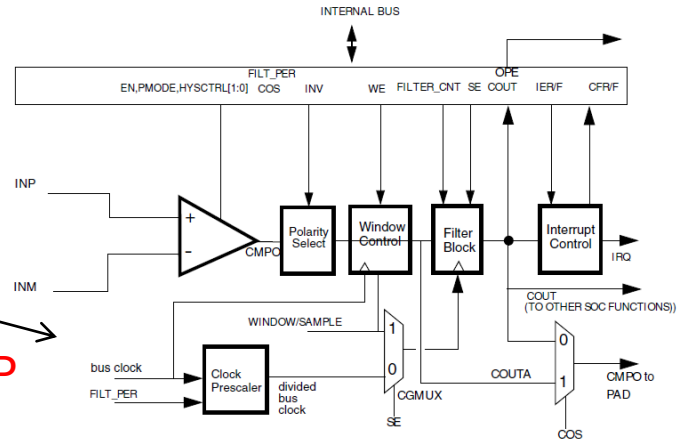
✓ Hardware average function

✓ Self-calibration mode

FESC

Analog Comparator





- ✓ Operates over the entire supply range
- ✓ Programmable hysteresis control
- ✓Selectable interrupt on rising edge, falling edge, or both rising or falling edges of comparator output
- ✓ Selectable inversion on comparator output
- ✓ Comparator output may be:
  - Sampled
  - Windowed
  - Digitally Filtered
    - * Filter can be bypassed
    - * Can be clocked via external SAMPLE signal or scaled bus clock
- ✓ Support DMA transfer
  - A comparison event can be selected to trigger a DMA transfer.
- ✓ Two software selectable performance levels:
  - Shorter propagation delay at the expense of higher power Td = 50ns (typ.)
  - Low power, with longer propagation delay Td = 250ns (typ.)

FESC

Voltage Reference(VREFV1)

- ✓ Intended to supply an accurate 1.2 V voltage output.
- ✓ VREFV1 can be used in medical applications such as glucose meters to provide a reference voltage to biosensors or as a reference to analog peripherals such as the ADC, DAC, or CMP.
- ✓ Low power mode: VREFV1 can only be used for internal peripheral
  High power mode: VREFV1 can be used for external peripheral, 100nF capacitor needed.

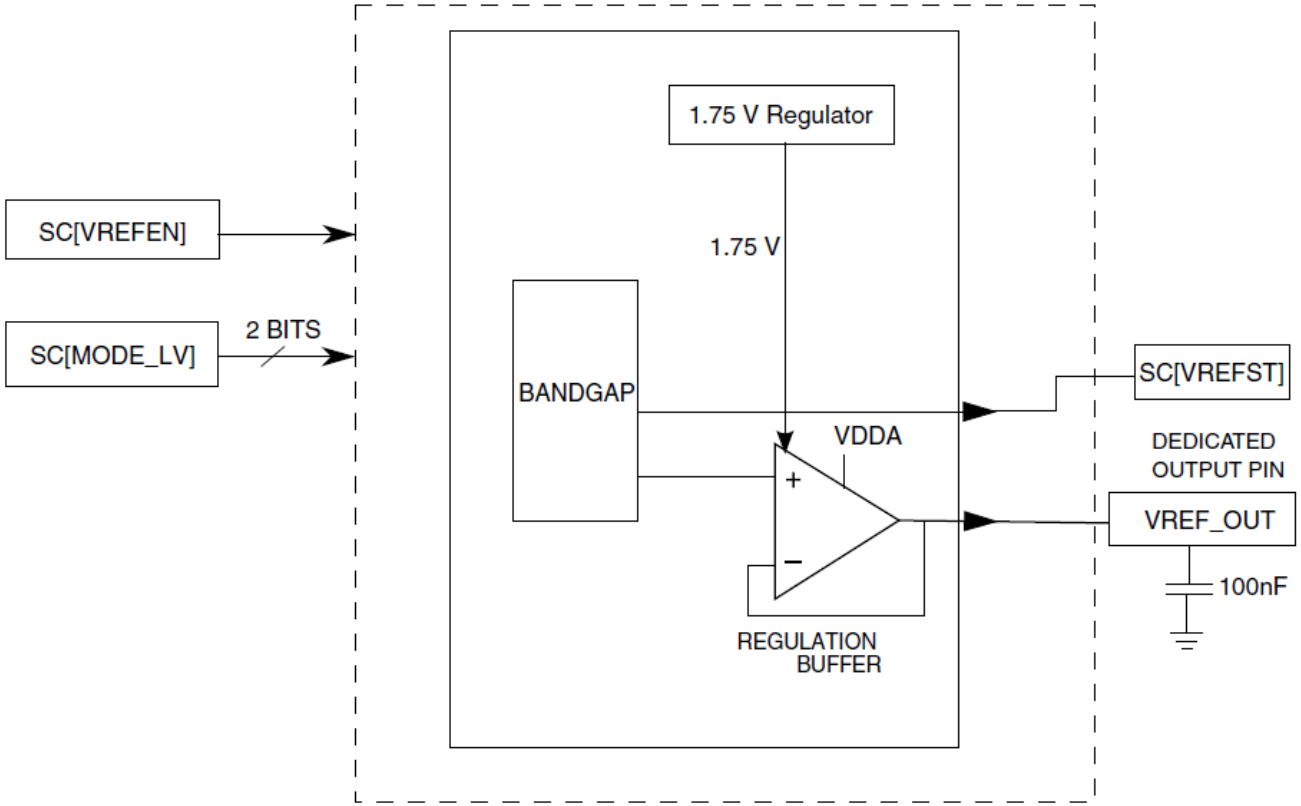


Figure 37-1. Voltage reference block diagram

FESC

USB Voltage Regulator (K20)

- ✓ The USB Voltage Regulator module is a LDO linear voltage regulator to provide 3.3V power from an input power supply varying from 2.7 V to 5.5 V.
- ✓ Low drop-out voltage: 300 mV
- ✓ Output current: 120 mA.
- ✓ Automatic current limiting if the load current is greater than 290 mA
- ✓ Small output capacitor: 2.2 uF
- ✓ Stable with aluminum, tantalum or ceramic capacitors.

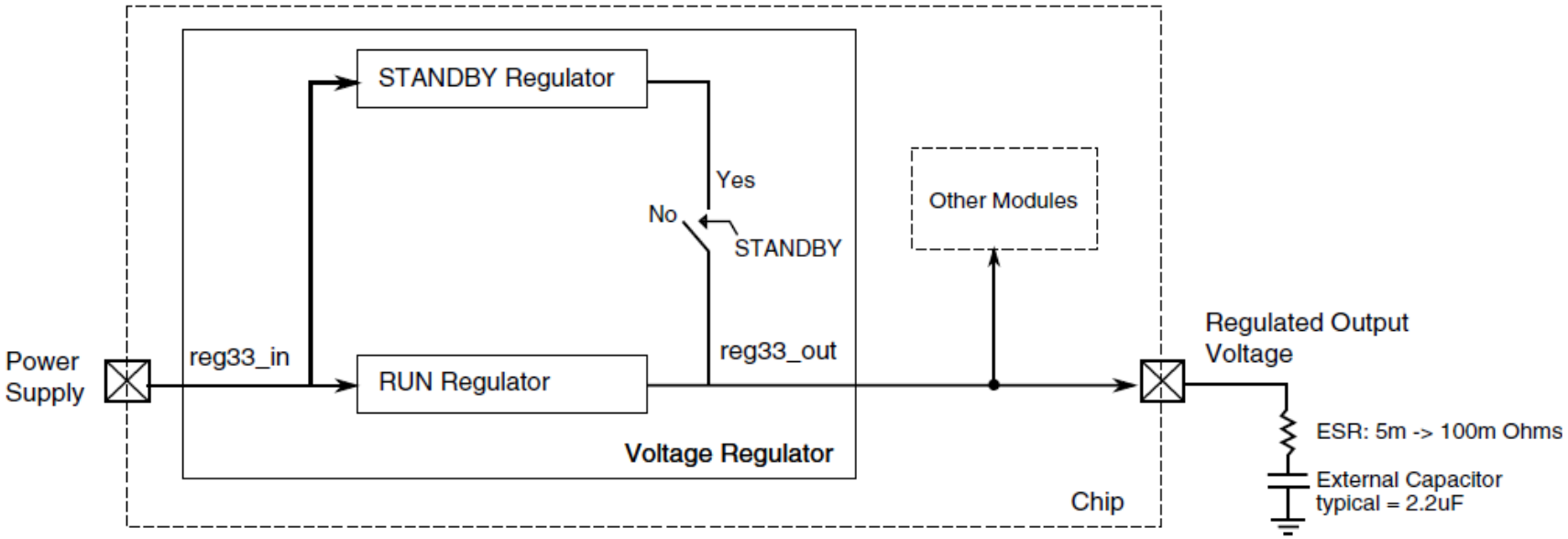


Figure 47-2. USB Voltage Regulator Block Diagram

FESC

10/100Mbps Ethernet MAC IEEE 1588 (K60)

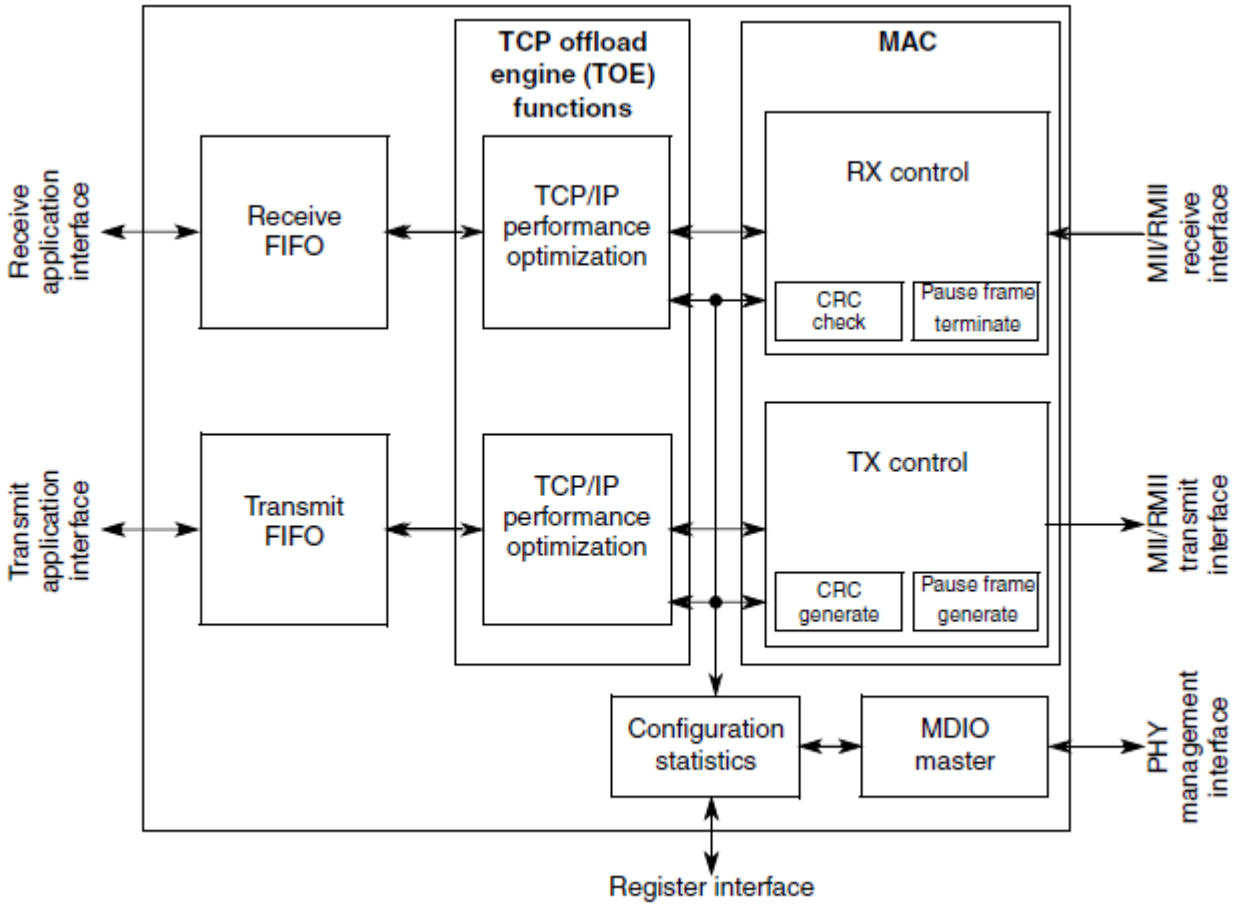


Figure 44-1. 10/100 Ethernet MAC-NET Core Block Diagram

✓ Implements the full 802.3 specification with preamble/SFD
generation, frame padding generation, CRC generation and checking
✓ Dynamically configurable to support 10/100 Mbps operation
✓ Supports 10/100 Mbps full duplex and configurable half duplex operation

✓IPv4 and IPv6 support

✓Support for all IEEE 1588 frames
✓Reference clock can be chosen independently of the network
Speed
✓Software-programmable precise time-stamping of ingress and egress frames
✓ 4 channel IEEE 1588 timer, each with support for input capture and output compare
using the 1588 counter

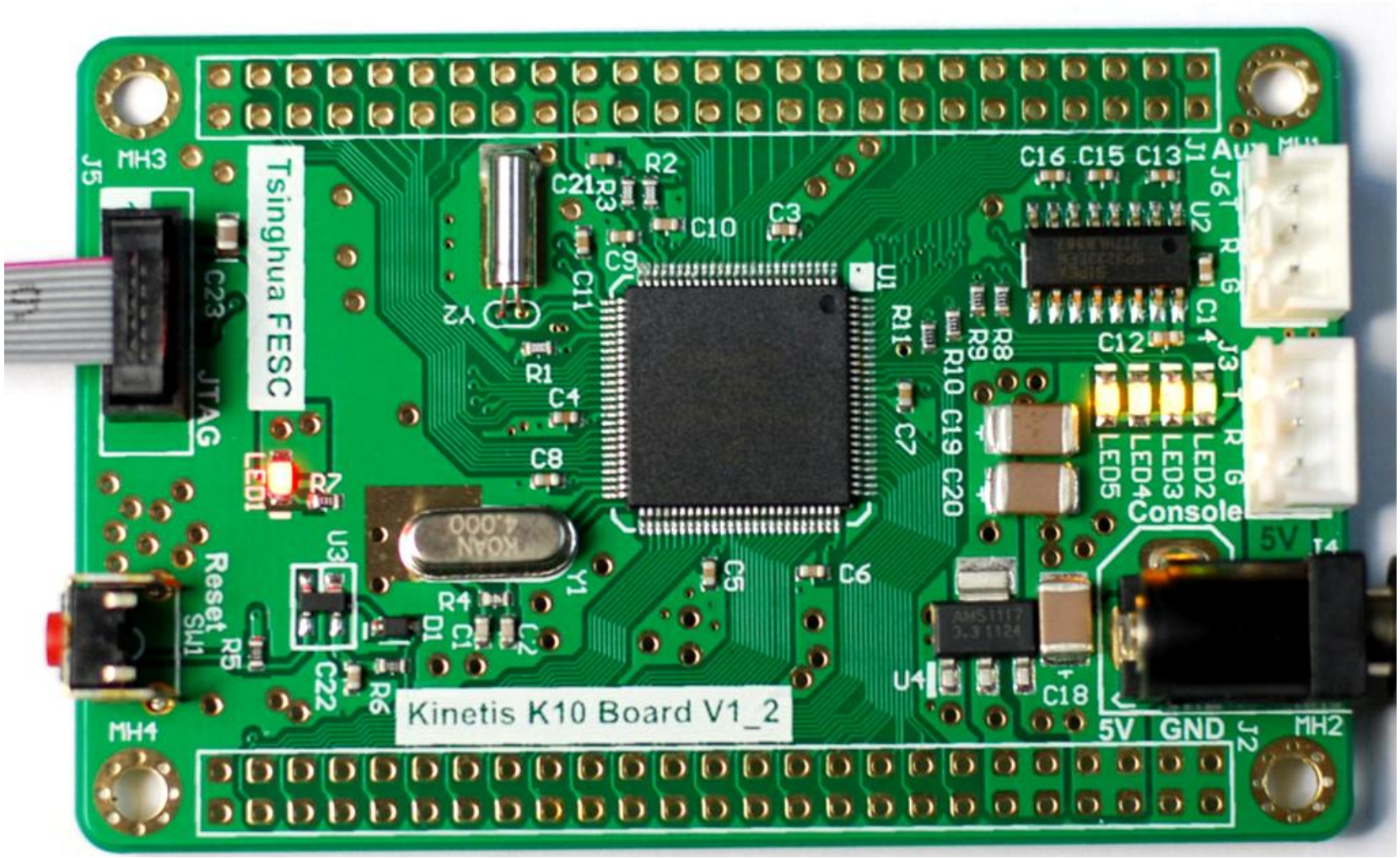
FESC

下届全国大学生Freescale杯车模竞赛（新）

ARM Cortex-4 K10 开发套件

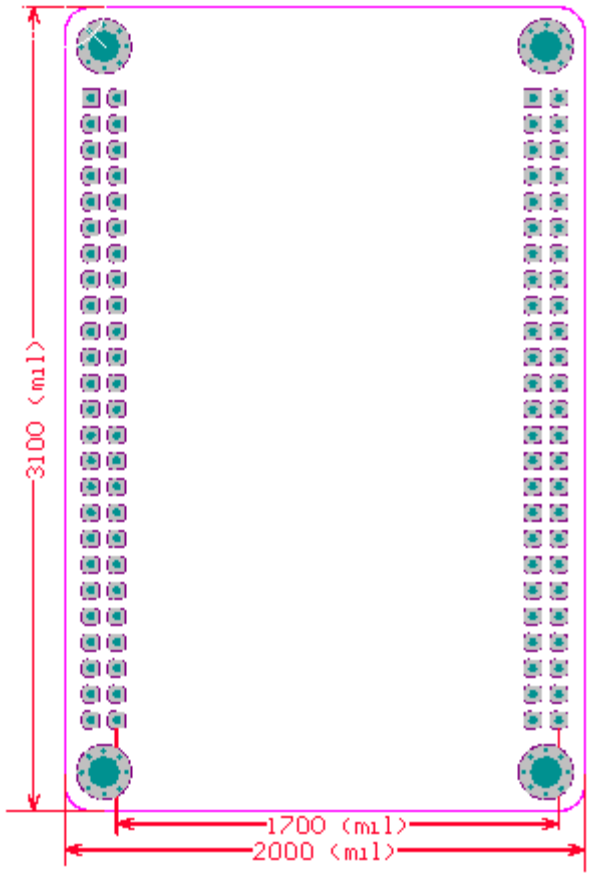
FESC

K10 核心小板



FESC

K10 核心小板机械尺寸



K10N512VLL100开发板J1、J2间的距离是1700mil

FESC

K10 核心小板引脚定义

J1				J2			
1	GND	2	GND	1	GND	2	GND
3	PTD0	4	PTD1	3	GND	4	GND
5	PTD2	6	PTD3	5	5V	6	5V
7	PTD4	8	PTD5	7	5V	8	5V
9	PTD6	10	PTD7	9	3.3V	10	3.3V
11	PTE0	12	PTE1	11	3.3V	12	3.3V
13	PTE2	14	PTE3	13		14	PTC18
15	PTE4	16	PTE5	15	PTC17	16	PTC16
17	PTE6	18		17	PTC15	18	PTC14
19	PTE16	20	PTE17	19	PTC13	20	PTC12
21	PTE18	22	PTE19	21	PTC11	22	PTC10
23	ADC0_DP1	24	ADC0_DM1	23	PTC9	24	PTC8
25	ADC1_DP1	26	ADC1_DM1	25	PTC7	26	PTC6
27	ADC0_DP0	28	ADC0_DM0	27	PTC5	28	PTC4
29	ADC1_DP0	30	ADC1_DM0	29	PTC3	30	PTC2
31	VDDA	32	GND	31	PTC1	32	PTC0
33	VREFH	34	GND	33	PTB23	34	PTB22
35	VREF_OUT	36	DAC0_OUT	35	PTB21	36	PTB20
37	PTE24	38	VBAT	37	PTB19	38	PTB18
39	PTE25	40	PTE26	39	PTB17	40	PTB16
41	PTA4	42	PTA5	41	PTB11	42	PTB10
43	PTA12	44	PTA13	43	PTB9	44	PTB3
45	PTA14	46	PTA15	45	PTB2	46	PTB1
47	PTA16	48	PTA17	47	PTB0	48	RESET
49	GND	50	GND	49	GND	50	GND

FESC

CodeWarrior Development Studio for Microcontrollers v10.1

- **Integrated development tool suite for ColdFire, Kinetis and S08 architectures based on the Eclipse open development platform**
  - Project Wizard creates a new project in as few as 9 clicks
  - MCU Change Wizard retargets a project to a new processor in as few as 6 clicks
  - CodeWarrior optimizing C/C ++ compilers for ColdFire and Kinetis Microcontrollers included
  - Extensions to Eclipse CDT to provide sophisticated features to troubleshoot and repair embedded applications
  - Processor Expert combines easy-to-use component-based application creation with an expert knowledge system
  - Trace and profile support for on-chip trace buffers to provide emulator-like debug capability without additional hardware
  - Kernel-aware debug for MQX, Linux and OSEK
  - CodeWarrior Special Edition is a complimentary version up to 128KB code size

Accelerate the development of the most complex embedded applications

www.freescale.com/codewarrior
to download

freescale semiconductor

IAR Embedded Workbench

- The most widely used tool chain for ARM MCUs
- A consistent tool chain for ColdFire+ and Kinetis devices
- Completely integrated development environment
- Highly optimized IAR C/C++ Compiler
- Powerful IAR C-SPY Debugger
- MQX integration
- Ready-made example projects

More on www.iar.com/freescale

freescale™ semiconductor

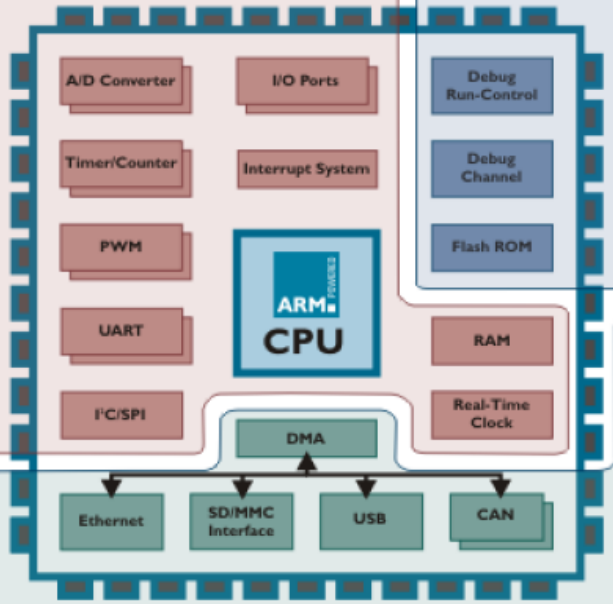
Keil Software Development Tools

Microcontroller Development Kit

CMSIS COMPLIANT

Complete software development environment for Cortex-M and ARM7/9 microcontrollers

Easy to learn and use, yet powerful enough for the most demanding embedded ARM application



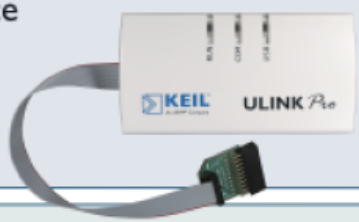
MDK-ARM
Microcontroller Development Kit

- ARM C/C++ Compiler
- Royalty-Free RTX RTOS
- µVision Device Database & IDE
- µVision Debugger & Analysis Tools
- Device Peripheral Simulation

Examples and Templates

ULINK USB Adapters

On-the-fly debugging and Flash programming via JTAG or serial interface



RTX and Real-Time Library

Fully featured real-time kernel

Library of middleware components to speed up software development and solve real-time and communication challenges

RL-ARM
Real-Time Library

- RTX RTOS Source Code
- TCPnet Networking Suite
- Flash File System
- USB Device Interface
- CAN Interface

Examples and Templates

freescale semiconductor

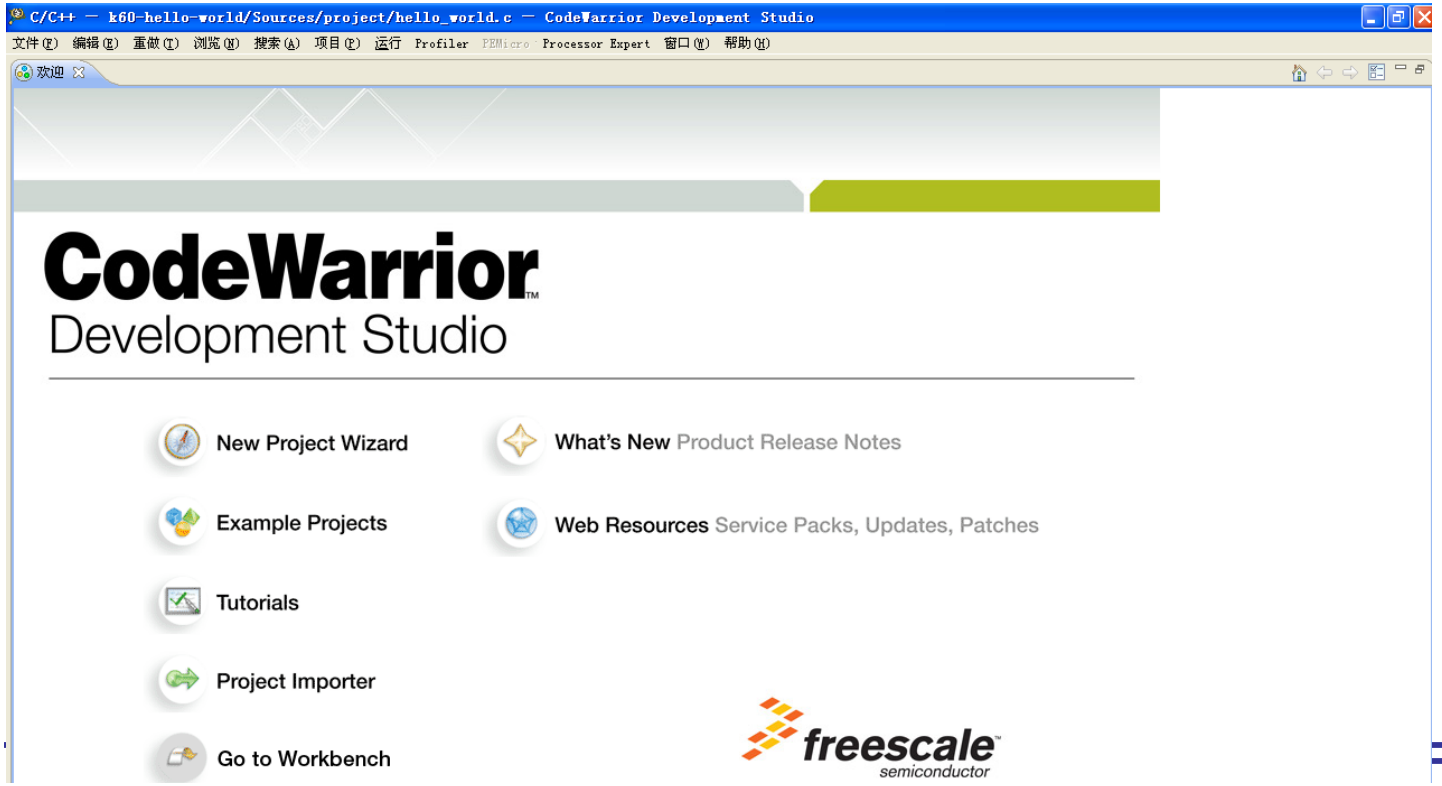
Codewarrior v10.x

What's New?

✓ **New Look!!** --based on the Eclipse open development platform user interface is substantially different from the *classic CodeWarrior IDE*

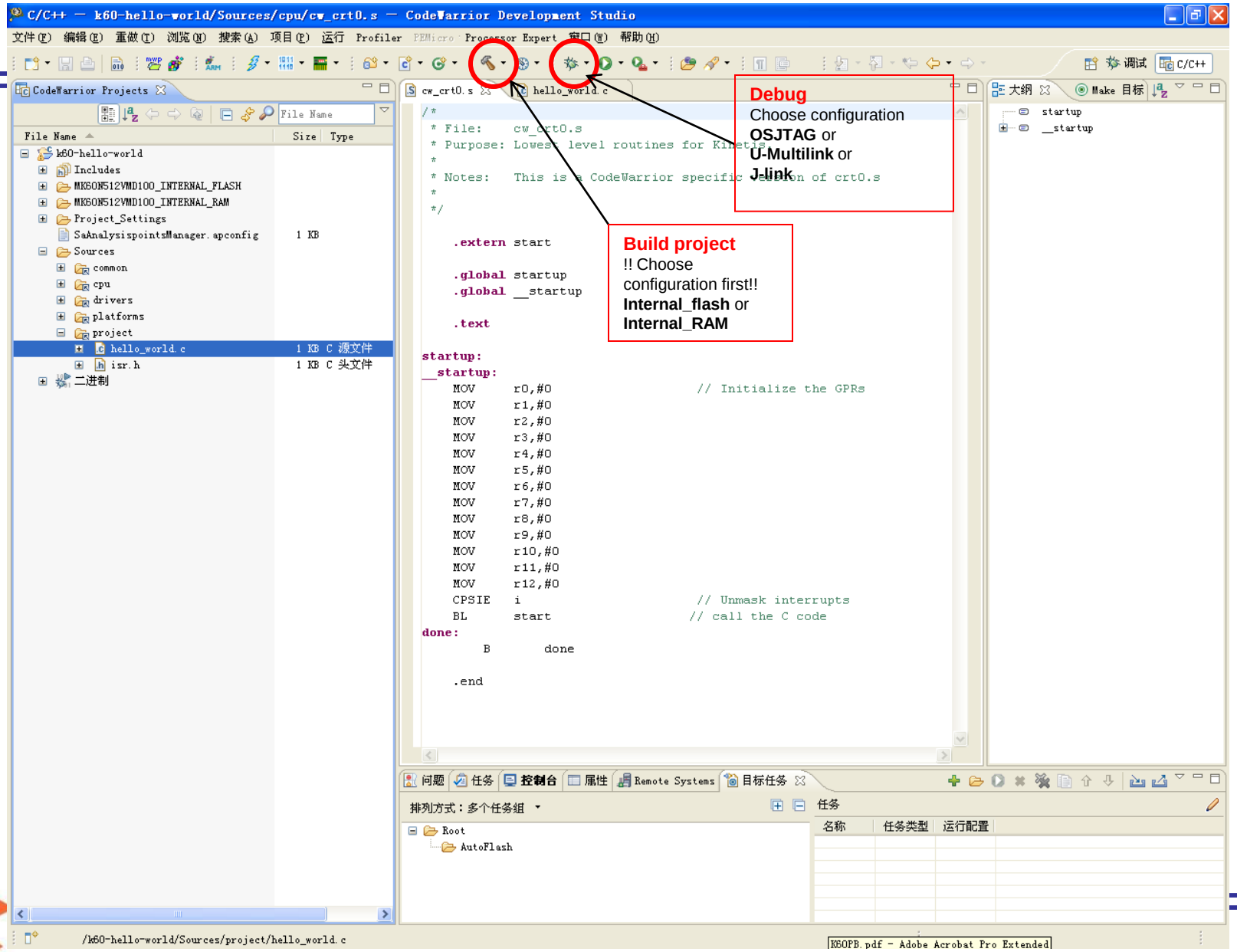
✓**Support** : RS08, HCS08, ColdFire, ColdFire+, Kinetis and MPC56xx

No S12 -_-



FESC

Codewarrior v10.x



Learning Ref.

I. Start with K10 :

- ✓ *K10PB*: **K10 Family Product Brief**
- ✓ *K10P100M100SF2*： mainly about electrical or timing specification
- ✓ *K10P100M100SF2RM:* **datasheet**
- ✓ *K10_KQRUG*: **quick start guide**
- ✓ *KINETIS512_SC*: **demo code**
- ✓ *CW_MCU_v10_1_Examples*: **demo code**

II. Start with Codewarrior v10.x : *CW_MCU_10.1_UM*

FESC