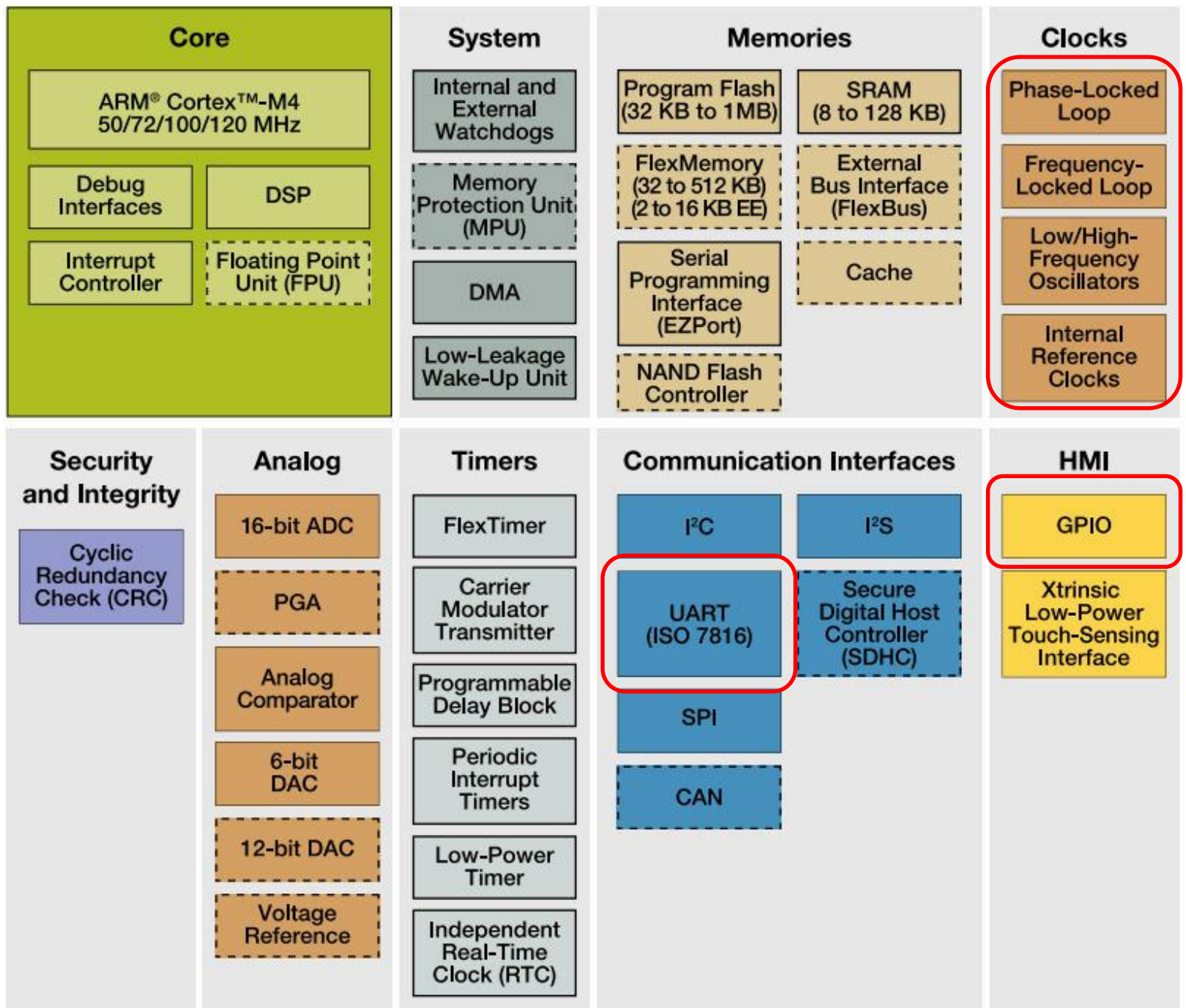


Freescale Kinetis K10 GPIO Step by Step

清华 Freescale 应用开发研究中心 薛涛

2011年12月





Standard Feature Optional Feature

What we used?

Freescale part number	CPU frequency	Pin count	Package	Total flash memory	Program flash	EEPROM	SRAM	GPIO
MK10DN512ZVLL10	100 MHz	100	LQFP	512 KB	512 KB	—	128 KB	70

Reference :

K10P100M100SF2RM.pdf

KQRUG.pdf

K10P100M100SF2.pdf

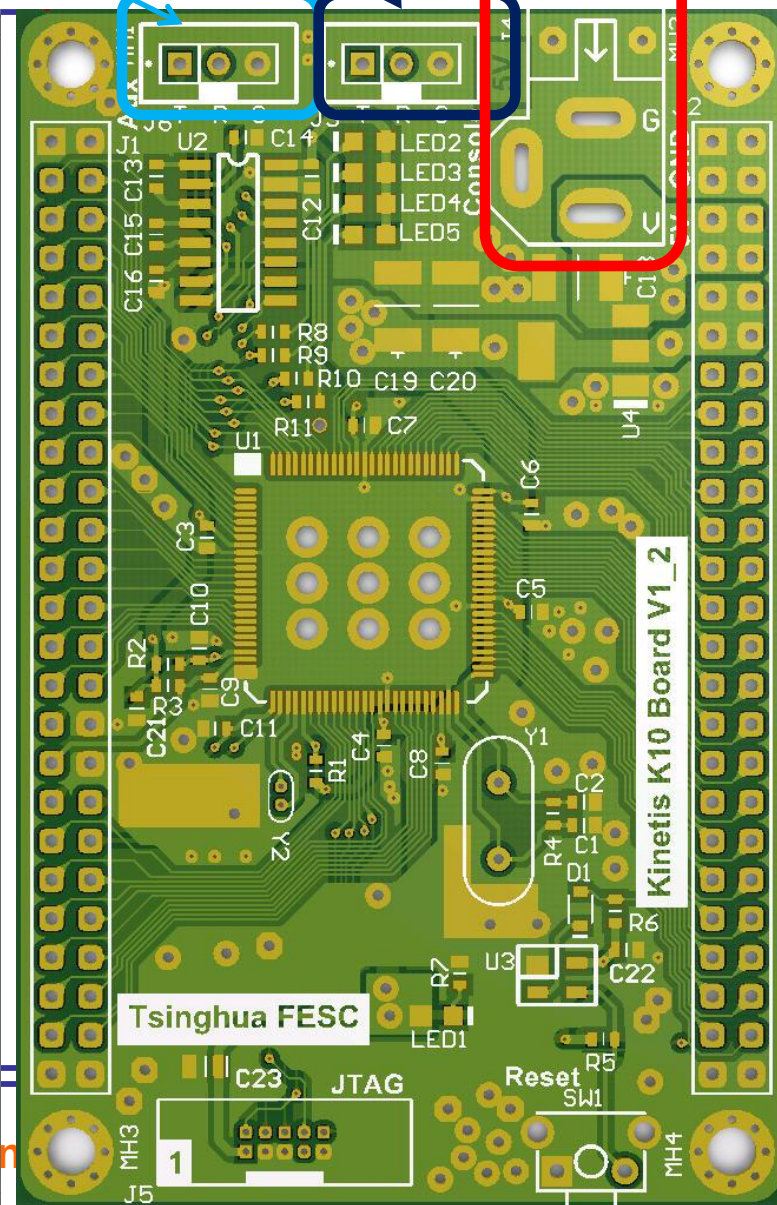
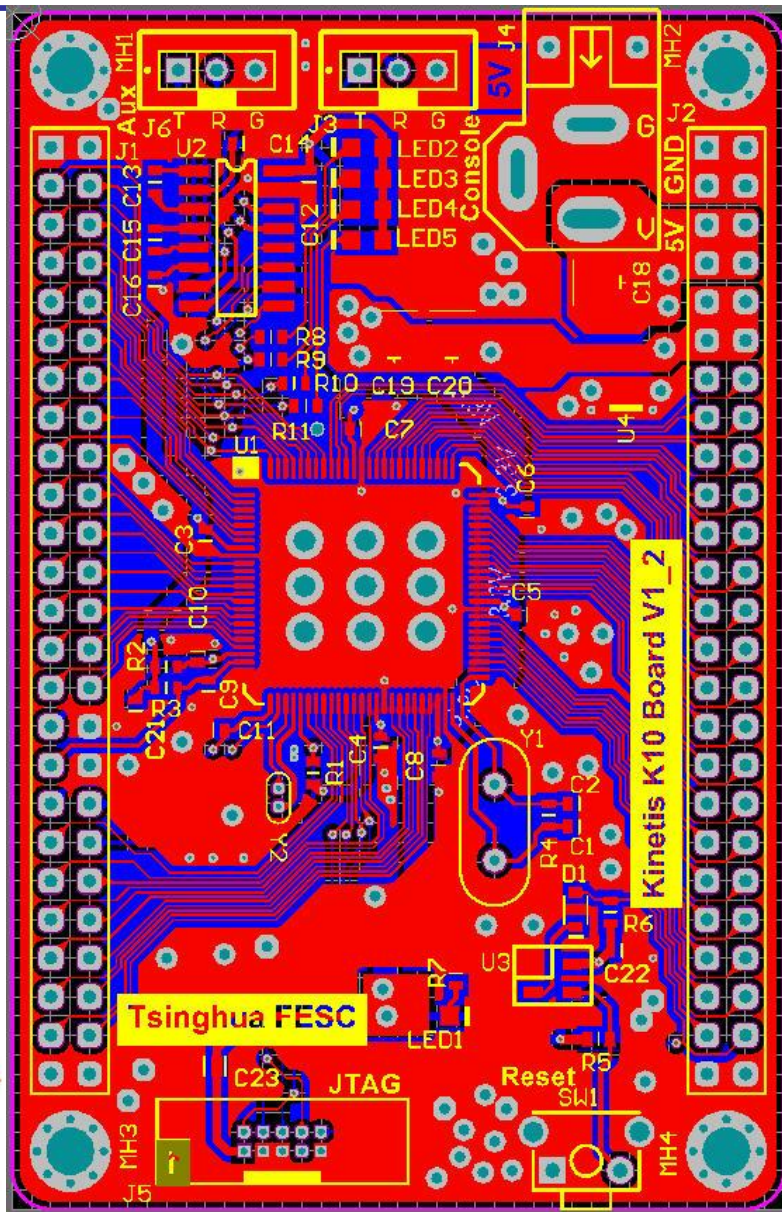


调试用串口UART0

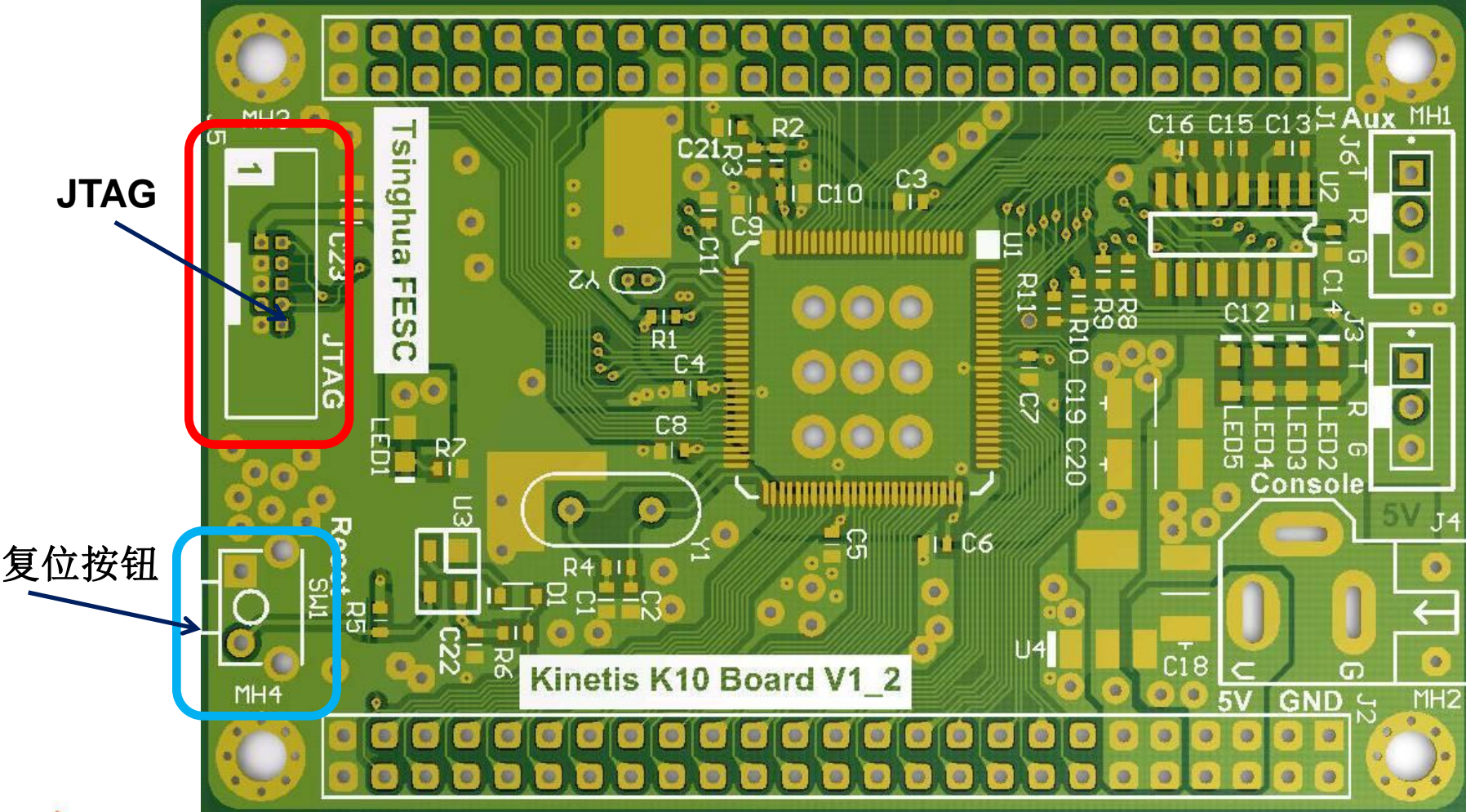
电源 直流5V 100mA

备用串口UART2

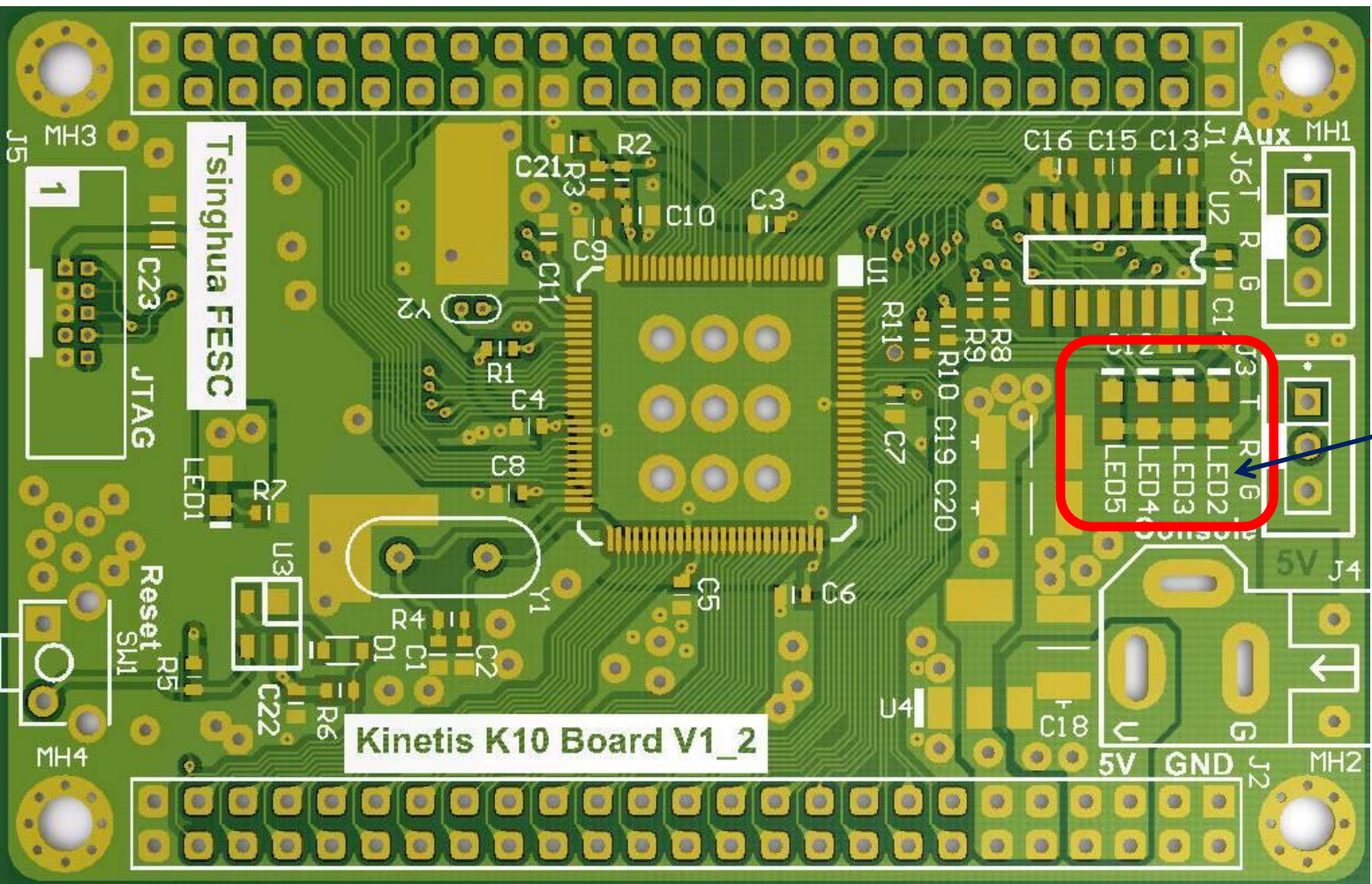
K10 board



K10 board Debug & Reset button



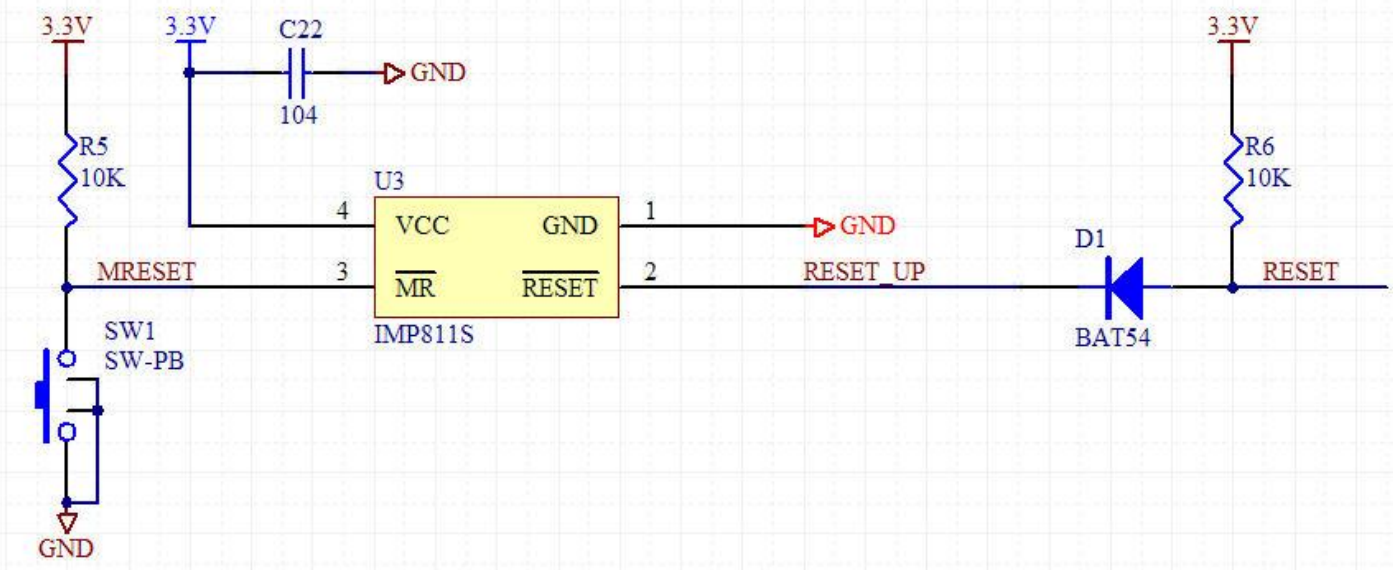
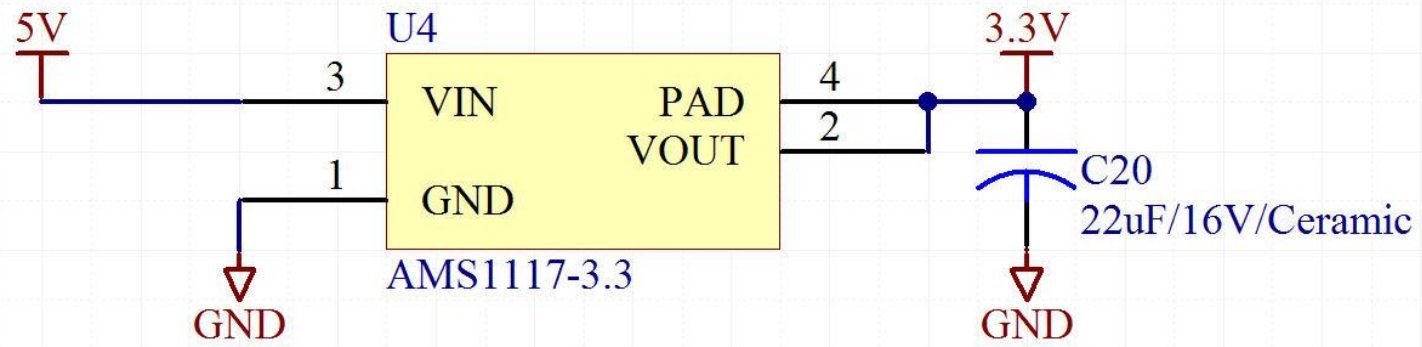
K10 board Leds



LEDs

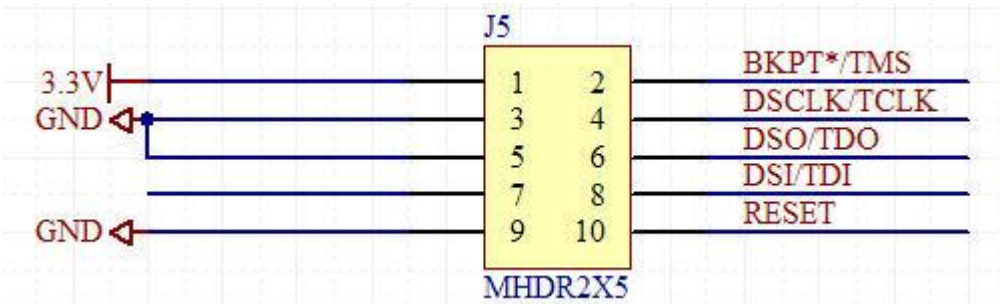
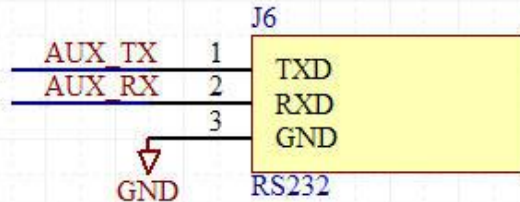
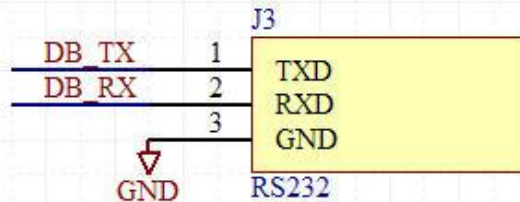
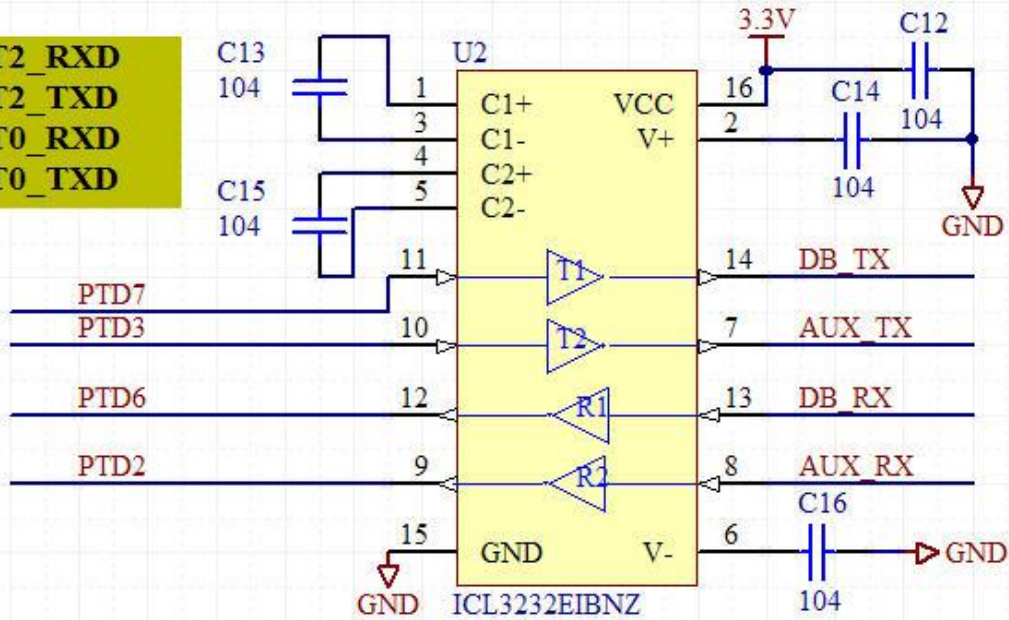


K10 board Power & Reset

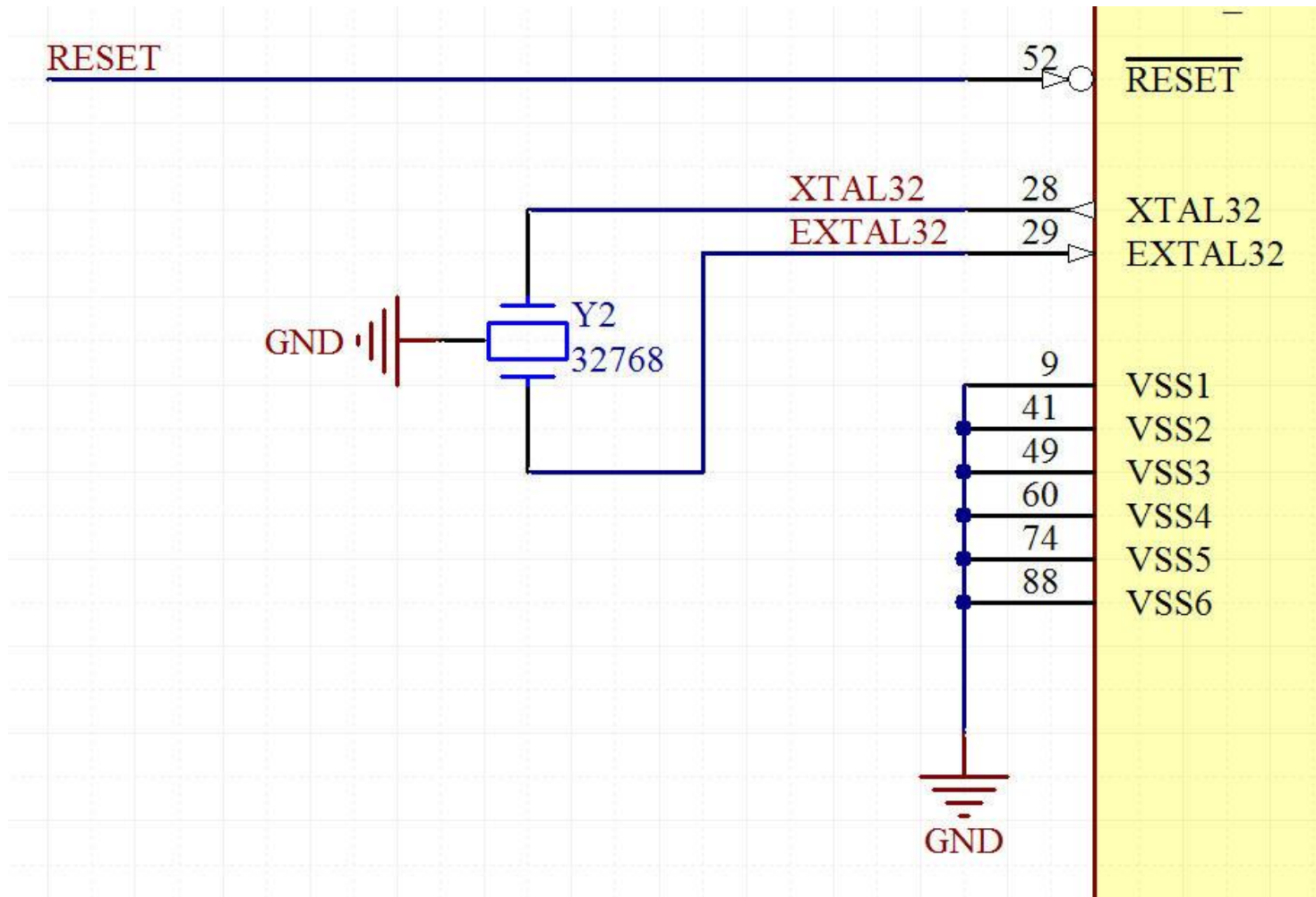


K10 board RS232 & JTAG

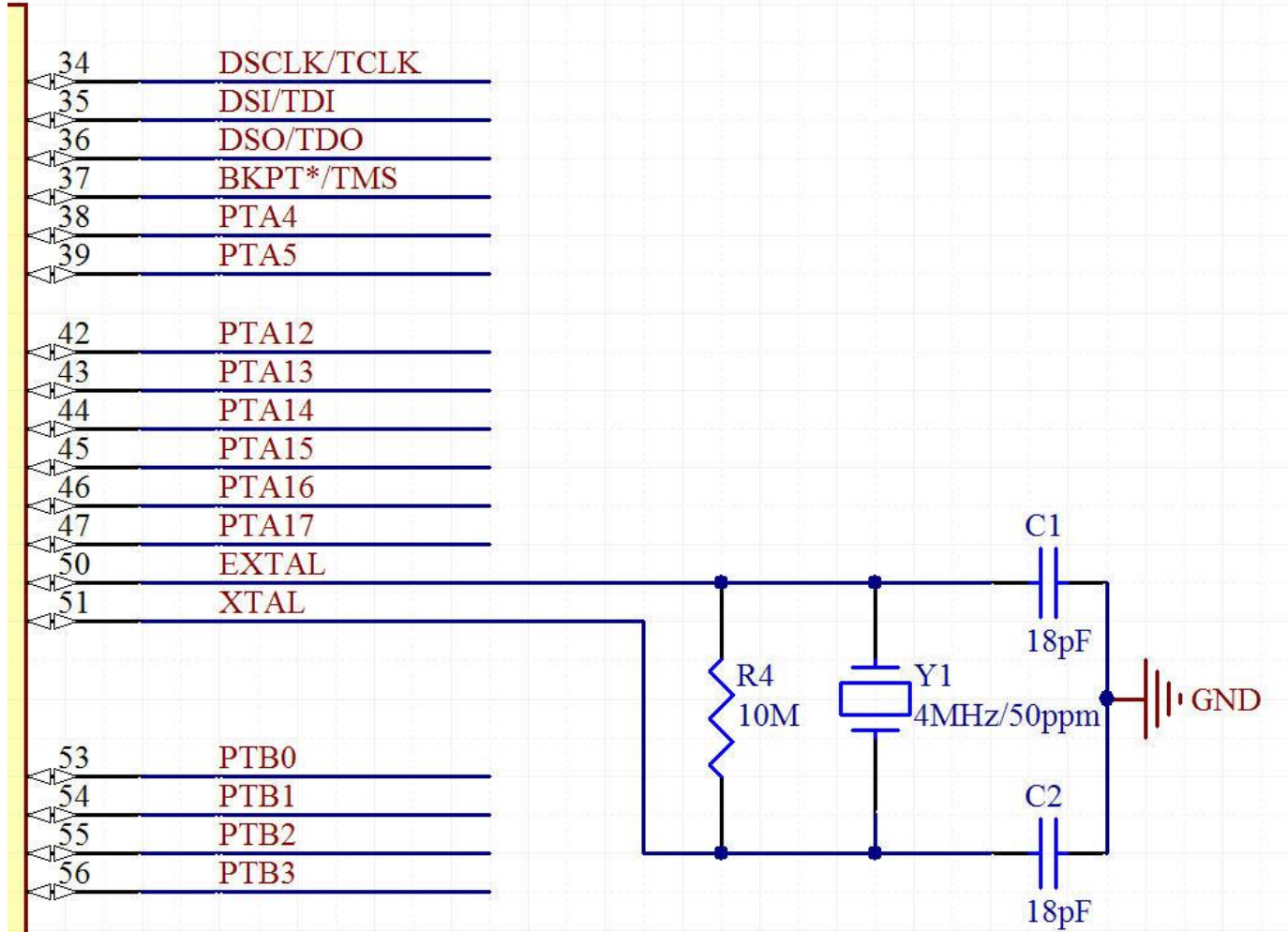
PTD2 as UART2_RXD
 PTD3 as UART2_TXD
 PTD6 as UART0_RXD
 PTD7 as UART0_TXD



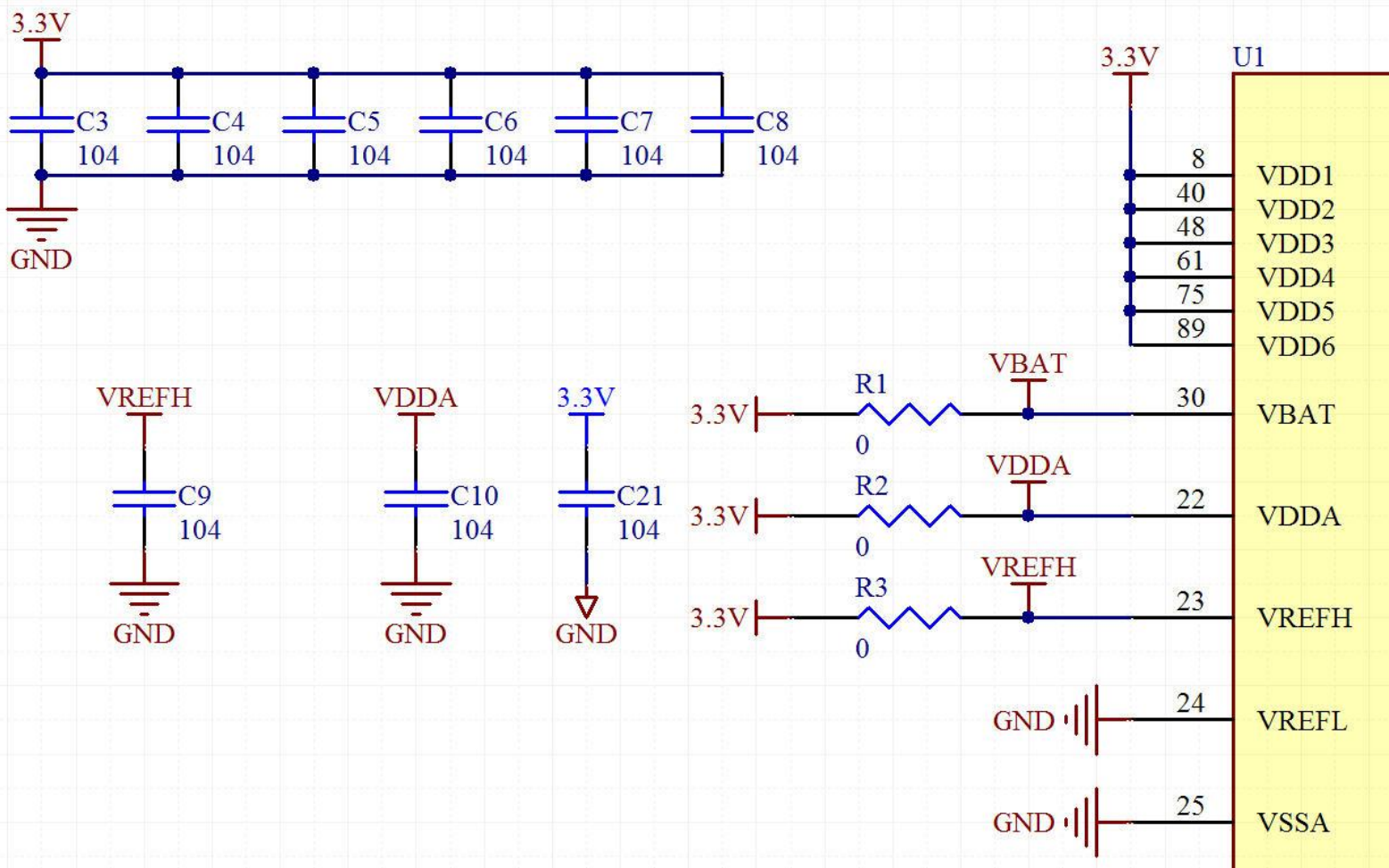
K10 board CLOCK 32768



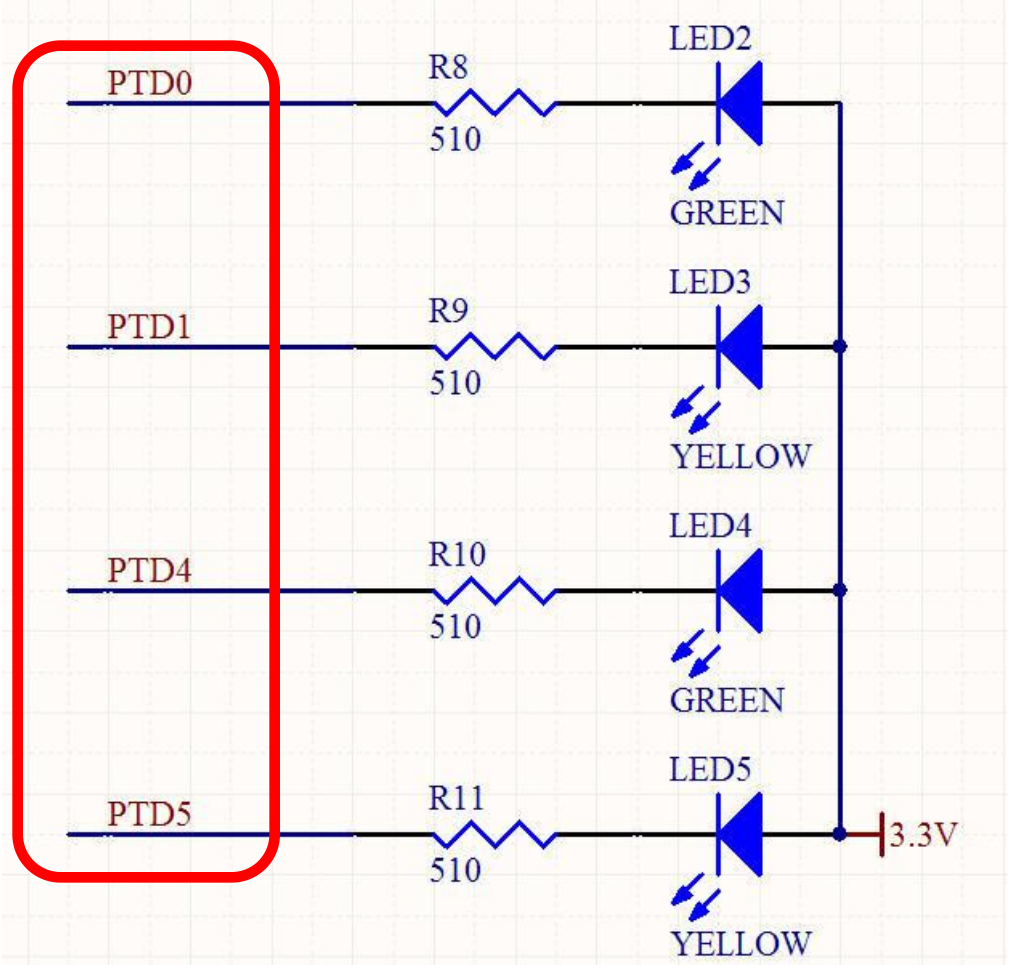
K10 board CLOCK 4MHz



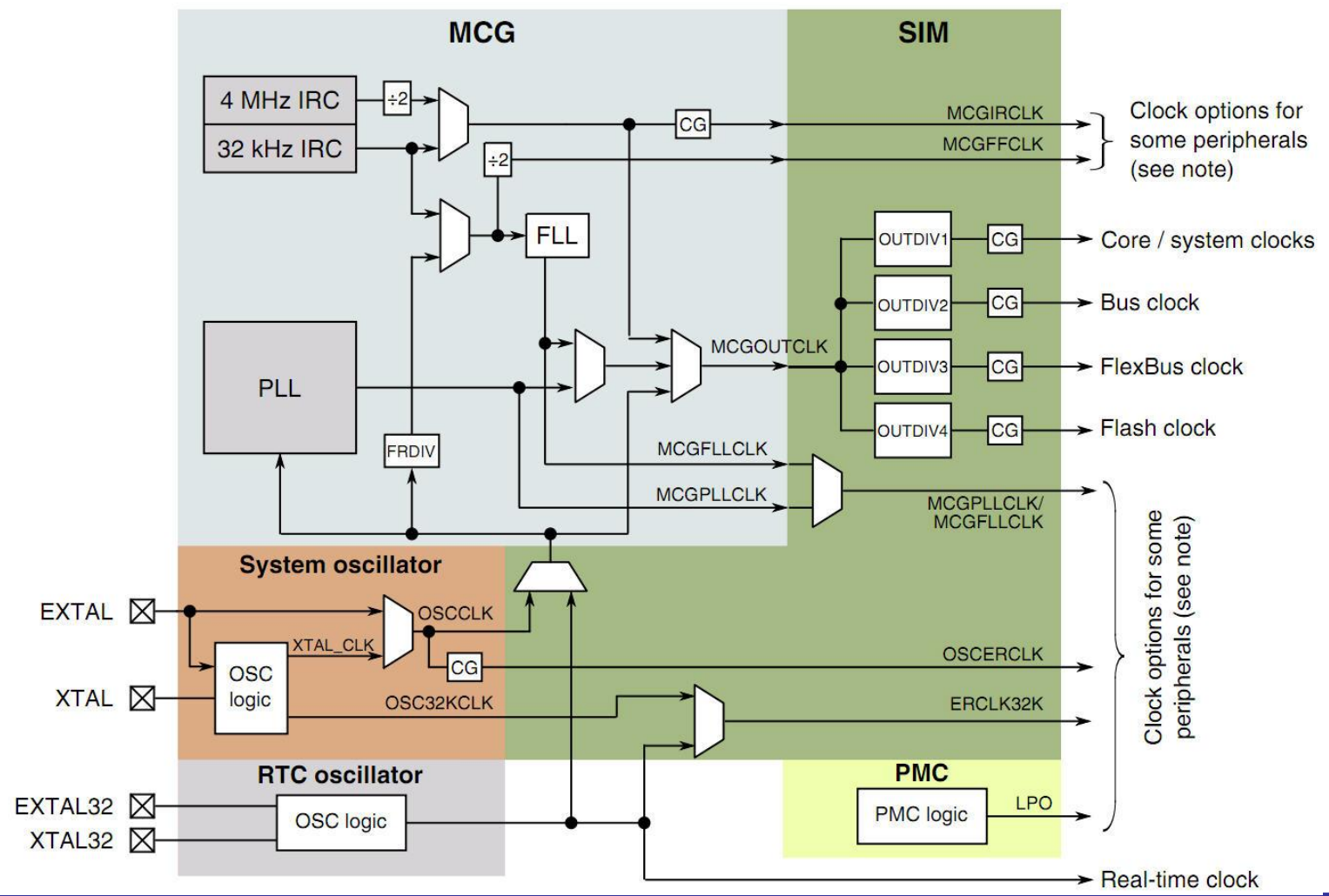
K10 board Power Supply



K10 LEDs



K10 Clock previous



SIM memory map

K10 SIM

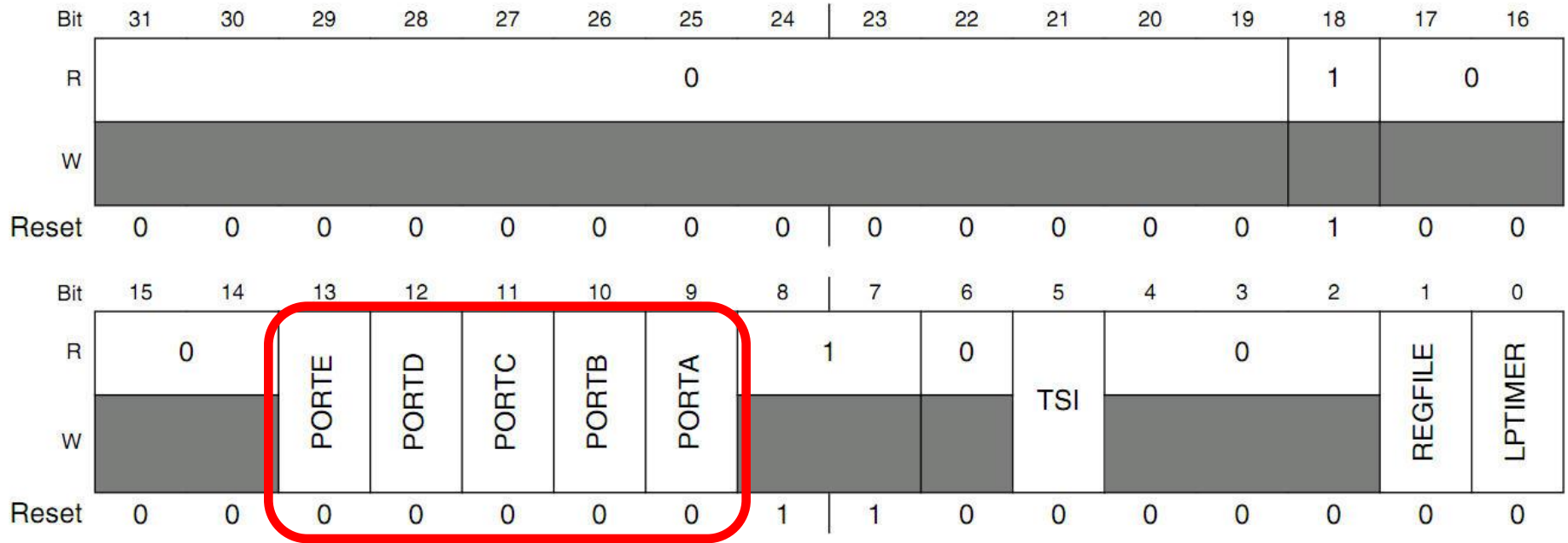
Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4004_7000	System Options Register 1 (SIM_SOPT1)	32	R/W	Undefined	12.2.1/250
4004_8004	System Options Register 2 (SIM_SOPT2)	32	R/W	0000_1000h	12.2.2/252
4004_800C	System Options Register 4 (SIM_SOPT4)	32	R/W	0000_0000h	12.2.3/254
4004_8010	System Options Register 5 (SIM_SOPT5)	32	R/W	0000_0000h	12.2.4/257
4004_8014	System Options Register 6 (SIM_SOPT6)	32	R/W	0000_0000h	12.2.5/258
4004_8018	System Options Register 7 (SIM_SOPT7)	32	R/W	0000_0000h	12.2.6/259
4004_8024	System Device Identification Register (SIM_SDID)	32	R	Undefined	12.2.7/261
4004_8028	System Clock Gating Control Register 1 (SIM_SCGC1)	32	R/W	0000_0000h	12.2.8/262
4004_802C	System Clock Gating Control Register 2 (SIM_SCGC2)	32	R/W	0000_0000h	12.2.9/263
4004_8030	System Clock Gating Control Register 3 (SIM_SCGC3)	32	R/W	0000_0000h	12.2.10/ 264
4004_8034	System Clock Gating Control Register 4 (SIM_SCGC4)	32	R/W	6010_0030h	12.2.11/ 265
4004_8038	System Clock Gating Control Register 5 (SIM_SCGC5)	32	R/W	0004_0180h	12.2.12/ 267
4004_803C	System Clock Gating Control Register 6 (SIM_SCGC6)	32	R/W	4000_0001h	12.2.13/ 269
4004_8040	System Clock Gating Control Register 7 (SIM_SCGC7)	32	R/W	0000_0007h	12.2.14/ 272
4004_8044	System Clock Divider Register 1 (SIM_CLKDIV1)	32	R/W	Undefined	12.2.15/ 273
4004_8048	System Clock Divider Register 2 (SIM_CLKDIV2)	32	R/W	0000_0000h	12.2.16/ 275
4004_804C	Flash Configuration Register 1 (SIM_FCFG1)	32	R	Undefined	12.2.17/ 276
4004_8050	Flash Configuration Register 2 (SIM_FCFG2)	32	R	Undefined	12.2.18/ 277
4004_8054	Unique Identification Register High (SIM_UIDH)	32	R	Undefined	12.2.19/ 278
4004_8058	Unique Identification Register Mid-High (SIM_UIDMH)	32	R	Undefined	12.2.20/ 279
4004_805C	Unique Identification Register Mid Low (SIM_UIDML)	32	R	Undefined	12.2.21/ 279
4004_8060	Unique Identification Register Low (SIM_UIDL)	32	R	Undefined	12.2.22/ 280



K10 SIM

12.2.12 System Clock Gating Control Register 5 (SIM_SCGC5)

Address: SIM_SCGC5 is 4004_7000h base + 1038h offset = 4004_8038h



K10 SIM

13 PORTE	Port E Clock Gate Control This bit controls the clock gate to the Port E module. 0 Clock disabled 1 Clock enabled
12 PORTD	Port D Clock Gate Control This bit controls the clock gate to the Port D module. 0 Clock disabled 1 Clock enabled
11 PORTC	Port C Clock Gate Control This bit controls the clock gate to the Port C module. 0 Clock disabled 1 Clock enabled
10 PORTB	Port B Clock Gate Control This bit controls the clock gate to the Port B module. 0 Clock disabled 1 Clock enabled
9 PORTA	Port A Clock Gate Control This bit controls the clock gate to the Port A module. 0 Clock disabled 1 Clock enabled



K10 GPIO Configure

Control Mode:

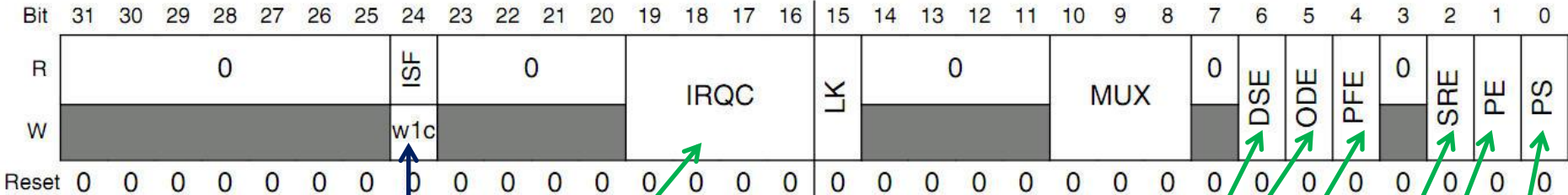
PORTx_PCRn	Pin Control Register
PORTx_GPCLR	Global Pin Control Low Register
PORTx_GPCHR	Global Pin Control High Register
PORTx_ISFR	Interrupt Status Flag Register
PORTx_DFER	Digital Filter Enable Register
PORTx_DFCR	Digital Filter Clock Register
PORTx_DFWR	Digital Filter Width Register



K10 GPIO PCR

Detail in Page 239 of [K10P100M100SF2RM.pdf](#)

Addresses: 4004_9000h base + 0h offset + (4d × n), where n = 0d to 31d



Interrupt Status Flag

Interrupt Configuration

- 0000 Interrupt/DMA Request disabled.
- 0001 DMA Request on rising edge.
- 0010 DMA Request on falling edge.
- 0011 DMA Request on either edge.
- 0100 Reserved.
- 1000 Interrupt when logic zero.
- 1001 Interrupt on rising edge.
- 1010 Interrupt on falling edge.
- 1011 Interrupt on either edge.
- 1100 Interrupt when logic one.

Drive Strength Enable

Open Drain Enable

Passive Filter Enable

Slow Rate Enable

Pull Enable

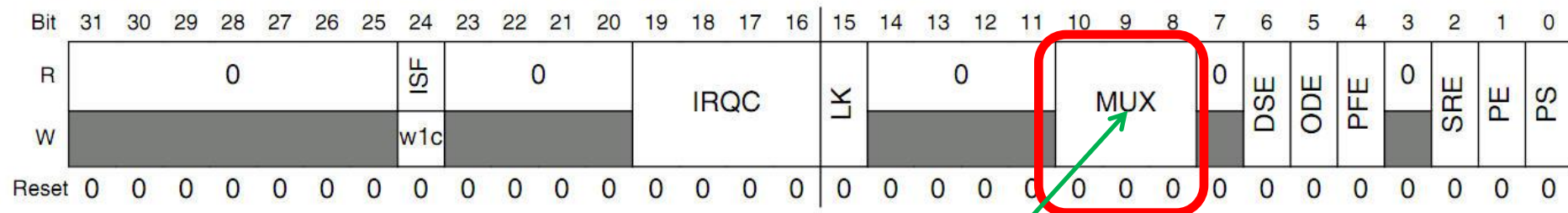
- Pull Select
- Pull Up
- Pull Down



K10 GPIO PCR

Detail in Page 239 of [K10P100M100SF2RM.pdf](#)

Addresses: 4004_9000h base + 0h offset + (4d × n), where n = 0d to 31d



Pin Mux Control

- 000 Pin Disabled (Analog).
- 001 Alternative 1 (GPIO).
- 010 Alternative 2 (chip specific).
- 011 Alternative 3 (chip specific).
- 100 Alternative 4 (chip specific).
- 101 Alternative 5 (chip specific).
- 110 Alternative 6 (chip specific).
- 111 Alternative 7 (chip specific / JTAG / NMI).

K10 Signal Multiplexing and Pin Assignments

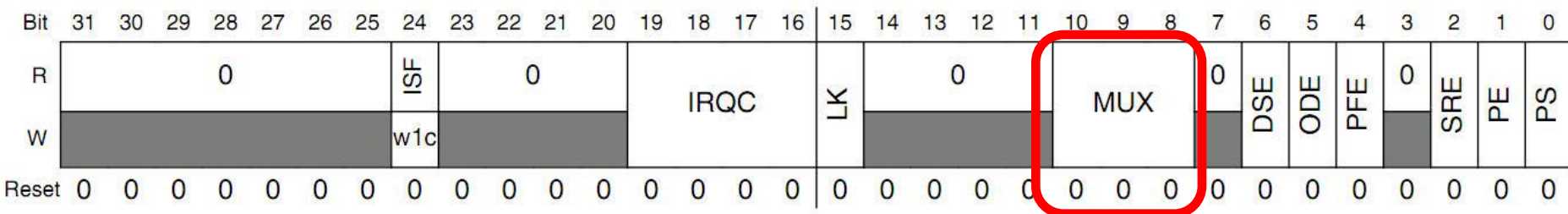
Find in Page 59 of [K10P100M100SF2.pdf](#)



K10 GPIO PCR

Detail in Page 239 of [K10P100M100SF2RM.pdf](#)

Addresses: 4004_9000h base + 0h offset + (4d × n), where n = 0d to 31d



93	PTD0			PTD0	SPI0_PCS0	UART2_RTS_b		FB_ALE/ FB_CS1_b/ FB_TS_b		
94	PTD1	/ADC0_SE5b	/ADC0_SE5b	PTD1	SPI0_SCK	UART2_CTS_b		FB_CS0_b		
95	PTD2			PTD2	SPI0_SOUT	UART2_RX		FB_AD4		
96	PTD3			PTD3	SPI0_SIN	UART2_TX		FB_AD3		
97	PTD4			PTD4	SPI0_PCS1	UART0_RTS_b	FTM0_CH4	FB_AD2	EWM_IN	
98	PTD5	/ADC0_SE6b	/ADC0_SE6b	PTD5	SPI0_PCS2	UART0_CTS_b	FTM0_CH5	FB_AD1	EWM_OUT_b	
99	PTD6	/ADC0_SE7b	/ADC0_SE7b	PTD6	SPI0_PCS3	UART0_RX	FTM0_CH6	FB_AD0	FTM0_FLT0	
100	PTD7			PTD7	CMT_IRO	UART0_TX	FTM0_CH7		FTM0_FLT1	



K10 Signal Multiplexing and Pin Assignments

Find in Page 59 of [K10P100M100SF2.pdf](#)

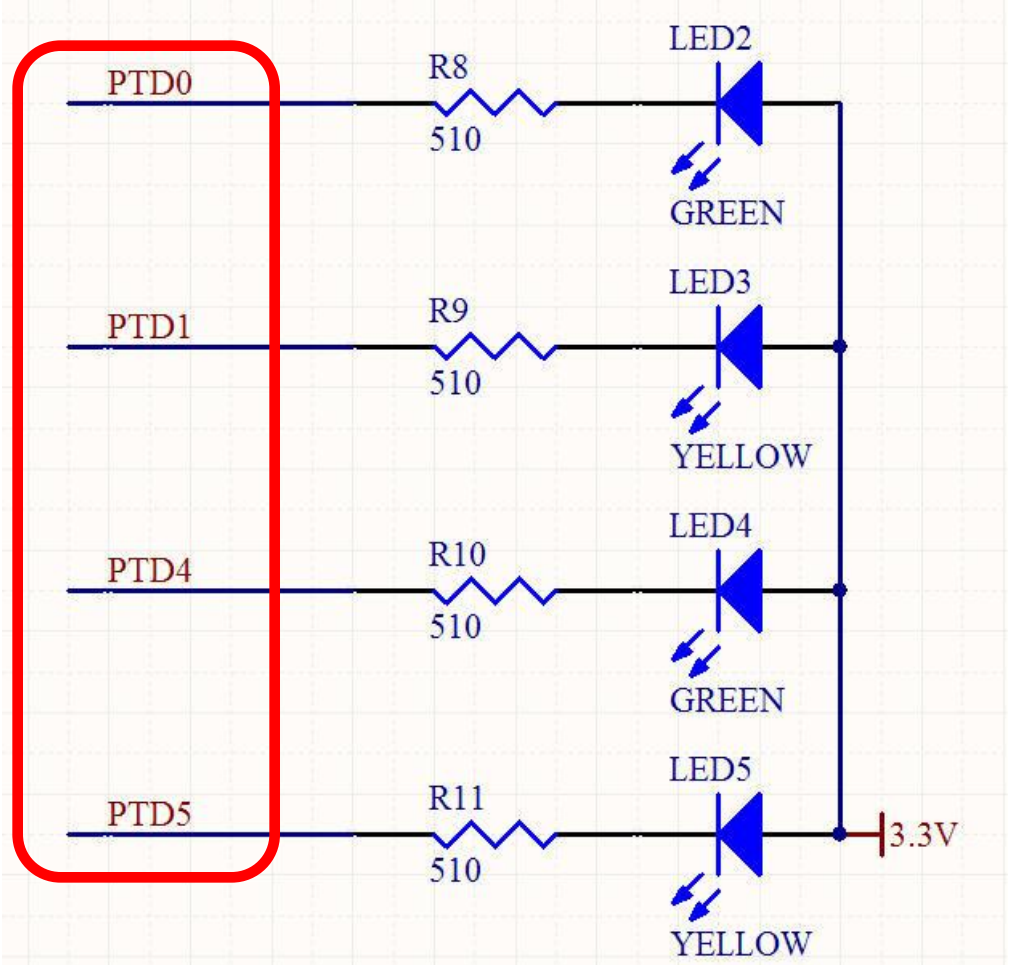


K10 GPIO PCR C Code

```
/* Set pin0,pin1 of PORTD as GPIO */  
PORTD_PCR0=(0|PORT_PCR_MUX(1));  
PORTD_PCR1=(0|PORT_PCR_MUX(1));
```



K10 LEDs



K10 GPIO

Detail in Page 1477 of [K10P100M100SF2RM.pdf](#)

Control Mode:

GPIOx_PDOR

Port Data Output Register

GPIOx_PSOR

Port Set Output Register

GPIOx_PCOR

Port Clear Output Register

GPIOx_PTOR

Port Toggle Output Register

GPIOx_PDIR

Port Data Input Register

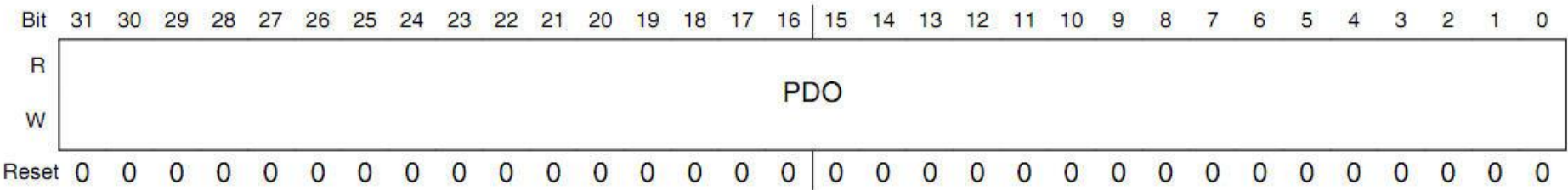
GPIOx_PDDR

Port Data Direction Register



K10 GPIO PDOR

Detail in Page 1482 of [K10P100M100SF2RM.pdf](#)



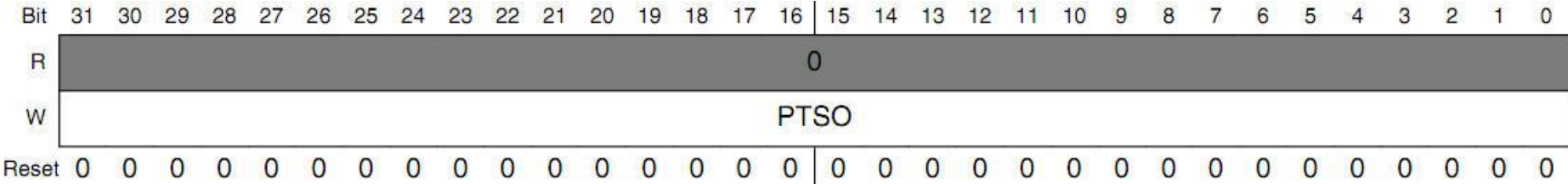
GPIOx_PDOR field descriptions

Field	Description
31–0 PDO	<p>Port Data Output</p> <p>Unimplemented pins for a particular device read as zero.</p> <p>0 Logic level 0 is driven on pin provided pin is configured for General Purpose Output.</p> <p>1 Logic level 1 is driven on pin provided pin is configured for General Purpose Output.</p>



K10 GPIO PSOR

Detail in Page 1482 of [K10P100M100SF2RM.pdf](#)



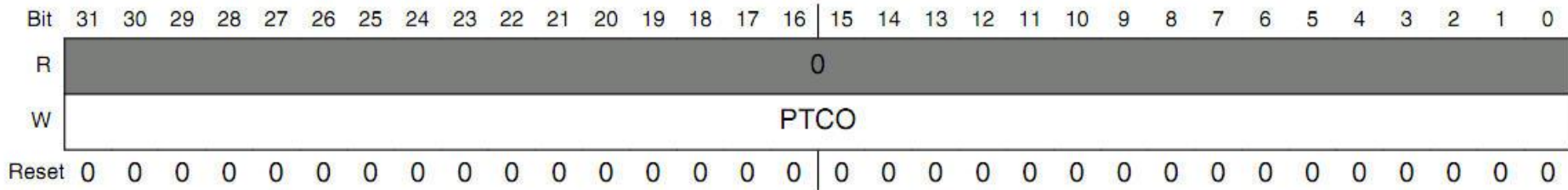
GPIOx_PSOR field descriptions

Field	Description
31–0 PTSO	<p>Port Set Output</p> <p>Writing to this register will update the contents of the corresponding bit in the Port Data Output Register (PDOR) as follows:</p> <p>0 Corresponding bit in PDORn does not change.</p> <p>1 Corresponding bit in PDORn is set to logic one.</p>



K10 GPIO PCOR

Detail in Page 1483 of [K10P100M100SF2RM.pdf](#)



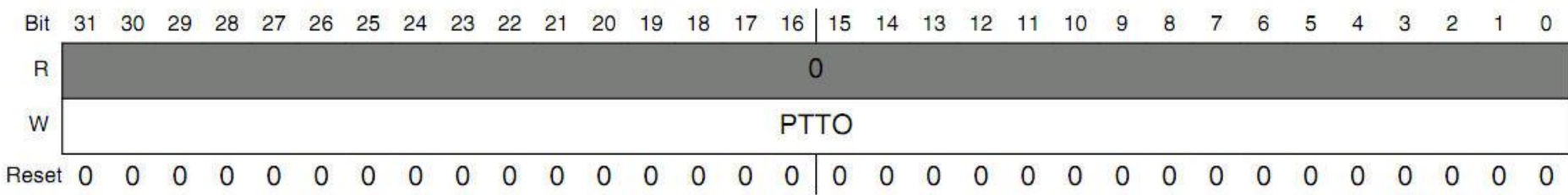
GPIOx_PCOR field descriptions

Field	Description
31-0 PTCO	<p>Port Clear Output</p> <p>Writing to this register will update the contents of the corresponding bit in the Port Data Output Register (PDOR) as follows:</p> <p>0 Corresponding bit in PDORn does not change.</p> <p>1 Corresponding bit in PDORn is set to logic zero.</p>



K10 GPIO PTOR

Detail in Page 1484 of [K10P100M100SF2RM.pdf](#)



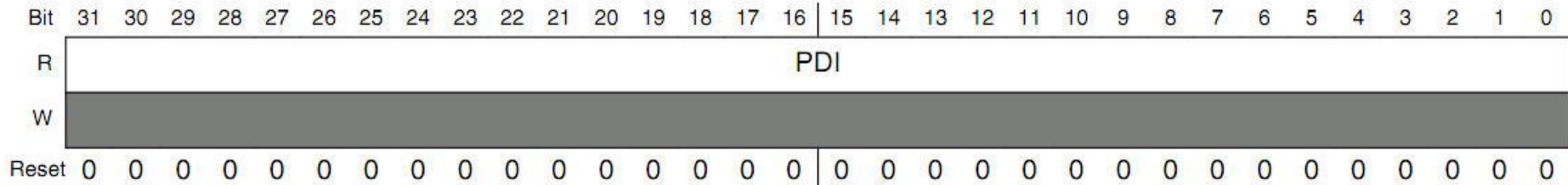
GPIOx_PTOR field descriptions

Field	Description
31-0 PTTO	Port Toggle Output Writing to this register will update the contents of the corresponding bit in the Port Data Output Register (PDOR) as follows:
0	Corresponding bit in PDORn does not change.
1	Corresponding bit in PDORn is set to the inverse of its existing logic state.



K10 GPIO PDIR

Detail in Page 1484 of [K10P100M100SF2RM.pdf](#)



GPIOx_PDIR field descriptions

Field	Description
31-0 PDI	<p>Port Data Input</p> <p>Unimplemented pins for a particular device read as zero. Pins that are not configured for a digital function read as zero. If the corresponding Port Control and Interrupt module is disabled, then that Port Data Input Register does not update.</p> <p>0 Pin logic level is logic zero or is configured for use by digital function.</p> <p>1 Pin logic level is logic one.</p>



K10 GPIO PDDR

Detail in Page 1485 of [K10P100M100SF2RM.pdf](#)

Field	Description
31-0 PDD	Port data direction 0 Pin is configured as general purpose input, if configured for the GPIO function 1 Pin is configured for general purpose output, if configured for the GPIO function



K10 GPIO C Code

```
/* set pin0,pin1 to be output*/
GPIOD_PDDR=GPIO_PDDR_PDD(GPIO_PIN(0)|GPIO_PIN(1));
GPIOD_PDOR &= ~GPIO_PDOR_PDO(GPIO_PIN(1)|GPIO_PIN(0));

#define GPIO_PDDR_PDD(x)
(((uint32_t)(((uint32_t)(x))<<GPIO_PDDR_PDD_SHIFT))&GPIO_PDDR_PDD_MASK)

#define GPIO_PDOR_PDO(x)
(((uint32_t)(((uint32_t)(x))<<GPIO_PDOR_PDO_SHIFT))&GPIO_PDOR_PDO_MASK)

#define GPIO_PDOR_PDO_MASK          0xFFFFFFFFFu
#define GPIO_PDOR_PDO_SHIFT        0

#define GPIO_PIN_MASK                0x1Fu
#define GPIO_PIN(x)                  (((1)<<(x & GPIO_PIN_MASK)))
```



K10 GPIO C Code

```
GPIOD_PDOR |= GPIO_PDOR_PDO(GPIO_PIN(0));  
GPIOD_PDOR &= ~GPIO_PDOR_PDO(GPIO_PIN(0));
```

```
#define GPIO_PDDR_PDD(x)  
(((uint32_t)(((uint32_t)(x))<<GPIO_PDDR_PDD_SHIFT))&GPIO_PDDR_PDD_MASK)
```

```
#define GPIO_PDOR_PDO(x)  
(((uint32_t)(((uint32_t)(x))<<GPIO_PDOR_PDO_SHIFT))&GPIO_PDOR_PDO_MASK)
```

```
#define GPIO_PDOR_PDO_MASK          0xFFFFFFFFFu  
#define GPIO_PDOR_PDO_SHIFT        0
```

```
#define GPIO_PIN_MASK              0x1Fu  
#define GPIO_PIN(x)                (((1)<<(x & GPIO_PIN_MASK)))
```



K10 GPIO C Code

```
//give some delay~~  
void delay()  
{  
    unsigned short i,j;  
    for(i=0;i<3000;i++)  
    {  
        for(j=0;j<100;j++)  
        asm("nop");  
    }  
}
```



K10 LEDs

