

# JTAGjet-Trace

Signum Systems Corp.

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[www.signum.com](http://www.signum.com)

# JTAGjet-Trace Hardware

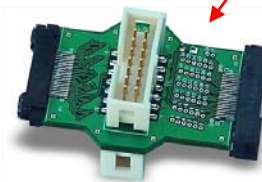
USB 2.0 High-Speed  
connection (480 Mbps)

Up to 4M frames  
deep (18 MBytes)  
ETM trace memory



ETM to JTAG  
adapter optional

38-pin Mictor connector  
contains all ETM and  
JTAG signals



# JTAGjet-Trace Features

- Up to 1.6 GHz CPU speed (200 MHz Trace CLK)
- Non-intrusive, real-time tracing
- Supports all ARM7, ARM9, ARM11 & Cortex ETMs
- Up to 18MB trace memory (4M x 36bits wide)
- 56-bit cycle accurate time stamp
- Traces all or in-range of PC addresses
- Trace on / off from specific PC address
- Traces all or range of data variables (bandwidth allowed)
- Traces data variable values
- Powerful trace post-filtering & timing display
- Compatible with all major C/C++ compilers/debuggers

# Compatible ARM Debuggers

- Chameleon (Signum Systems) is included
- uVision (Keil-ARM)
- Code Composer Studio (Texas Instruments)
- RealView & ADS (ARM Ltd.)
- eBinder (eSol)
- Multi-2000 (Green Hills Software)
- GDB & Insight (GNU / Eclipse)
- EWARM (IAR)
- XRAY & EDGE (Mentor Graphics)
- Code Warrior (MetroWerks)
- CodeSourcery

# Trace Display -Overview

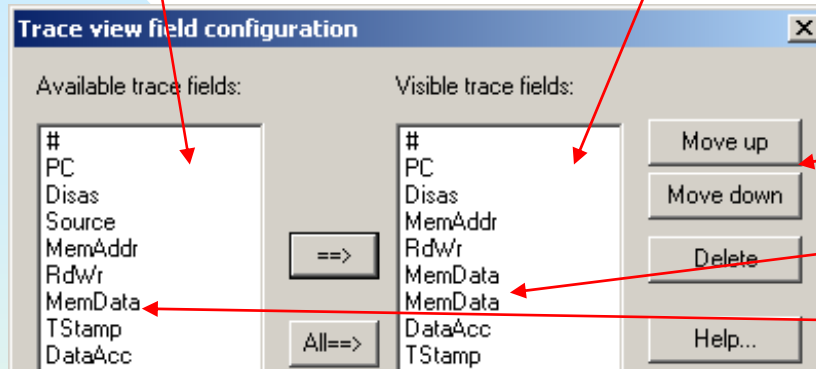
Arm:trace										
Control... Start Resume Clear < Query > <input checked="" type="checkbox"/> Query... <input type="checkbox"/> Filter... Fields... Save...										
#	PC	PC	Disas	Source	MemAddr	R...	DataAcc	MemData	TStamp	
#3223	processing+0x20	2000006C	STRB	R1,[R0,#0]	Buf1[12]	Wr	Byte	60	-132	
#3224	processing+0x24	20000070	ADD	R0,R0,#0x1					-130	
#3225	processing+0x28	20000074	B	processing ... )					-128	
#3230	processing	2000004C	LDRSB	R1,[R0,#0] (	Buf1[13]	Rd	Byte	53	-104	
#3231	processing+0x4	20000050	CMP	R1,#0					-102	
#3232	processing+0x8	20000054	BEQ	0x20000078					-100	
#3235	processing+0xC	20000058	LDRSB	R1,[R0,#0] if (*text != ' ') (	Buf1[13]	Rd	Byte	53	-80	
#3236	processing+0x10	2000005C	CMP	R1,#0x20					-78	
#3237	processing+0x14	20000060	BEQ	0x20000070					-76	
#3240	processing+0x18	20000064	LDRB	R1,[R0,#0] *text ^= 0x20; ...	Buf1[13]	Rd	Byte	53	-56	
#3241	processing+0x1C	20000068	EOR	R1,R1,#0x20					-54	
#3242	processing+0x20	2000006C	STRB	R1,[R0,#0]	Buf1[13]	Wr	Byte	73	-44	
#3243	processing+0x24	20000070	ADD	R0,R0,#0x1					-42	
#3244	processing+0x28	20000074	B	processing ... )					-40	
#3249	processing	2000004C	LDRSB	R1,[R0,#0] (	Buf1[14]	Rd	Byte	00	-16	
#3250	processing+0x4	20000050	CMP	R1,#0					-14	
#3251	processing+0x8	20000054	BEQ	0x20000078					-12	
#3254	processing+0x2C	20000078	MOV	PC,LR					-6	
#3257	main+0x80	200000FC	B	0x200000e4					0	
#3260	main+0x68	200000E4	ADD	R4,R4,#0x1					6	
#3261	main+0x6C	200000E8	B	0x200000d0					8	
#3265	main+0x54	200000D0	LDR	R0,[PC,#0x90]	20000168	Rd	Word	20002000	30	
#3271	main+0x58	200000D4	LDR	R0,[R0,#0x1c]	delay loop	Rd	Word	00000064	50	
#3272	main+0x5C	200000D8	CMP	R4,R0					52	
#3273	main+0x60	200000DC	BLT	0x200000ec					54	
#3276	main+0x70	200000EC	MOV	R0,#0x1 delay(1); ...					60	
#3277	main+0x74	200000F0	BL	delay ...					62	
#3282	delay	20000194	STMFD	SP!,(R4,LR) (	20003FEC	Wr	Word	00000002	80	
#3286	delay	20000194	STMFD	SP!,(R4,LR) (	20003FF0	Wr	Word	200000F4	88	
#3290	delay+0x4	20000198	MOV	R3,R0					96	
#3291	delay+0x8	2000019C	MOV	R2,#0 k = 0;					98	
#3292	delay+0xC	200001A0	MOV	R4,#0 for (i = 0; i < cnt; i++) (					100	
#3293	delay+0x10	200001A4	CMP	R4,R3					102	
#3294	delay+0x14	200001A8	BLT	0x200001b8					104	
#3295	delay+0x24	200001B8	MOV	R12,#0 for (j = 0; j < delaycnt;...					120	
#3296	delay+0x28	200001BC	LDR	R0,[PC,#-0x34]	20000190	Rd	Word	20002020	122	
#3302	delay+0x2C	200001C0	LDR	R0,[R0,#0]	delaycnt	Rd	Word	00000005	142	
#3303	delay+0x30	200001C4	CMP	R12,R0					144	
#3304	delay+0x34	200001C8	BLT	0x200001d8					146	
#3307	delay+0x44	200001D8	MOV	R0,R12 k = k + delay1(j); ...					152	
#3308	delay+0x48	200001DC	BL	delay1 ...					154	
#3311	delay	20000174	MOV	R1,R0					160	
#3313	delay1+0x4	20000178	LDR	R0,[PC,#0x10] delaytemp = v;	20000190	Rd	Word	20002020	178	
#3318	delay1+0x8	2000017C	STR	R1,[R0,#0x4]	delaytemp	Wr	Word	00000000	188	
#3319	delay1+0xC	20000180	MOV	R0,R1 return v;					190	
Status: NotActive,Full Trace Full (100%) Trace Clock: 132.01MHz										

# Trace - Field Selection and Format

Available fields

Visible fields

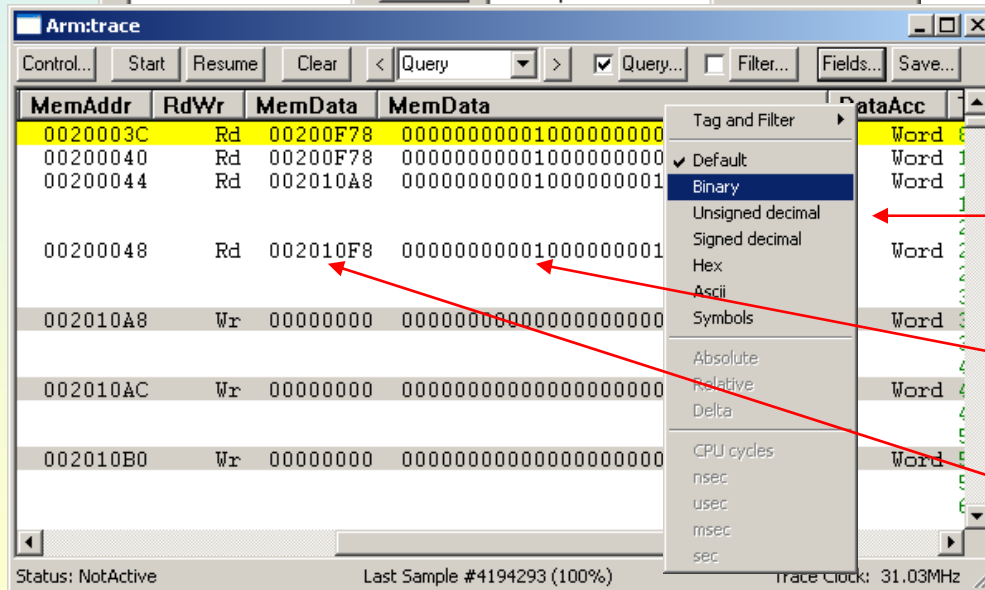
Fields visible in the trace window can be customized by user.



Order of fields can be defined

MemData field used twice

Fields available to display



Display format of each field may be customized too.

Field format selection - click on column header

Field in binary format (useful when displaying bit-register values)

Field in hex format (default)

# Trace - Controls



Saving

Start/Stop

Clear buffer

Search&Tag

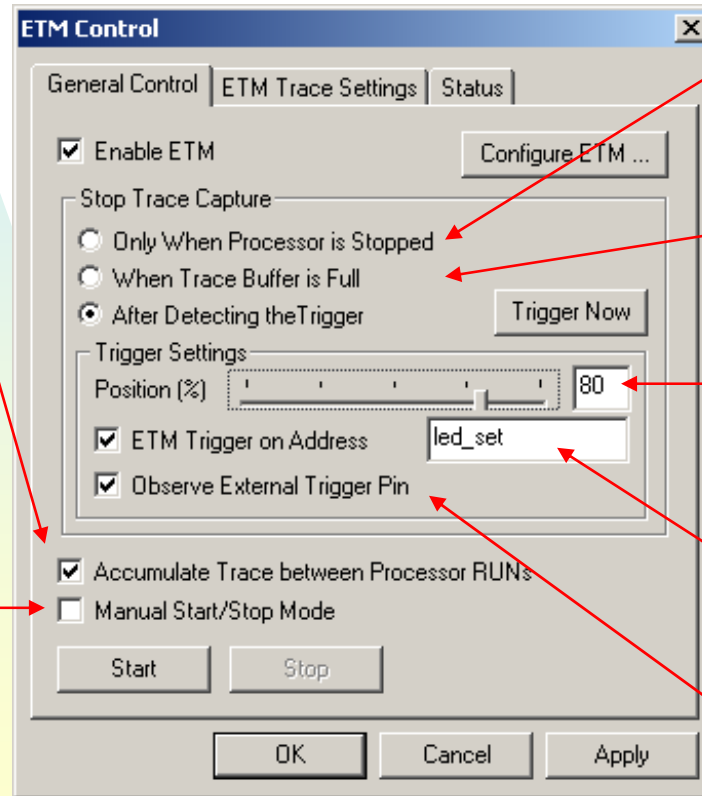
Post-filtering

Fields

Resume (start without clear).

Do not clear buffer before each CPU GO. Useful in source-level stepping.

Do not start trace when CPU starts. Start must be used manually. Useful for reset sequence tracing.



Capture will only stop if CPU stops.

Capture will stop when trace buffer is full - CPU will continue to run.

80% of buffer will have trace before trigger, 20% will have trace after it.

ETM trigger will happen on led\_set function.

Observe the trigger pin on ETM connector.

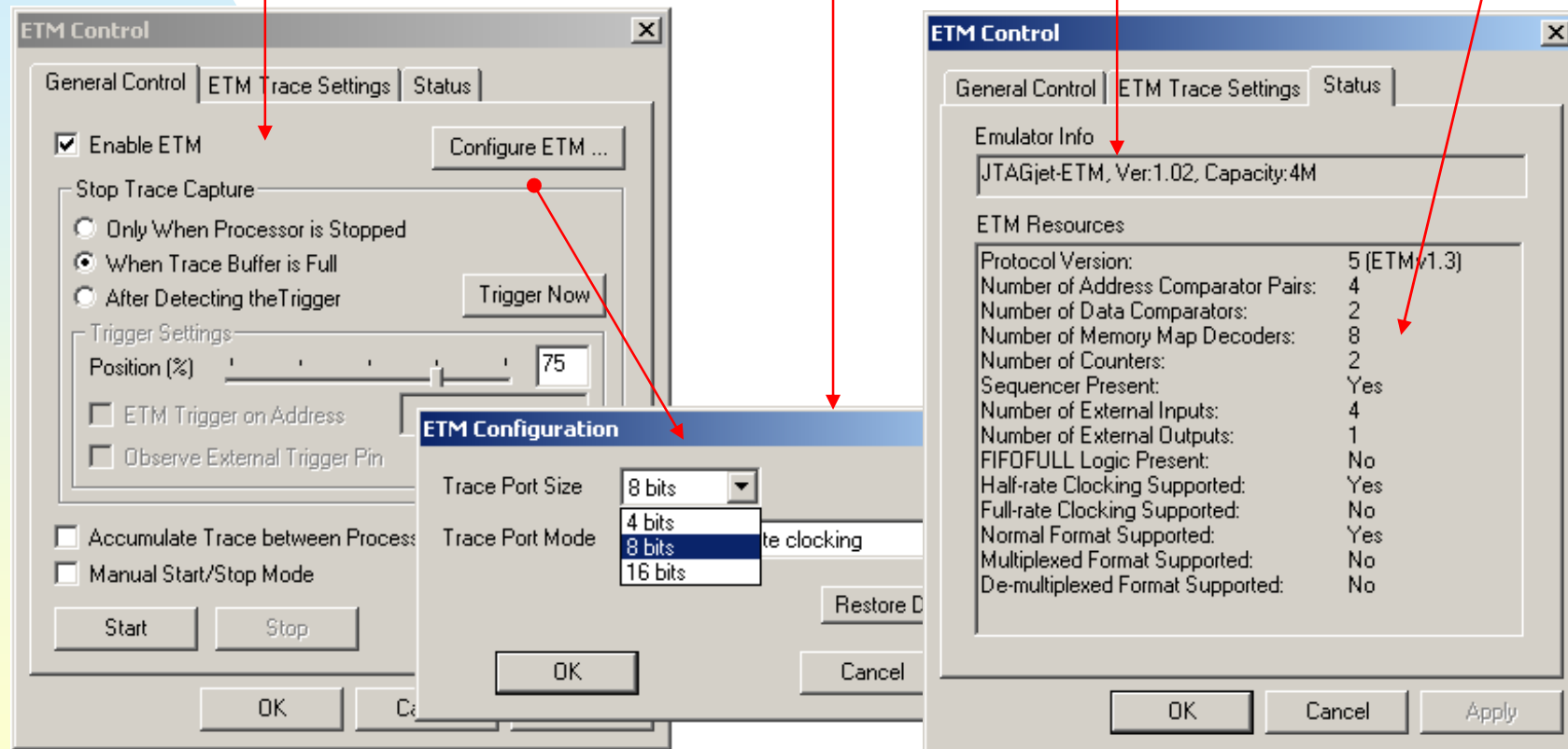
# Trace - ETM Controls and Info

Emulator capture and trigger controls

ETM port mode selection

Emulator info & trace size

On-chip ETM capabilities



# Trace - ETM Pre-Filtering

ETM Control

General Control ETM Trace Settings Status

Program Counter (PC) Tracing Mode

- ☐ Capture Complete PC Trace
- ☐ Start PC Capture at Address
- ☐ Start/Stop Tracing on Addresses
- ☒ Capture PC in Address Range

Begin: processing End: {"demo.c"}@25

Data Tracing Mode

- ☒ Capture Data Values
- ☒ Capture Data Addresses
- ☐ Limit Data Tracing to Data Address Range

Begin: End:

OK Cancel Apply

Trace PC in range only. Every call/jump outside range will stop tracing & resume on any return.

Do not trace PC until the code at 'Begin' executes. Useful to start trace on a rare event.

Start/stop mode starts on 'Begin' and stops on 'End' (latch mode)

Data tracing of Values and/or Addresses

Limit data trace in range (very useful in 4-bit mode to prevent FIFO overflows). This range covers all on-chip registers.

Program Counter (PC) Tracing Mode

- ☐ Capture Complete PC Trace
- ☒ Start PC Capture at Address
- ☐ Start/Stop Tracing on Addresses
- ☐ Capture PC in Address Range

Begin: processing End:

Program Counter (PC) Tracing Mode

- ☐ Capture Complete PC Trace
- ☐ Start PC Capture at Address
- ☒ Start/Stop Tracing on Addresses
- ☐ Capture PC in Address Range

Begin: processing End: {"demo.c"}@25

Data Tracing Mode

- ☒ Capture Data Values
- ☒ Capture Data Addresses
- ☒ Limit Data Tracing to Data Address Range

Begin: 0xE000\_0000 End: 0xEFFF\_FFFF

# Trace - Discontinuity

Arm:trace

Control... Start Resume Clear < Query > Query... Filter... Fields... Save...

#	PC	Disas	MemAddr	RdWr	DataAcc	MemData	TStamp [dt] [cyc]	Sync...
#1205	200002B4	ADD R2,R4,#0xa8					+4	
#1206	200002B8	ADD R1,R4,#0xa4					+12	
#1207	200002BC	STR R2,[R1,#0]	200020D4	Wr	Word	200020D8	+2	
#1208	200002C0	SWI 0x123456					+7030398	
#1230	200002C4	ADD R0,R4,#0xa8					+24	Start
#1231	200002C8	LDR R10,[R0,#+0xc]	200020E4	Rd	Word	20000000	+16	
#1239	200002CC	LDR SP,[R0,#+0x8]	200020E0	Rd	Word	20004000	+16	
#1245	200002D0	LDR R3,[R0,#+0x4]	200020DC	Rd	Word	20000000	+32	
#1255	200002D4	LDR R1,[R0,#+0]						
#1256	200002D8	CMP R1,#0						
#1258	200002DC	LDREQ R1,[PC,#+0x374]						
#1263	200002E0	LDREQ R1,[R1,#+0]						

Status: NotActive

Trace Clock: 132.01MHz

Debugging stopped after SWI.  
Big time gap (in CPU cycles).  
Restart of execution (Start).

Arm:trace

Control... Start Resume Clear < Query > Query... Filter... Fields... Save...

#	PC	Disas	MemAddr	RdWr	DataAcc	MemData	TStamp [dt] [...]	Sync...
#262023	processing+0x4	CMP R1,#0					+2	
#262024	processing+0x8	BEQ 0x20000078					+6	
#262027	processing+0x2C	MOV PC,LR					+812	
#262037	processing+0x4	CMP R1,#0					+2	
#262038	processing+0x8	BEQ 0x20000078					+20	
#262041	processing+0xC	LDRSB R1,[R0,#+0]	Bufl[0]	Rd	Byte	53	+2	ON
#262042	processing+0x10	CMP R1,#0x20					+2	
#262043	processing+0x14	BEQ 0x20000078					+20	
#262047	processing+0x18	LDRB R1,[R0,#+0]	Bufl[0]	Rd	Byte	53	+2	
#262048	processing+0x1C	EOR R1,R1,#0x20					+10	
#262049	processing+0x20	STRB R1,[R0,#+0]	Bufl[0]	Wr	Byte	73	+2	
#262050	processing+0x24	ADD R0,R0,#0x1						
#262051	processing+0x28	B processing						
#262056	processing	LDRSB R1,[R0,#+0]						
#262057	processing+0x4	CMP R1,#0						

Status: NotActive,Full

Trace Clock: 132.01MHz

Conditional trace (PC range).  
Not collecting for 812 cycles.  
Restart of collection (ON).

# Trace - Synchronization with Source

```
SRC Arm:source.1 - source mode {C:\Sig\Chameleon\arm\29900\Arm\Demos\BoardSupport\TI\OMAP\Demo\demo...}
38: led_init(); /* initialize LED module */
39:
40: for (;;) { /* repeat forever */
41:     if (GlobalStruct.Counter & 1) { /* toggle the LED */
42:         led_set(1);
43:     } else {
44:         led_set(0);
45:     }
46:     for (i = 0; i < delayloop; i++) { /* repeat */
```

1) Click on source line in Source Window.

2) Set Code Focus as a search mode

3) Use < and > buttons to search for this line in trace (backward, forward)

4) Use filtering to see only such lines in trace

Arm:trace

Control... Start Resume Clear < Code Focus > Query... Filter... Fields...

#	PC	Disas	Source	Mem...	R
#5608	200000AC	LDR R0,[R0,#+0]		20002014	..
#5609	200000B0	TST R0,#0x1			
#5610	200000B4	BEQ 0x200000C4			
#5611	200000B8	MOV R0,#0x1	led_set(1);		
#5612	200000BC	BL			
#5616	20000210	LDR R1,[PC,#-0x0]		2000020C	..
#5621	20000214	STR R0,[R1,#+0]		20000208	..
#5628	20000218	LDR R1,[PC,#-0x14]	led++;	2000020C	..
#5634	2000021C	LDR R1,[R1,#+0x4]		2000020C	..

Status: NotActive Last Sample #262119 (100%)

✓ Tag  
Tag only PC = 200000B8  
And Tag with PC = 200000B8

✓ Filter  
Filter only PC = 200000B8  
Or Filter with PC = 200000B8  
Filter non-empty PC ...

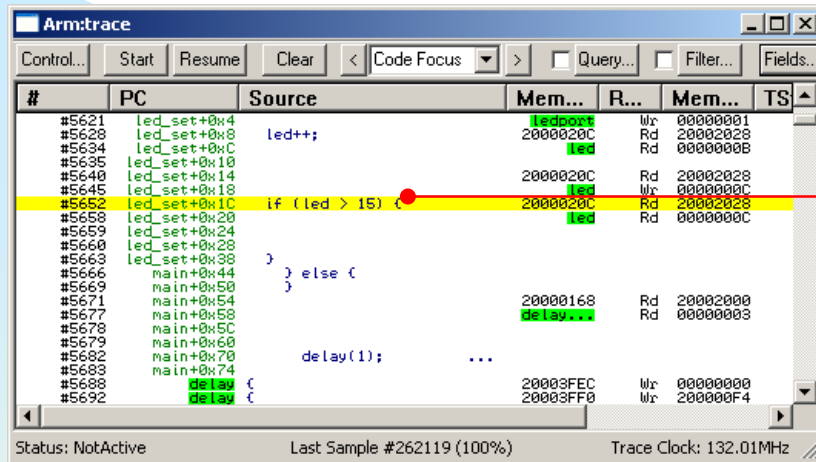
Arm:trace

Control... Start Resume Clear < Code Focus > Query... Filter... Fields...

#	PC	Disas	Source
#5611	200000B8	MOV R0,#0x1	led_set(1);
#10798	200000B8	MOV R0,#0x1	led_set(1);
#15988	200000B8	MOV R0,#0x1	led_set(1);
#21168	200000B8	MOV R0,#0x1	led_set(1);
#26373	200000B8	MOV R0,#0x1	led_set(1);
#31563	200000B8	MOV R0,#0x1	led_set(1);
#36754	200000B8	MOV R0,#0x1	led_set(1);
#41942	200000B8	MOV R0,#0x1	led_set(1);
#47130	200000B8	MOV R0,#0x1	led_set(1);

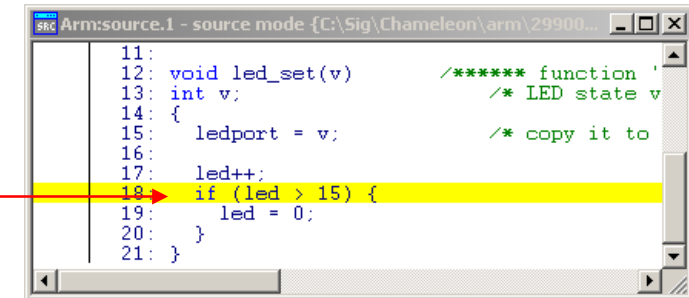
Status: NotActive Last Sample #262119 (100%)

# Trace - Synchronization to source



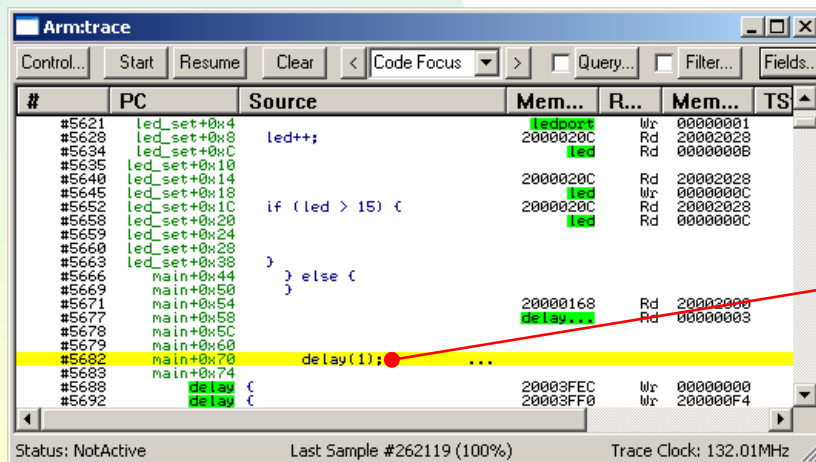
#	PC	Source	Mem...	R...	Mem...	TS
#5621	led_set+0x4		ledport	Wr	00000001	
#5628	led_set+0x8	led++;	2000020C	Rd	20002028	
#5634	led_set+0xC		led	Rd	0000000B	
#5635	led_set+0x10					
#5640	led_set+0x14		2000020C	Rd	20002028	
#5645	led_set+0x18		led	Wr	0000000C	
#5652	led_set+0x1C	if (led > 15) {	2000020C	Rd	20002028	
#5658	led_set+0x20		led	Rd	0000000C	
#5659	led_set+0x24					
#5660	led_set+0x28					
#5663	led_set+0x38					
#5666	main+0x44	} else {				
#5669	main+0x50		20000168	Rd	20002000	
#5671	main+0x54		delay...	Rd	00000003	
#5677	main+0x58					
#5678	main+0x5C					
#5679	main+0x60	delay(1);	...			
#5682	main+0x70					
#5688	main+0x74		20003FEC	Wr	00000000	
#5692	main+0x78		20003FF0	Wr	200000F4	

Status: NotActive      Last Sample #262119 (100%)      Trace Clock: 132.01MHz



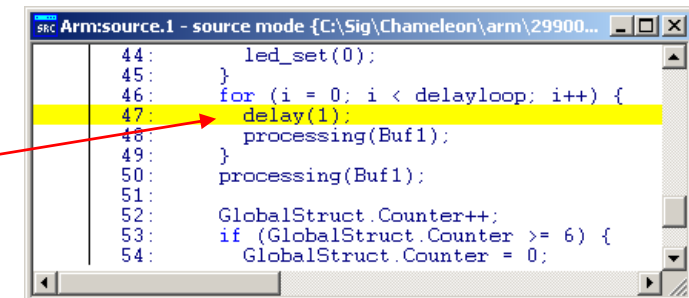
```
11:
12: void led_set(v)          /****** function '
13: int v;                  /* LED state v
14: {
15:     ledport = v;         /* copy it to
16:
17:     led++;
18:
19:     if (led > 15) {
20:         led = 0;
21:     }
```

Click on any trace frame and the Source Window will show the corresponding source line instantly. Scroll back and forth the trace to see the program flow.



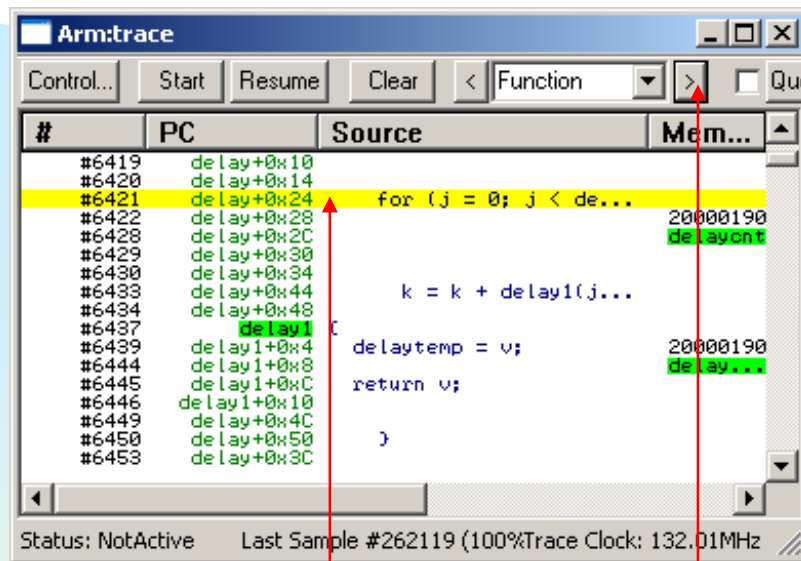
#	PC	Source	Mem...	R...	Mem...	TS
#5621	led_set+0x4		ledport	Wr	00000001	
#5628	led_set+0x8	led++;	2000020C	Rd	20002028	
#5634	led_set+0xC		led	Rd	0000000B	
#5635	led_set+0x10					
#5640	led_set+0x14		2000020C	Rd	20002028	
#5645	led_set+0x18		led	Wr	0000000C	
#5652	led_set+0x1C	if (led > 15) {	2000020C	Rd	20002028	
#5658	led_set+0x20		led	Rd	0000000C	
#5659	led_set+0x24					
#5660	led_set+0x28					
#5663	led_set+0x38					
#5666	main+0x44	} else {				
#5669	main+0x50		20000168	Rd	20002000	
#5671	main+0x54		delay...	Rd	00000003	
#5677	main+0x58					
#5678	main+0x5C					
#5679	main+0x60	delay(1);	...			
#5682	main+0x70					
#5688	main+0x74		20003FEC	Wr	00000000	
#5692	main+0x78		20003FF0	Wr	200000F4	

Status: NotActive      Last Sample #262119 (100%)      Trace Clock: 132.01MHz



```
44:     led_set(0);
45: }
46: for (i = 0; i < delayloop; i++) {
47:     delay(1);
48:     processing(Buf1);
49: }
50: processing(Buf1);
51:
52: GlobalStruct.Counter++;
53: if (GlobalStruct.Counter >= 6) {
54:     GlobalStruct.Counter = 0;
```

# Trace - Function Navigation



Initial position (in function delay)

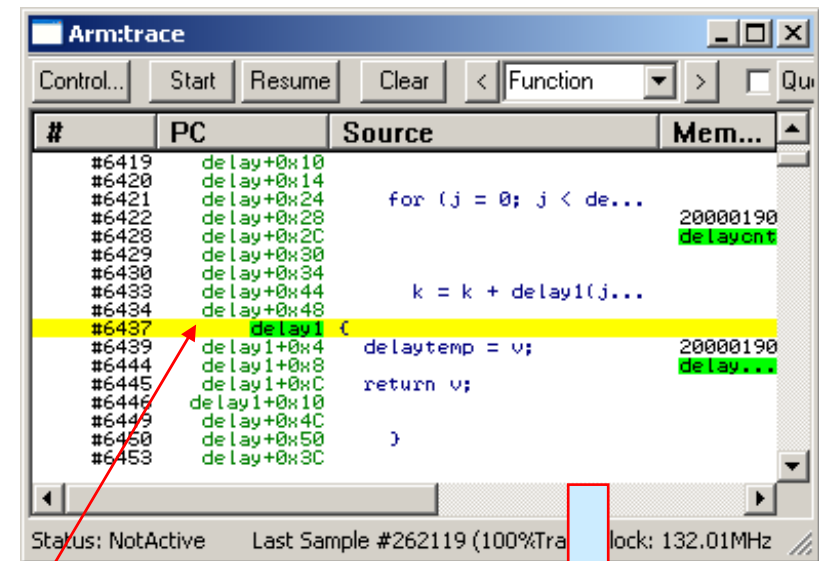
#	PC	Source	Mem...
#6419	delay+0x10		
#6420	delay+0x14		
#6421	delay+0x24	for (j = 0; j < de...	20000190 delaycnt
#6422	delay+0x28		
#6428	delay+0x2C		
#6429	delay+0x30		
#6430	delay+0x34		
#6433	delay+0x44	k = k + delay1(j...	
#6434	delay+0x48		
#6437	delay+0x4C	delay1 (	20000190 delay...
#6439	delay+0x44	delaytemp = v;	
#6444	delay+0x08		
#6445	delay+0x0C	return v;	
#6446	delay+0x10		
#6449	delay+0x4C		
#6450	delay+0x50	)	
#6453	delay+0x3C		

Status: NotActive Last Sample #262119 (100%Trace Clock: 132.01MHz)

Initial position  
(in function delay)

After 1-st click on >  
(in function delay1)

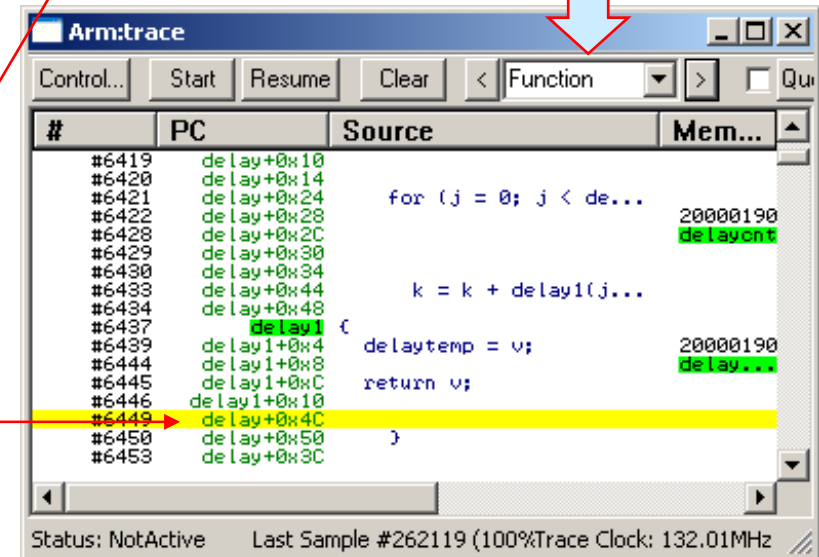
After 2-nd click on >  
(back in function delay -  
after return from delay1)



After 1-st click on > (in function delay1)

#	PC	Source	Mem...
#6419	delay+0x10		
#6420	delay+0x14		
#6421	delay+0x24	for (j = 0; j < de...	20000190 delaycnt
#6422	delay+0x28		
#6428	delay+0x2C		
#6429	delay+0x30		
#6430	delay+0x34		
#6433	delay+0x44	k = k + delay1(j...	
#6434	delay+0x48		
#6437	delay+0x4C	delay1 (	20000190 delay...
#6439	delay+0x44	delaytemp = v;	
#6444	delay+0x08		
#6445	delay+0x0C	return v;	
#6446	delay+0x10		
#6449	delay+0x4C		
#6450	delay+0x50	)	
#6453	delay+0x3C		

Status: NotActive Last Sample #262119 (100%Trace Clock: 132.01MHz)



After 2-nd click on > (back in function delay - after return from delay1)

#	PC	Source	Mem...
#6419	delay+0x10		
#6420	delay+0x14		
#6421	delay+0x24	for (j = 0; j < de...	20000190 delaycnt
#6422	delay+0x28		
#6428	delay+0x2C		
#6429	delay+0x30		
#6430	delay+0x34		
#6433	delay+0x44	k = k + delay1(j...	
#6434	delay+0x48		
#6437	delay+0x4C	delay1 (	20000190 delay...
#6439	delay+0x44	delaytemp = v;	
#6444	delay+0x08		
#6445	delay+0x0C	return v;	
#6446	delay+0x10		
#6449	delay+0x4C		
#6450	delay+0x50	)	
#6453	delay+0x3C		

Status: NotActive Last Sample #262119 (100%Trace Clock: 132.01MHz)

# Trace - Function/Module Navigation

#	PC	Source
#910	main+0x78	processing(Buf1); ...
#911	main+0x7C	
#914	processing	{
#915	processing+0x4	
#916	processing+0x8	
#919	processing+0xC	if (*text != ' ') { ...
#920	processing+0x10	
#921	processing+0x14	
#924	processing+0x18	*text ^= 0x20; ...
#925	processing+0x1C	
#926	processing+0x20	

Status: NotActive Last Sample #262119 (100%) Trace Clock: 132.01MHz

**Function** - function processing found (in same module as main).

#	PC	Source
#910	main+0x78	processing(Buf1); ...
#911	main+0x7C	
#914	processing	{
#915	processing+0x4	
#916	processing+0x8	
#919	processing+0xC	if (*text != ' ') { ...
#920	processing+0x10	
#921	processing+0x14	
#924	processing+0x18	*text ^= 0x20; ...
#925	processing+0x1C	
#926	processing+0x20	

Status: NotActive Last Sample #262119 (100%) Trace Clock: 132.01MHz

**Module** - function processing skipped (in same module as main). delay in different module found.

#	PC	Source
#910	main+0x78	processing(Buf1); ...
#911	main+0x7C	
#914	processing	{
#915	processing+0x4	
#916	processing+0x8	
#919	processing+0xC	if (*text != ' ') { ...
#920	processing+0x10	
#921	processing+0x14	
#924	processing+0x18	*text ^= 0x20; ...
#925	processing+0x1C	
#926	processing+0x20	

Status: NotActive Last Sample #262119 (100%) Trace Clock: 132.01MHz

#	PC	Source
#1214	delay	{
#1218	delay	{
#1222	delay+0x4	
#1223	delay+0x8	k = 0;
#1224	delay+0xC	for (i = 0; i < ont; i++) {
#1225	delay+0x10	
#1226	delay+0x14	
#1227	delay+0x24	for (j = 0; j < delayont; j...
#1228	delay+0x28	
#1234	delay+0x2C	
#1235	delay+0x30	

Status: NotActive Last Sample #262119 (100%) Trace Clock: 132.01MHz

# Trace - Timestamp Display

Timestamp is captured with CPU cycle accuracy - captured time can be shown in **3 modes (Absolute, Relative & Delta)** and as **CPU cycles** or **time units**.

#	PC	Disas	TStamp [dt] [cyc]	TStamp [rel] [cyc]	TStamp [abs] [ms]
#1052	main	STMFD SP!, {R4, LR}	+422	0	324.9
#1081	led_set	LDR R1, [PC, #-0xc]	+204616	422	324.9
#38145	led_set	LDR R1, [PC, #-0xc]	+204128	205038	325.6
#75223	led_set	LDR R1, [PC, #-0xc]	+204120	409168	326.4
#112288	led_set	LDR R1, [PC, #-0xc]	+204128	613286	327.2
#149368	led_set	LDR R1, [PC, #-0xc]	+204120	817414	327.9
#186432	led_set	LDR R1, [PC, #-0xc]	+204136	1021534	328.7
#223515	led_set	LDR R1, [PC, #-0xc]	+204120	1225670	329.5
#260579	led_set	LDR R1, [PC, #-0xc]	+0	1429790	330.3

Status: NotActive, Full      Trace Full (100%)      Trace Clock: 132.01M

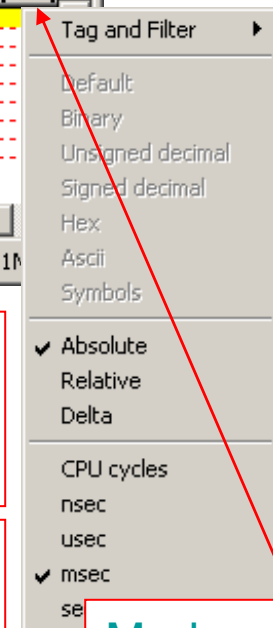
Functions selected  
(by post-filtering)

**Absolute mode (in ms)**  
shows time since CPU  
start.

**Relative mode (in CPU cycles)**. Sample  
#1052 is time reference sample.

**Delta mode (in CPU cycles)** shows distance in time  
to next displayed sample 422 cycles from main to  
led\_set. About 204120 cycles between led\_set calls.

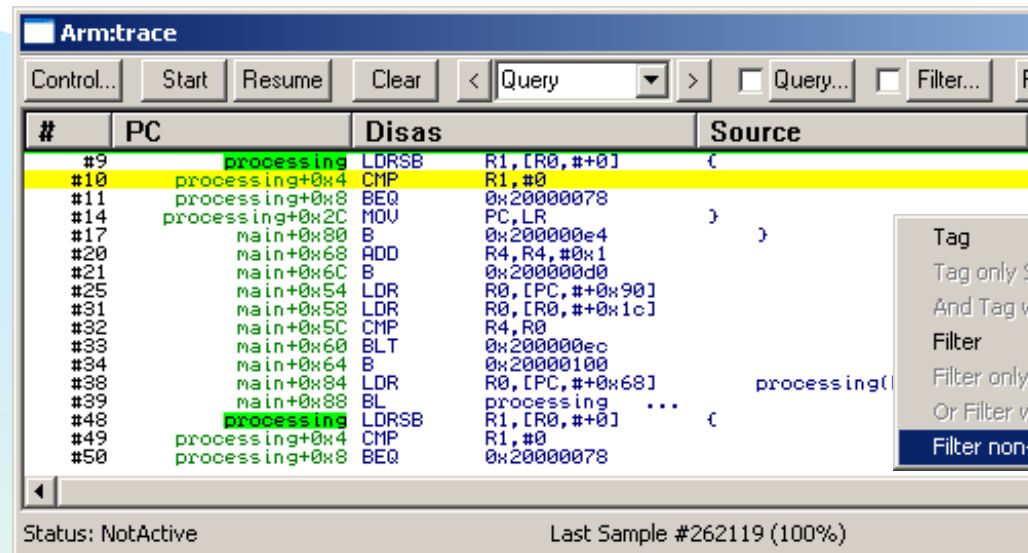
Red  
discontinuity  
marker  
(between  
post-filtered  
samples)



Mode  
change  
(click on  
column)



# Trace - Quick Filtering (sources)



**Before:**

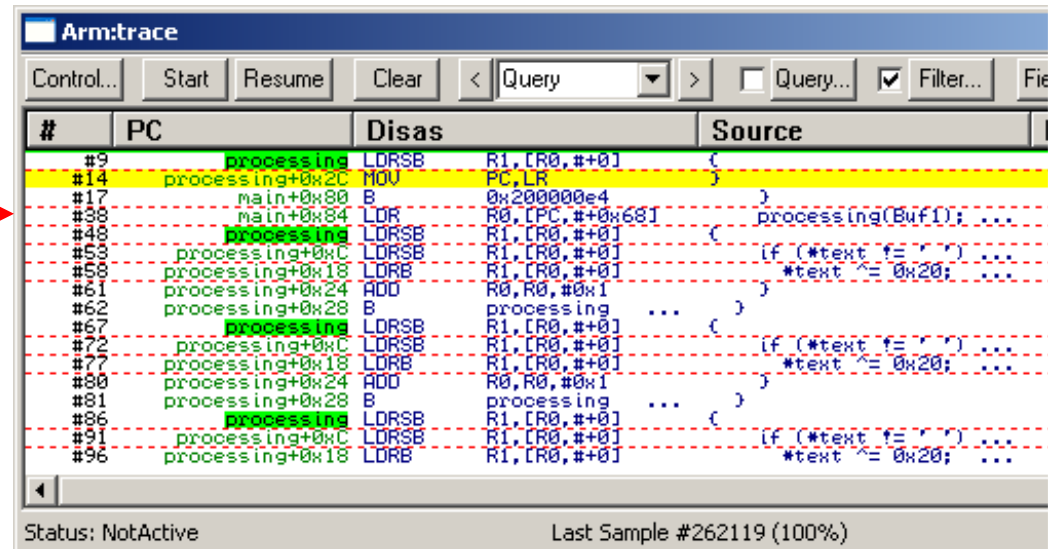
Code without sources visible.



Double-click popup menu

**After:**

Only code with sources visible.



# Trace - Complex Filtering (1)

Trace filter query

PC: (any)  
Disas: (any)  
Source: (any)  
MemAddr: (0x20002000) <= Value <= (0x20002002)  
RdWr: (any)  
MemData: (any)  
DataAcc: (any)  
SyncCode: (any)  
CpuMode: (any)

Field condition

☐ Don't care  
☐ Field == A  
☐ (Field & Mask) == A  
☒ (Field & Mask) >= A && (Field & Mask) <= B  
☐ Field contains string A

A = 0x20002000  
B = 0x20002002  
Mask =

Help... OK Cancel

Display samples with memory address in specified range.

Buf[0] tagged.

MemAddr as symbols and number.

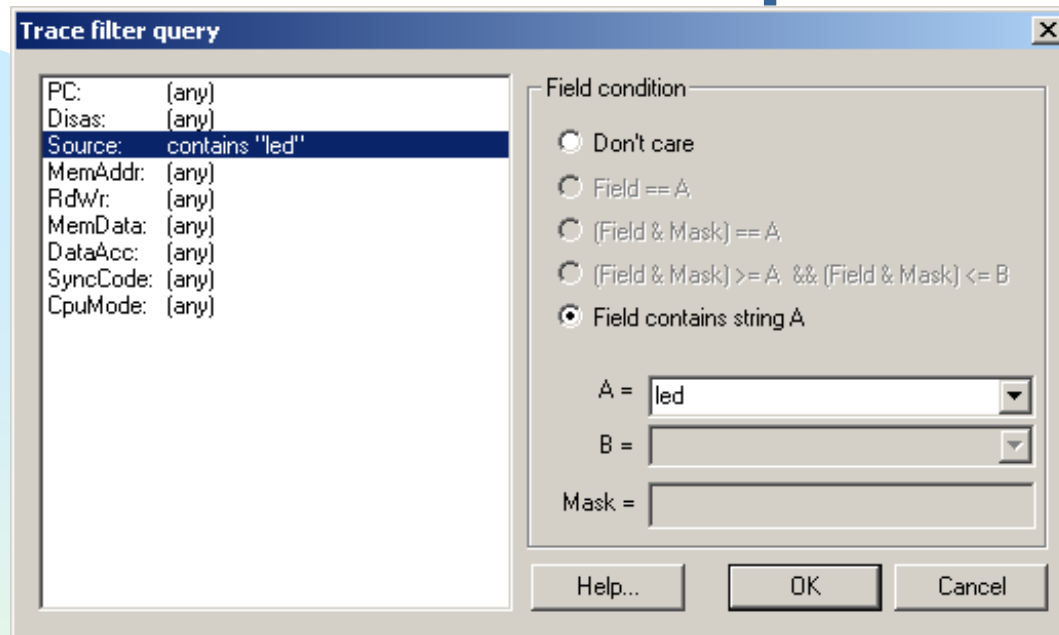
Arm:trace

Control... Start Resume Clear < Query > [x] Query... [x] Filter... Fields... Save...

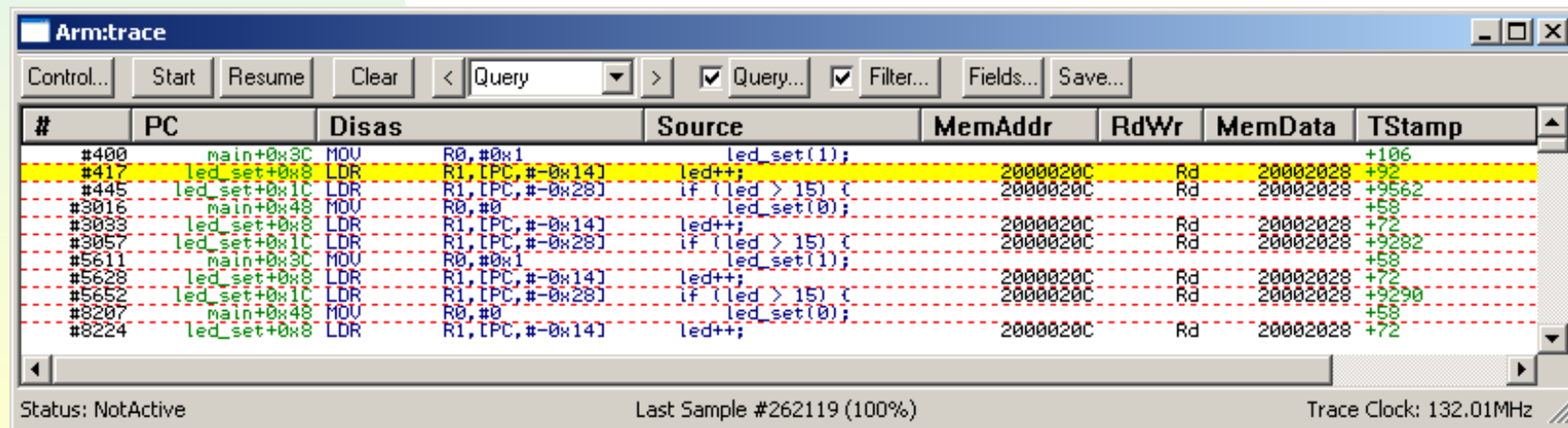
#	PC	Disas	MemAddr	MemAddr	RdWr	MemData	TStamp
#964	processing+0x20	STRB R1,[R0,#0]	Buf[12]	20002002	Wr	67 +2328	
#1635	processing	LDRSB R1,[R0,#0]	Buf[10]	20002000	Rd	73 +24	
#1640	processing+0x18	LDRSB R1,[R0,#0]	Buf[10]	20002000	Rd	73 +24	
#1645	processing+0x18	LDRSB R1,[R0,#0]	Buf[10]	20002000	Rd	73 +12	
#1647	processing+0x20	STRB R1,[R0,#0]	Buf[10]	20002000	Wr	53 +28	
#1656	processing	LDRSB R1,[R0,#0]	Buf[10]	20002001	Rd	69 +24	
#1661	processing+0x18	LDRSB R1,[R0,#0]	Buf[10]	20002001	Rd	69 +24	
#1666	processing+0x18	LDRB R1,[R0,#0]	Buf[10]	20002001	Rd	69 +12	
#1668	processing+0x20	STRB R1,[R0,#0]	Buf[10]	20002001	Wr	49 +28	
#1675	processing	LDRSB R1,[R0,#0]	Buf[12]	20002002	Rd	67 +24	
#1680	processing+0x18	LDRSB R1,[R0,#0]	Buf[12]	20002002	Rd	67 +24	
#1685	processing+0x18	LDRB R1,[R0,#0]	Buf[12]	20002002	Rd	67 +12	
#1687	processing+0x20	STRB R1,[R0,#0]	Buf[12]	20002002	Wr	47 +2328	
#2369	processing	LDRSB R1,[R0,#0]	Buf[10]	20002000	Rd	53 +24	
#2364	processing+0x18	LDRSB R1,[R0,#0]	Buf[10]	20002000	Rd	53 +24	
#2369	processing+0x18	LDRB R1,[R0,#0]	Buf[10]	20002000	Rd	53 +12	

Status: NotActive Last Sample #262119 (100%) Trace Clock: 132.01MHz

# Trace - Complex Filtering (2)



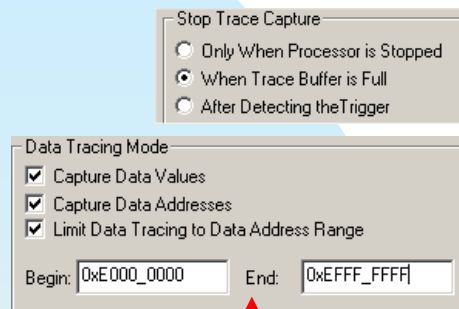
Display only samples with text "led" in Source field.



# Tracing CPU Initialization

ETM is disabled on power-up and CPU reset. Start from 0 needed.

Full trace captured, CPU still running.



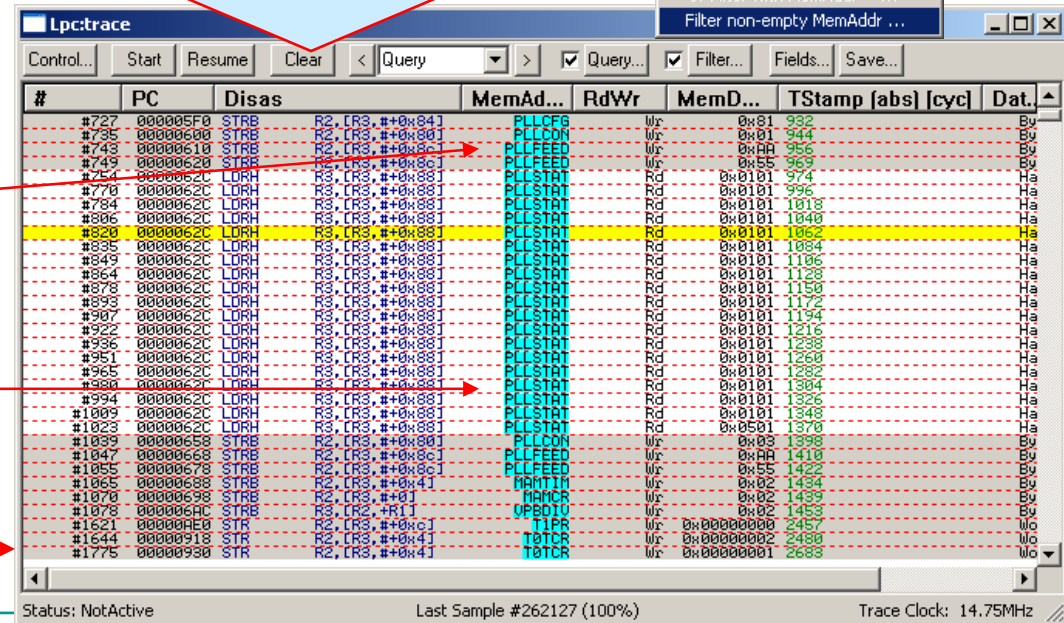
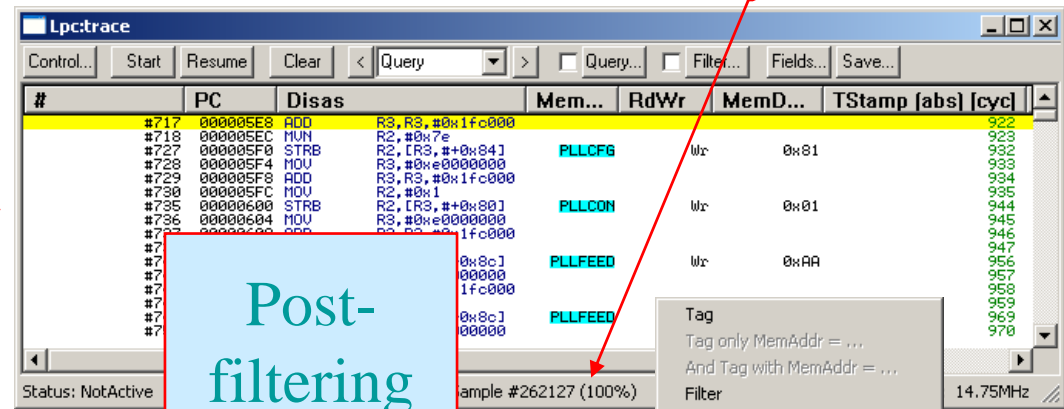
Start from 0

Data trace for registers only!!  
(very important in 4-bit ETM).

All register accesses visible  
(PLL initialization).

Loop while waiting for PLL  
setup (reading PLLSTAT)

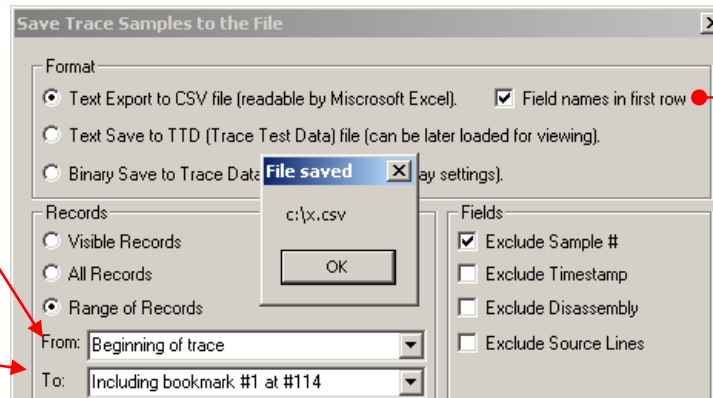
All writes tagged (RdWr=Wr)



# Trace - Save to EXCEL File

Limiting range of records to save.

Bookmark



Field names in first row.

Saved file (shown in split view).

LpcTrace

Control... Start Resume Clear < Query > Query... F

#	PC	PC	MemAddr	RdWr	MemData
#32	0x40000080	0x40000080			
#36	C_Entry+0x4	0x400000E0			
#37	C_Entry+0x4	0x400000E0			
#38	C_Entry+0x8	0x400000E4			
#39	C_Entry+0xC	0x400000E8			
#40	C_Entry+0x10	0x400000EC			
#41	C_Entry+0x14	0x400000F0			
#42	C_Entry+0x18	0x400000F4			
#43	C_Entry+0x1C	0x400000F8			
#46	led_init	0x4000024C			
#47	led_init+0x4	0x40000250			
#48	led_init+0x8	0x40000254			
#49	led_init+0xC	0x40000258			
#50	led_init+0x10	0x4000025C			
#51	led_init+0x14	0x40000260			
#53	led_init+0x18	0x40000264	IO1DIR	Wtr	0x00FF0000
#54	led_init+0x1C	0x40000268			
#70	led_init+0x20	0x4000026C			
#71	led_init+0x24	0x40000270			
#73	led_init+0x28	0x40000274			
#74	led_init+0x2C	0x40000278	IO1CLR	Wtr	0x00FF0000
#79	C_Entry+0x20	0x400000FC			
#82	C_Entry+0x24	0x40000100			
#83	C_Entry+0x28	0x40000104			
#84	C_Entry+0x2C	0x40000108			
#87	C_Entry+0x30	0x40000118			
#88	C_Entry+0x40	0x4000011C			
#93	led_set	0x40000280			
#94	led_set+0x4	0x40000284			
#95	led_set+0x8	0x40000288			
#96	led_set+0xC	0x4000028C			
#99	led_set+0x24	0x400002A4			
#100	led_set+0x28	0x400002A8			
#101	led_set+0x2C	0x400002AC			
#103	led_set+0x30	0x400002B0			
#104	led_set+0x34	0x400002B4			
#107	C_Entry+0x44	0x40000120			
#110	C_Entry+0x48	0x40000124			
#113	C_Entry+0x50	0x4000012C			
#114	C_Entry+0x54	0x40000130			
#115	C_Entry+0x58	0x40000134			
#118	C_Entry+0x64	0x40000140			

Status: NotActive Last Sample #262133 (100%) Trace Clock: 6.00MHz

Save to CSV

Register name

Last saved sample (Bookmark #1)

X.csv

	A	B	C	D	E
1	PC	PC	MemAddr	RdWr	MemData
2	0x40000000	0x40000000			
3	0x40000020	0x40000020			
4	0x40000024	0x40000024			
5	0x40000028	0x40000028			
46	C_Entry+0x28	0x40000104			
47	C_Entry+0x2C	0x40000108			
48	C_Entry+0x3C	0x40000118			
49	C_Entry+0x40	0x4000011C			
50	led_set	0x40000280			
51	led_set+0x4	0x40000284			
52	led_set+0x8	0x40000288			
53	led_set+0xC	0x4000028C			
54	led_set+0x24	0x400002A4			
55	led_set+0x28	0x400002A8			
56	led_set+0x2C	0x400002AC			
57	led_set+0x30	0x400002B0			
58	led_set+0x34	0x400002B4			
59	C_Entry+0x44	0x40000120			
60	C_Entry+0x48	0x40000124			
61	C_Entry+0x4C	0x40000128			
62	C_Entry+0x50	0x4000012C			
63					

# Trace - Command Line Access

Short info

Complete settings  
display

Command help

```
C:\> Lpc:command.1

>trace info
JTAGjet-ETM, Ver:1.04, Capacity:256K, TraceSW:1.31, ETMArch:1.2, ETMRev:2

>trace
JTAGjet-ETM, Ver:1.04, Capacity:256K, TraceSW:1.31, ETMArch:1.2, ETMRev:2
Status: NotActive      Last Sample #262127 (100%)      Trace Clock: 12.00MHz
trace ctrl stop=full
trace ctrl triggerpos=50
trace ctrl accumulate=off
trace ctrl manual=off
trace etm pc=all
trace etm data=all
trace etm portsize=8
trace etm halfrate=off

>trace help
General commands
TRACE
- display info, status and all settings
TRACE HELP
- help of trace commands (this description)
TRACE STATUS
- display trace collection status
TRACE INFO
- display trace module info
TRACE DISABLE
- disable trace module (as non-existed)
TRACE ENABLE
- enable trace module
TRACE CLEAR
- clear trace buffer
```

# Trace - Integration with External Debuggers (CCS/ADS/GNU/etc.)

