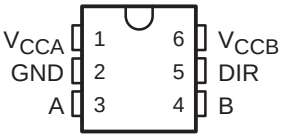
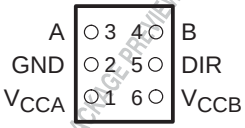
- **Available in the Texas Instruments NanoStar™ and NanoFree™ Packages**
- **Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.65-V to 5.5-V Power-Supply Range**
- **$V_{CC}$ Isolation Feature − If Either $V_{CC}$ Input Is at GND, Both Ports Are in the High-Impedance State**
- **DIR Input Circuit Referenced to $V_{CCA}$**
- **Low Power Consumption, 4-μA Max $I_{CC}$**
- **±24-mA Output Drive at 3.3 V**
- **$I_{off}$ Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

**DBV OR DCK PACKAGE**
**(TOP VIEW)**




**YEP OR YZP PACKAGE**
**(BOTTOM VIEW)**






## description/ordering information

This single-bit noninverting bus transceiver uses two separate configurable power-supply rails. The A-port is designed to track $V_{CCA}$. $V_{CCA}$ accepts any supply voltage from 1.65 V to 5.5 V. The B-port is designed to track $V_{CCB}$. $V_{CCB}$ accepts any supply voltage from 1.65 V to 5.5 V. This allows for universal low-voltage bidirectional translation between any of the 1.8-V, 2.5-V, 3.3-V, and 5-V voltage nodes.

The SN74LVC1T45 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input.

**ORDERING INFORMATION**

| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING‡ |
|---|---|---|---|---|
| −40°C to 85°C | NanoStar™ − WCSP (DSBGA) 0.23-mm Large Bump − YEP | Reel of 3000 | SN74LVC1T45YEPR | _ _ _TA_ |
| | NanoFree™ − WCSP (DSBGA) 0.23-mm Large Bump − YZP (Pb-free) | | SN74LVC1T45YZPR | |
| | SOT (SOT-23) − DBV | Reel of 3000 | SN74LVC1T45DBVR | CT1_ |
| | | Reel of 250 | SN74LVC1T45DBVT | |
| | SOT (SC-70) − DCK | Reel of 3000 | SN74LVC1T45DCKR | TA_ |
| | | Reel of 250 | SN74LVC1T45DCKT | |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

‡ DBV/DCK: The actual top-side marking has one additional character that designates the assembly/test site.
YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, ● = Pb-free).

## description/ordering information (continued)

The SN74LVC1T45 is designed so that DIR input circuit is supplied by $V_{CCA}$.

This device is fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

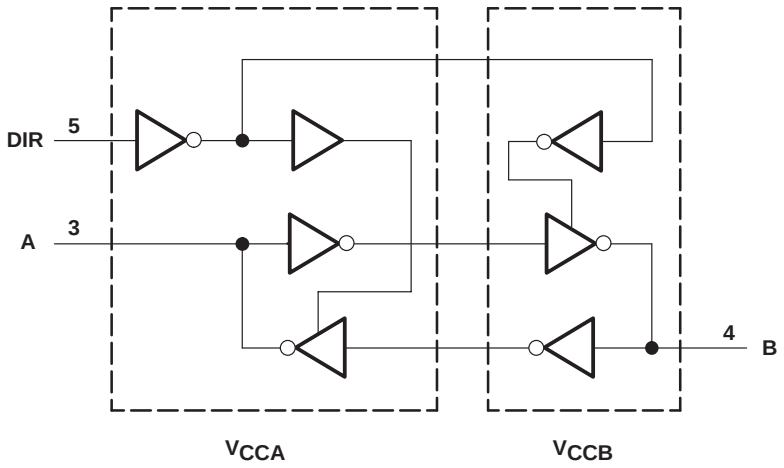
The $V_{CC}$ isolation feature ensures that if either $V_{CC}$ input is at GND, then both ports are in the high-impedance state.

NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

**FUNCTION TABLE**

| INPUT DIR | OPERATION |
|---|---|
| L | B data to A bus |
| H | A data to B bus |

## logic diagram (positive logic)



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

| | |
|---|---|
| Supply voltage range, $V_{CCA}$ and $V_{CCB}$ | −0.5 V to 6.5 V |
| Input voltage range, $V_I$ (see Note 1) | −0.5 V to 6.5 V |
| Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1) | −0.5 V to 6.5 V |
| Voltage range applied to any output in the high or low state, $V_O$ (see Notes 1 and 2): A port | −0.5 V to $V_{CCA}$ + 0.5V |
| B port | −0.5 V to $V_{CCB}$ + 0.5V |
| Input clamp current, $I_{IK}$ ($V_I$ < 0) | −50 mA |
| Output clamp current, $I_{OK}$ ($V_O$ < 0) | −50 mA |
| Continuous output current, $I_O$ | ±50 mA |
| Continuous current through $V_{CC}$ or GND | ±100 mA |
| Package thermal impedance, $\theta_{JA}$ (see Note 3): DBV package | 165°C/W |
| DCK package | 259°C/W |
| YEP/YZP package | 123°C/W |
| Storage temperature range, $T_{stg}$ | −65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The value of $V_{CC}$ is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Notes 4 through 8)

| | | | $V_{CCI}$ | $V_{CCO}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{CCA}$ | Supply voltage | | | | 1.65 | 5.5 | V |
| $V_{CCB}$ | | | | | 1.65 | 5.5 | |
| $V_{IH}$ | High-level input voltage | Data inputs (see Note 7) | 1.65 V to 1.95 V | | $V_{CCI} \times 0.65$ | | V |
| | | | 2.3 V to 2.7 V | | 1.7 | | |
| | | | 3 V to 3.6 V | | 2 | | |
| | | | 4.5 V to 5.5 V | | $V_{CCI} \times 0.7$ | | |
| $V_{IL}$ | Low-level input voltage | Data inputs (see Note 7) | 1.65 V to 1.95 V | | | $V_{CCI} \times 0.35$ | V |
| | | | 2.3 V to 2.7 V | | | 0.7 | |
| | | | 3 V to 3.6 V | | | 0.8 | |
| | | | 4.5 V to 5.5 V | | | $V_{CCI} \times 0.3$ | |
| $V_{IH}$ | High-level input voltage | DIR (Referenced to $V_{CCA}$) (see Note 8) | 1.65 V to 1.95 V | | $V_{CCA} \times 0.65$ | | V |
| | | | 2.3 V to 2.7 V | | 1.7 | | |
| | | | 3 V to 3.6 V | | 2 | | |
| | | | 4.5 V to 5.5 V | | $V_{CCA} \times 0.7$ | | |
| $V_{IL}$ | Low-level input voltage | DIR (Referenced to $V_{CCA}$) (see Note 8) | 1.65 V to 1.95 V | | | $V_{CCA} \times 0.35$ | V |
| | | | 2.3 V to 2.7 V | | | 0.7 | |
| | | | 3 V to 3.6 V | | | 0.8 | |
| | | | 4.5 V to 5.5 V | | | $V_{CCA} \times 0.3$ | |
| $V_I$ | Input voltage | | | | 0 | 5.5 | V |
| $V_O$ | Output voltage | | | | 0 | $V_{CCO}$ | V |
| $I_{OH}$ | High-level output current | | | 1.65 V to 1.95 V | | −4 | mA |
| | | | | 2.3 V to 2.7 V | | −8 | |
| | | | | 3 V to 3.6 V | | −24 | |
| | | | | 4.5 V to 5.5 V | | −32 | |
| $I_{OL}$ | Low-level output current | | | 1.65 V to 1.95 V | | 4 | mA |
| | | | | 2.3 V to 2.7 V | | 8 | |
| | | | | 3 V to 3.6 V | | 24 | |
| | | | | 4.5 V to 5.5 V | | 32 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | Data input | 1.65 V to 1.95 V | | | 20 | ns/V |
| | | | 2.3 V to 2.7 V | | | 20 | |
| | | | 3 V to 3.6 V | | | 10 | |
| | | | 4.5 V to 5.5 V | | | 5 | |
| | | Control input | 1.65 V to 5.5 V | | | 5 | |
| $T_A$ | Operating free-air temperature | | | | −40 | 85 | °C |

NOTES: 4. $V_{CCI}$ is the $V_{CC}$ associated with the data input port.
5. $V_{CCO}$ is the $V_{CC}$ associated with the output port.
6. All unused data inputs of the device must be held at $V_{CCI}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
7. For $V_{CCI}$ values not specified in the data sheet, $V_{IH(min)} = V_{CCI} \times 0.7$ V, $V_{IL(max)} = V_{CCI} \times 0.3$ V.
8. For $V_{CCI}$ values not specified in the data sheet, $V_{IH(min)} = V_{CCA} \times 0.7$ V, $V_{IL(max)} = V_{CCA} \times 0.3$ V.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Notes 9 and 10)**

| PARAMETER | | TEST CONDITIONS | | $V_{CCA}$ | $V_{CCB}$ | $T_A$ = 25°C | | | −40°C to 85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | MIN | TYP | MAX | MIN | MAX | |
| $V_{OH}$ | | $I_{OH}$ = −100 μA, $V_I$ = $V_{IH}$ | | 1.65 V to 4.5 V | 1.65 V to 4.5 V | | | | $V_{CCO}$−0.1 V | | V |
| | | $I_{OH}$ = −4 mA, $V_I$ = $V_{IH}$ | | 1.65V | 1.65 V | | | | 1.2 | | |
| | | $I_{OH}$ = −8 mA, $V_I$ = $V_{IH}$ | | 2.3 V | 2.3 V | | | | 1.9 | | |
| | | $I_{OH}$ = −24 mA, $V_I$ = $V_{IH}$ | | 3 V | 3 V | | | | 2.4 | | |
| | | $I_{OH}$ = −32 mA, $V_I$ = $V_{IH}$ | | 4.5 V | 4.5 V | | | | 3.8 | | |
| $V_{OL}$ | | $I_{OL}$ = 100 μA, $V_I$ = $V_{IL}$ | | 1.65 V to 4.5 V | 1.65 V to 4.5 V | | | | | 0.1 | V |
| | | $I_{OL}$ = 4 mA, $V_I$ = $V_{IL}$ | | 1.65 V | 1.65 V | | | | | 0.45 | |
| | | $I_{OL}$ = 8 mA, $V_I$ = $V_{IL}$ | | 2.3 V | 2.3 V | | | | | 0.3 | |
| | | $I_{OL}$ = 24 mA, $V_I$ = $V_{IL}$ | | 3 V | 3 V | | | | | 0.55 | |
| | | $I_{OL}$ = 32 mA, $V_I$ = $V_{IL}$ | | 4.5 V | 4.5 V | | | | | 0.55 | |
| $I_I$ | DIR input | $V_I$ = $V_{CCA}$ or GND | | 1.65 V to 5.5 V | 1.65 V to 5.5 V | | | ±1 | | ±2 | μA |
| $I_{off}$ | A port | $V_I$ or $V_O$ = 0 to 5.5 V | | 0 V | 0 to 5.5 V | | | ±1 | | ±2 | μA |
| | B port | | | 0 to 5.5 V | 0 V | | | ±1 | | ±2 | |
| $I_{OZ}$ | A or B ports | $V_O$ = $V_{CCO}$ or GND | | 1.65 V to 5.5 V | 1.65 V to 5.5 V | | | ±1 | | ±2 | μA |
| $I_{CCA}$ | | $V_I$ = $V_{CCI}$ or GND | $I_O$ = 0 | 1.65 V to 5.5 V | 1.65 V to 5.5 V | | | | | 3 | μA |
| | | | | 5.5 V | 0 V | | | | | 2 | |
| | | | | 0 V | 5.5 V | | | | | 0 | |
| $I_{CCB}$ | | $V_I$ = $V_{CCI}$ or GND | $I_O$ = 0 | 1.65 V to 5.5 V | 1.65 V to 5.5 V | | | | | 3 | μA |
| | | | | 5.5 V | 0 V | | | | | 0 | |
| | | | | 0 V | 5.5 V | | | | | 2 | |
| $I_{CCA}$ + $I_{CCB}$ | | $V_I$ = $V_{CCI}$ or GND | $I_O$ = 0 | 1.65 V to 5.5 V | 1.65 V to 5.5 V | | | | | 4 | μA |
| $\Delta I_{CCA}$ | A port | A port at $V_{CCA}$ − 0.6 V, DIR at $V_{CCA}$, B port = OPEN | | 3 V to 5.5 V | 3 V to 5.5 V | | | | | 50 | μA |
| | DIR | DIR at $V_{CCA}$ − 0.6 V, B port = OPEN, A port at $V_{CCA}$ or GND | | | | | | | | 50 | |
| $\Delta I_{CCB}$ | B port | B port at $V_{CCB}$ − 0.6 V, DIR at GND, A port = OPEN | | 3 V to 5.5 V | 3 V to 5.5 V | | | | | 50 | μA |
| $C_i$ | DIR input | $V_I$ = $V_{CCA}$ or GND | | 3.3 V | 3.3 V | | 2.5 | | | | pF |
| $C_{io}$ | A or B ports | $V_O$ = $V_{CCA/B}$ or GND | | 3.3 V | 3.3 V | | 6 | | | | pF |

NOTES: 9. $V_{CCO}$ is the $V_{CC}$ associated with the output port.
10. $V_{CCI}$ is the $V_{CC}$ associated with the input port.

**switching characteristics over recommended operating free-air temperature range, $V_{CCA}$ = 1.8 V ± 0.15 V(unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CCB}$ = 1.8 V ± 0.15 V | | $V_{CCB}$ = 2.5 V ± 0.2 V | | $V_{CCB}$ = 3.3 V ± 0.3 V | | $V_{CCB}$ = 5 V ± 0.5 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A | B | 3 | 17.7 | 2.2 | 10.3 | 1.7 | 8.3 | 1.4 | 7.2 | ns |
| $t_{PHL}$ | | | 2.8 | 14.3 | 2.2 | 8.5 | 1.8 | 7.1 | 1.7 | 7 | |
| $t_{PLH}$ | B | A | 3 | 17.7 | 2.3 | 16 | 2.1 | 15.5 | 1.9 | 15.1 | ns |
| $t_{PHL}$ | | | 2.8 | 14.3 | 2.1 | 12.9 | 2 | 12.6 | 1.8 | 12.2 | |
| $t_{PHZ}$ | DIR | A | 5.2 | 19.4 | 4.8 | 18.5 | 4.7 | 18.4 | 5.1 | 17.1 | ns |
| $t_{PLZ}$ | | | 2.3 | 10.5 | 2.1 | 10.5 | 2.4 | 10.7 | 3.1 | 10.9 | |
| $t_{PHZ}$ | DIR | B | 7.4 | 21.9 | 4.9 | 11.5 | 4.6 | 10.3 | 2.8 | 8.2 | ns |
| $t_{PLZ}$ | | | 4.2 | 16 | 3.7 | 9.2 | 3.3 | 8.4 | 2.4 | 6.4 | |
| $t_{PZH}$† | DIR | A | | 33.7 | | 25.2 | | 23.9 | | 21.5 | ns |
| $t_{PZL}$† | | | | 36.2 | | 24.4 | | 22.9 | | 20.4 | |
| $t_{PZH}$† | DIR | B | | 28.2 | | 20.8 | | 19 | | 18.1 | ns |
| $t_{PZL}$† | | | | 33.7 | | 27 | | 25.5 | | 24.1 | |

† The enable time is a calculated value, derived using the formula shown in the section entitled *enable times* on page 16.

**switching characteristics over recommended operating free-air temperature range, $V_{CCA}$ = 2.5 V ± 0.2 V(unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CCB}$ = 1.8 V ± 0.15 V | | $V_{CCB}$ = 2.5 V ± 0.2 V | | $V_{CCB}$ = 3.3 V ± 0.3 V | | $V_{CCB}$ = 5 V ± 0.5 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A | B | 2.3 | 16 | 1.5 | 8.5 | 1.3 | 6.4 | 1.1 | 5.1 | ns |
| $t_{PHL}$ | | | 2.1 | 12.9 | 1.4 | 7.5 | 1.3 | 5.4 | 0.9 | 4.6 | |
| $t_{PLH}$ | B | A | 2.2 | 10.3 | 1.5 | 8.5 | 1.4 | 8 | 1 | 7.5 | ns |
| $t_{PHL}$ | | | 2.2 | 8.5 | 1.4 | 7.5 | 1.3 | 7 | 0.9 | 6.2 | |
| $t_{PHZ}$ | DIR | A | 3 | 8.1 | 3.1 | 8.1 | 2.8 | 8.1 | 3.2 | 8.1 | ns |
| $t_{PLZ}$ | | | 1.3 | 5.9 | 1.3 | 5.9 | 1.3 | 5.9 | 1 | 5.8 | |
| $t_{PHZ}$ | DIR | B | 6.5 | 23.7 | 4.1 | 11.4 | 3.9 | 10.2 | 2.4 | 7.1 | ns |
| $t_{PLZ}$ | | | 3.9 | 18.9 | 3.2 | 9.6 | 2.8 | 8.4 | 1.8 | 5.3 | |
| $t_{PZH}$† | DIR | A | | 29.2 | | 18.1 | | 16.4 | | 12.8 | ns |
| $t_{PZL}$† | | | | 32.2 | | 18.9 | | 17.2 | | 13.3 | |
| $t_{PZH}$† | DIR | B | | 21.9 | | 14.4 | | 12.3 | | 10.9 | ns |
| $t_{PZL}$† | | | | 21 | | 15.6 | | 13.5 | | 12.7 | |

† The enable time is a calculated value, derived using the formula shown in the section entitled *enable times* on page 16.

**switching characteristics over recommended operating free-air temperature range, $V_{CCA}$ = 3.3 V ± 0.3 V(unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CCB}$ = 1.8 V ± 0.15 V | | $V_{CCB}$ = 2.5 V ± 0.2 V | | $V_{CCB}$ = 3.3 V ± 0.3 V | | $V_{CCB}$ = 5 V ± 0.5 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A | B | 2.1 | 15.5 | 1.4 | 8 | 0.7 | 5.8 | 0.7 | 4.4 | ns |
| $t_{PHL}$ | | | 2 | 12.6 | 1.3 | 7 | 0.8 | 5 | 0.7 | 4 | |
| $t_{PLH}$ | B | A | 1.7 | 8.3 | 1.3 | 6.4 | 0.7 | 5.8 | 0.6 | 5.4 | ns |
| $t_{PHL}$ | | | 1.8 | 7.1 | 1.3 | 5.4 | 0.8 | 5 | 0.7 | 4.5 | |
| $t_{PHZ}$ | DIR | A | 2.9 | 7.3 | 3 | 7.3 | 2.8 | 7.3 | 3.4 | 7.3 | ns |
| $t_{PLZ}$ | | | 1.8 | 5.6 | 1.6 | 5.6 | 2.2 | 5.7 | 2.2 | 5.7 | |
| $t_{PHZ}$ | DIR | B | 5.4 | 20.5 | 3.9 | 10.1 | 2.9 | 8.8 | 2.4 | 6.8 | ns |
| $t_{PLZ}$ | | | 3.3 | 14.5 | 2.9 | 7.8 | 2.4 | 7.1 | 1.7 | 4.9 | |
| $t_{PZH}$† | DIR | A | | 22.8 | | 14.2 | | 12.9 | | 10.3 | ns |
| $t_{PZL}$† | | | | 27.6 | | 15.5 | | 13.8 | | 11.3 | |
| $t_{PZH}$† | DIR | B | | 21.1 | | 13.6 | | 11.5 | | 10.1 | ns |
| $t_{PZL}$† | | | | 19.9 | | 14.3 | | 12.3 | | 11.3 | |

† The enable time is a calculated value, derived using the formula shown in the section entitled *enable times* on page 16.

**switching characteristics over recommended operating free-air temperature range, $V_{CCA}$ = 5 V ± 0.5 V(unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CCB}$ = 1.8 V ± 0.15 V | | $V_{CCB}$ = 2.5 V ± 0.2 V | | $V_{CCB}$ = 3.3 V ± 0.3 V | | $V_{CCB}$ = 5 V ± 0.5 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A | B | 1.9 | 15.1 | 1 | 7.5 | 0.6 | 5.4 | 0.5 | 3.9 | ns |
| $t_{PHL}$ | | | 1.8 | 12.2 | 0.9 | 6.2 | 0.7 | 4.5 | 0.5 | 3.5 | |
| $t_{PLH}$ | B | A | 1.4 | 7.2 | 1 | 5.1 | 0.7 | 4.4 | 0.5 | 3.9 | ns |
| $t_{PHL}$ | | | 1.7 | 7 | 0.9 | 4.6 | 0.7 | 4 | 0.5 | 3.5 | |
| $t_{PHZ}$ | DIR | A | 2.1 | 5.4 | 2.2 | 5.4 | 2.2 | 5.5 | 2.2 | 5.4 | ns |
| $t_{PLZ}$ | | | 0.9 | 3.8 | 1 | 3.8 | 1 | 3.7 | 0.9 | 3.7 | |
| $t_{PHZ}$ | DIR | B | 4.8 | 20.2 | 2.5 | 9.8 | 1 | 8.5 | 2.5 | 6.5 | ns |
| $t_{PLZ}$ | | | 4.2 | 14.8 | 2.5 | 7.4 | 2.5 | 7 | 1.6 | 4.5 | |
| $t_{PZH}$† | DIR | A | | 22 | | 12.5 | | 11.4 | | 8.4 | ns |
| $t_{PZL}$† | | | | 27.2 | | 14.4 | | 12.5 | | 10 | |
| $t_{PZH}$† | DIR | B | | 18.9 | | 11.3 | | 9.1 | | 7.6 | ns |
| $t_{PZL}$† | | | | 17.6 | | 11.6 | | 10 | | 8.9 | |

† The enable time is a calculated value, derived using the formula shown in the section entitled *enable times* on page 16.

## operating characteristics, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | $V_{CCA}$ = $V_{CCB}$ = 1.8 V | $V_{CCA}$ = $V_{CCB}$ = 2.5 V | $V_{CCA}$ = $V_{CCB}$ = 3.3 V | $V_{CCA}$ = $V_{CCB}$ = 5 V | UNIT |
|---|---|---|---|---|---|---|---|
| | | | TYP | TYP | TYP | TYP | |
| $C_{pdA}$† | A port input, B port output | $C_L$ = 0, f = 10 MHz, $t_r$ = $t_f$ =1 ns | 3 | 4 | 4 | 4 | pF |
| | B port input, A port output | | 18 | 19 | 20 | 21 | |
| $C_{pdB}$† | A port input, B port output | | 18 | 19 | 20 | 21 | |
| | B port input, A port output | | 3 | 4 | 4 | 4 | |

† Power-dissipation capacitance per transceiver

### power-up considerations

A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies. Take the following precautions to guard against such power-up problems:

1. Connect ground before any supply voltage is applied.
2. Power up $V_{CCA}$.
3. $V_{CCB}$ can be ramped up along with or after $V_{CCA}$.

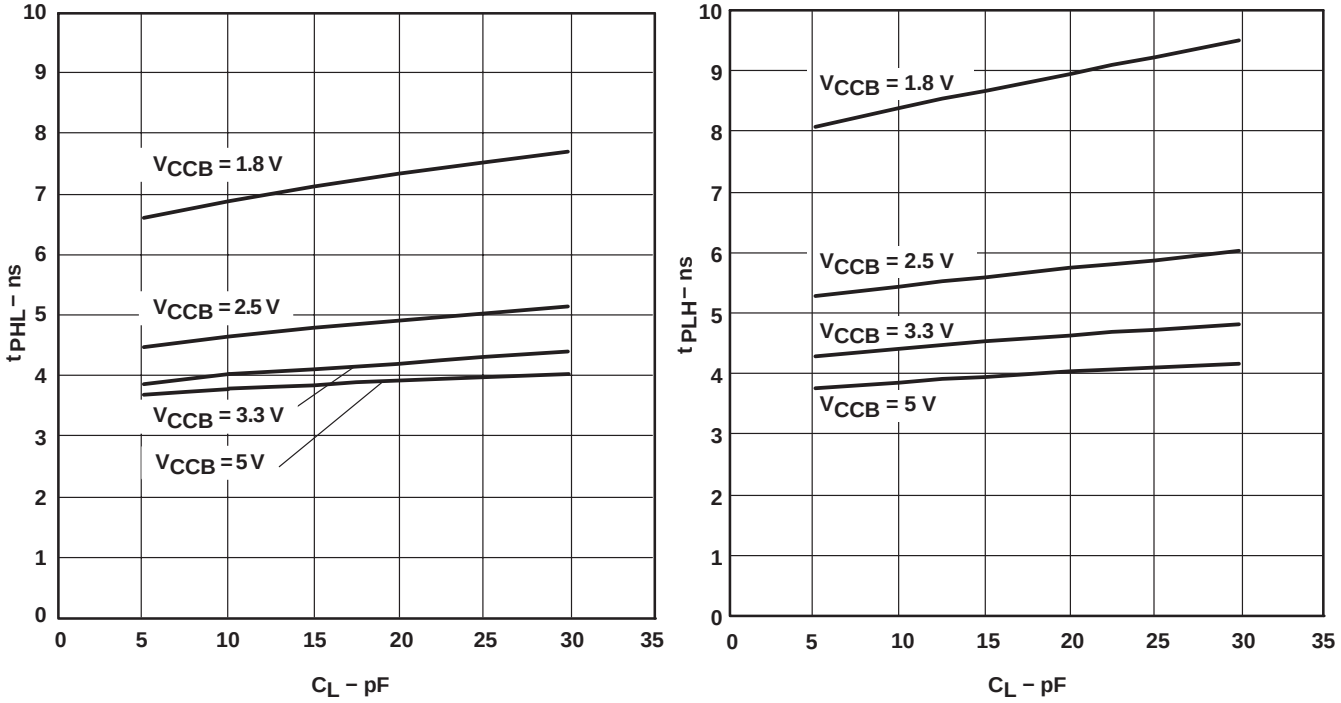
### typical total static power consumption ($I_{CCA}$ + $I_{CCB}$)

**Table 1**

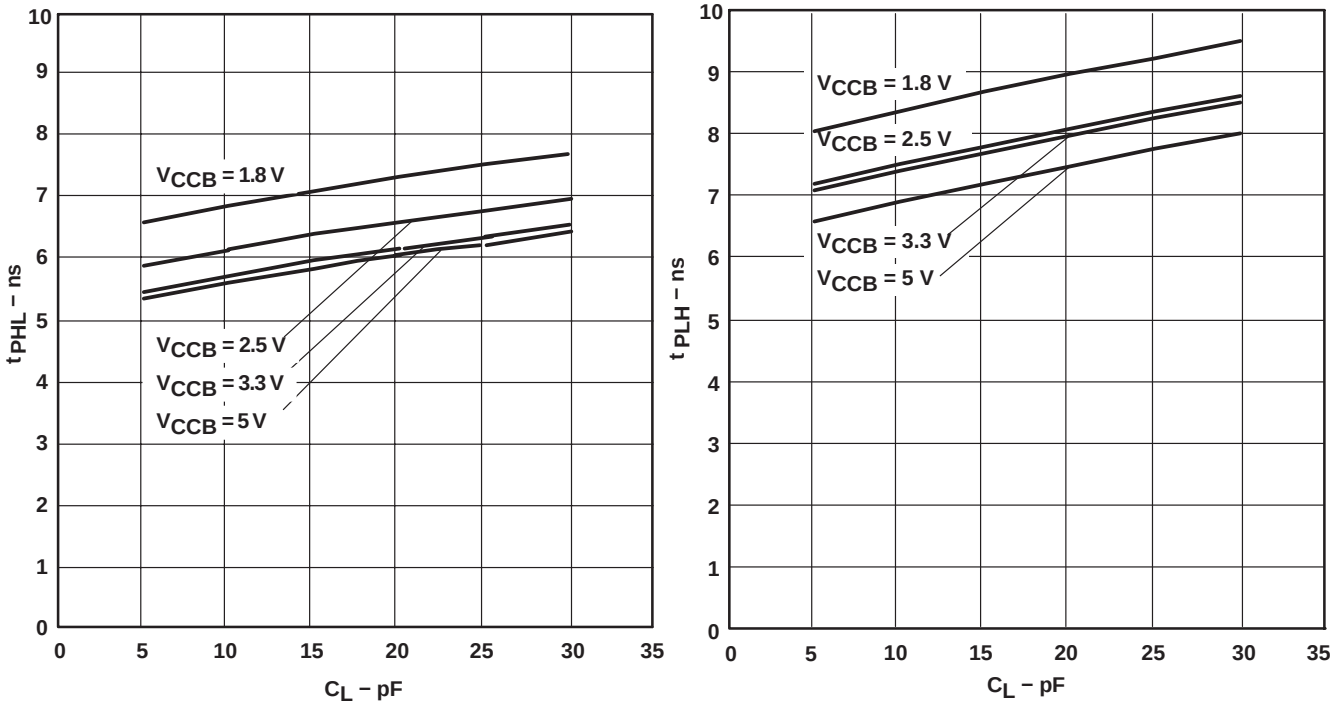
| $V_{CCB}$ | $V_{CCA}$ | | | | | UNIT |
|---|---|---|---|---|---|---|
| | 0 V | 1.8 V | 2.5 V | 3.3 V | 5 V | |
| 0 V | 0 | <1 | <1 | <1 | <1 | μA |
| 1.8 V | <1 | <2 | <2 | <2 | 2 | |
| 2.5 V | <1 | <2 | <2 | <2 | <2 | |
| 3.3 V | <1 | <2 | <2 | <2 | <2 | |
| 5 V | <1 | 2 | <2 | <2 | <2 | |

## TYPICAL CHARACTERISTICS

### TYPICAL PROPAGATION DELAY (A TO B) vs LOAD CAPACITANCE
$T_A = 25°C$, $V_{CCA} = 1.8$ V

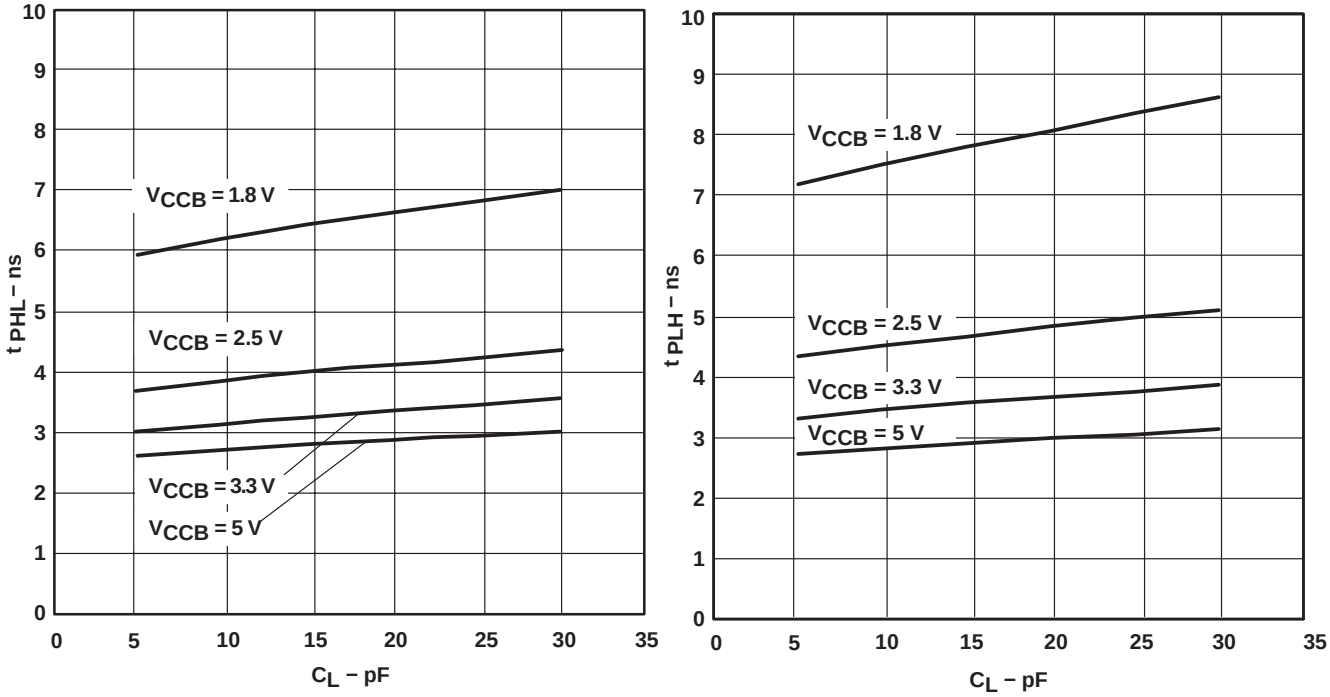



### TYPICAL PROPAGATION DELAY (B TO A) vs LOAD CAPACITANCE
$T_A = 25°C$, $V_{CCA} = 1.8$ V

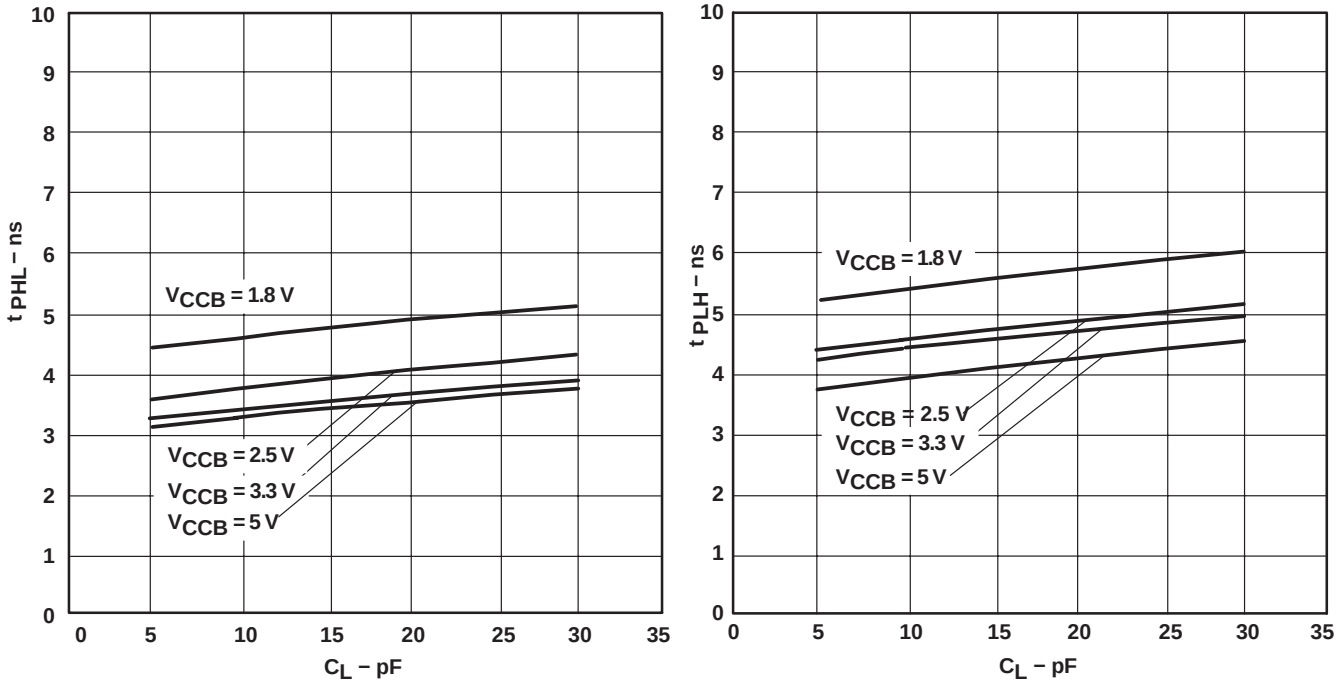


## TYPICAL CHARACTERISTICS

### TYPICAL PROPAGATION DELAY (A TO B) vs LOAD CAPACITANCE
$T_A = 25°C$, $V_{CCA} = 2.5$ V

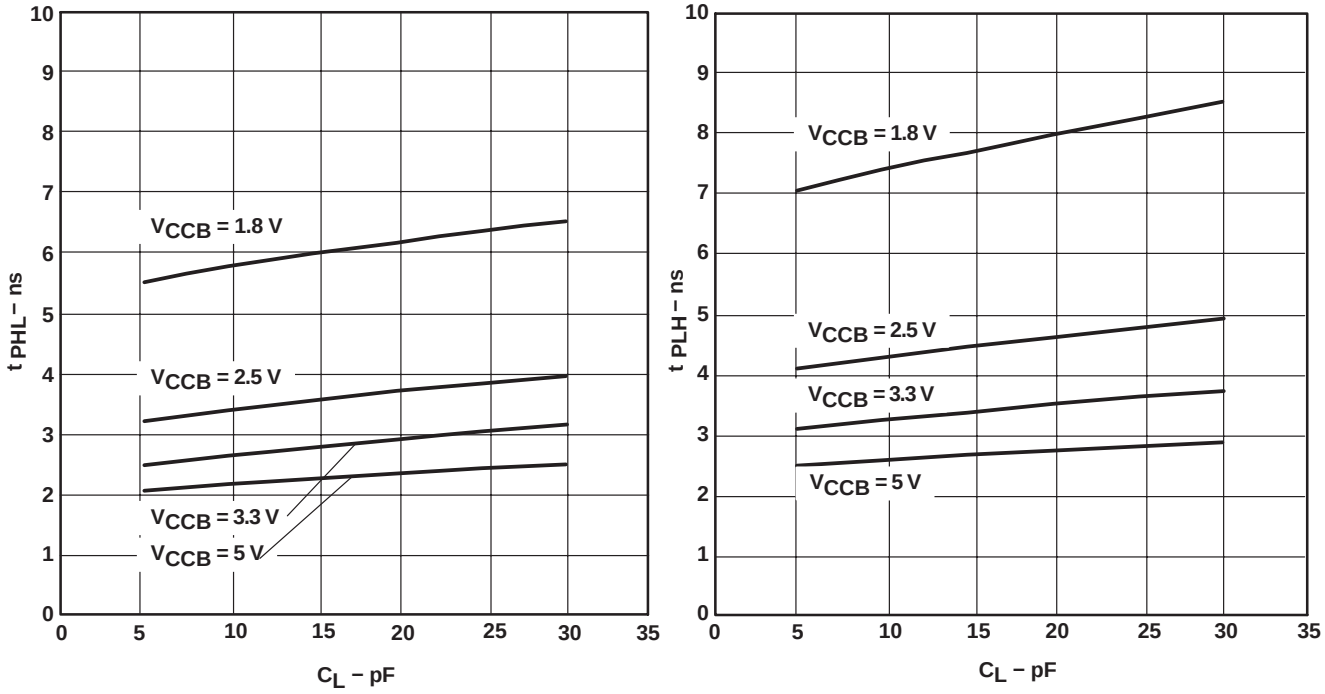



### TYPICAL PROPAGATION DELAY (B TO A) vs LOAD CAPACITANCE
$T_A = 25°C$, $V_{CCA} = 2.5$ V

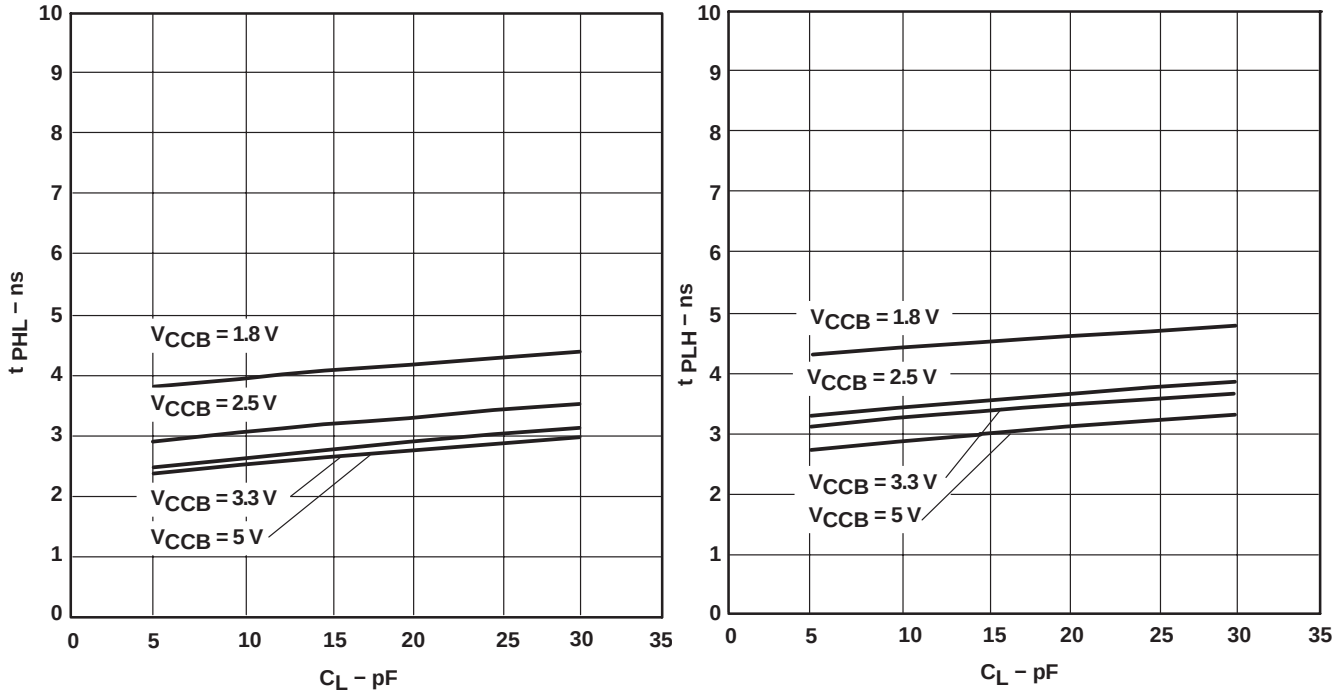


## TYPICAL CHARACTERISTICS

### TYPICAL PROPAGATION DELAY (A TO B) vs LOAD CAPACITANCE
$T_A = 25°C$, $V_{CCA} = 3.3$ V

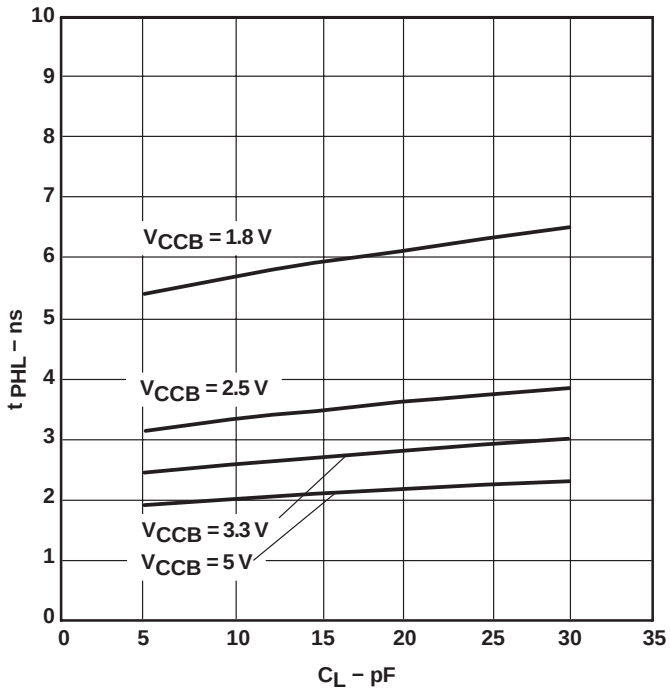


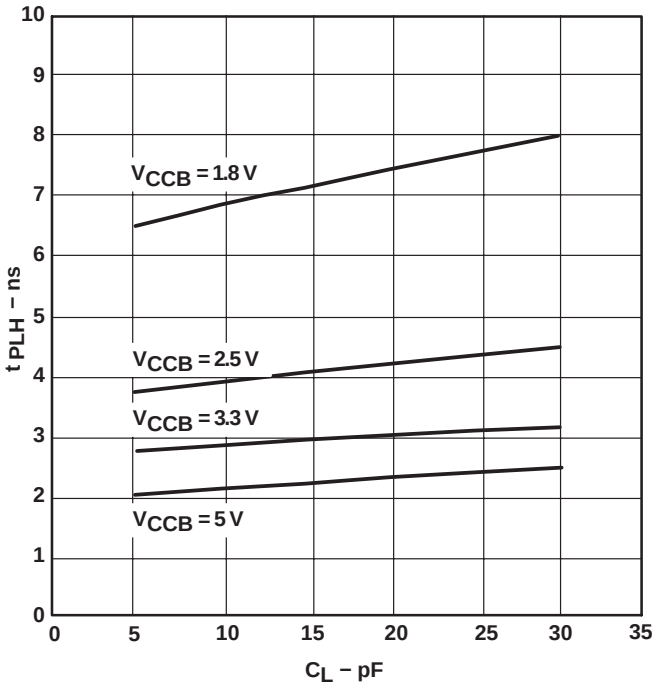

### TYPICAL PROPAGATION DELAY (B TO A) vs LOAD CAPACITANCE
$T_A = 25°C$, $V_{CCA} = 3.3$ V



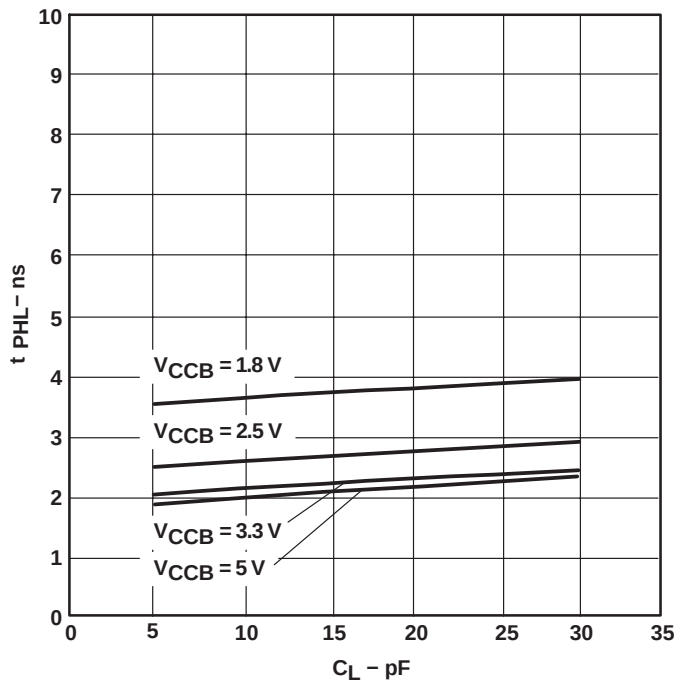
## TYPICAL CHARACTERISTICS

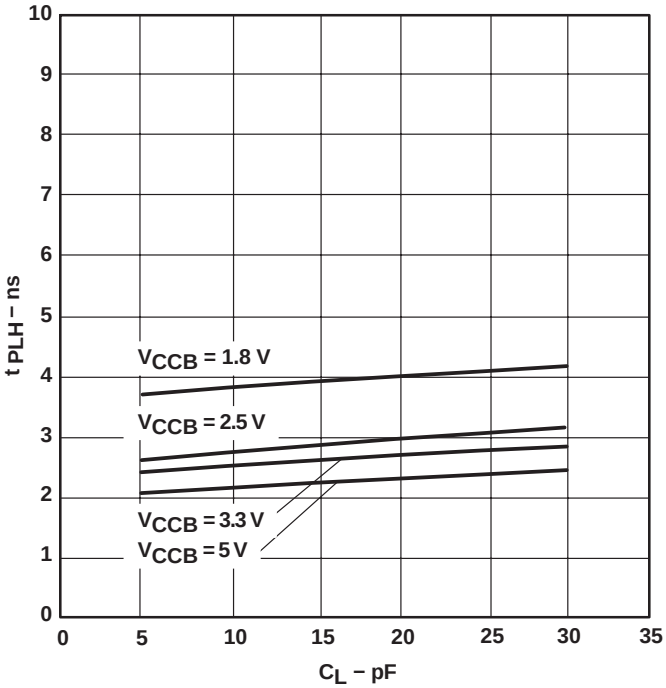
### TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE
$T_A = 25°C$, $V_{CCA} = 5$ V



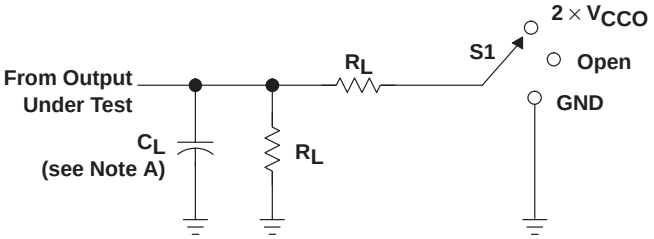




### TYPICAL PROPAGATION DELAY (B TO A) vs LOAD CAPACITANCE
$T_A = 25°C$, $V_{CCA} = 5$ V



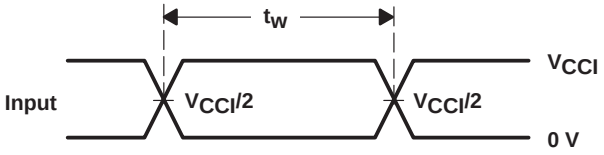
## PARAMETER MEASUREMENT INFORMATION



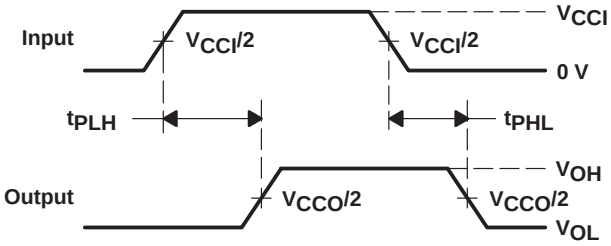

LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{pd}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $2 \times V_{CCO}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

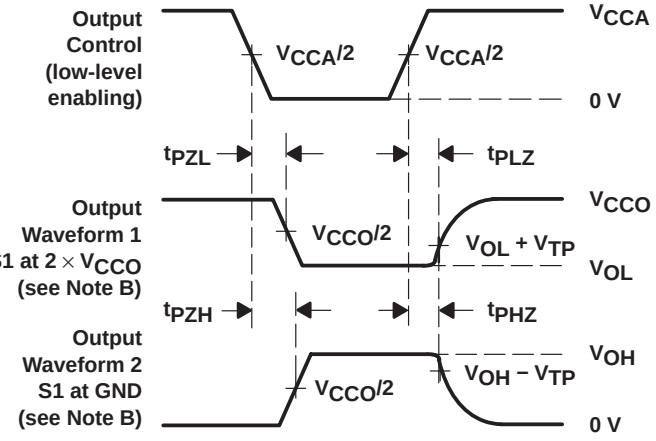
| $V_{CCO}$ | $C_L$ | $R_L$ | $V_{TP}$ |
|---|---|---|---|
| 1.5 V ± 0.1 V | 15 pF | 2 kΩ | 0.1 V |
| 1.8 V ± 0.15 V | 15 pF | 2 kΩ | 0.15 V |
| 2.5 V ± 0.2 V | 15 pF | 2 kΩ | 0.15 V |
| 3.3 V ± 0.3 V | 15 pF | 2 kΩ | 0.3 V |




VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



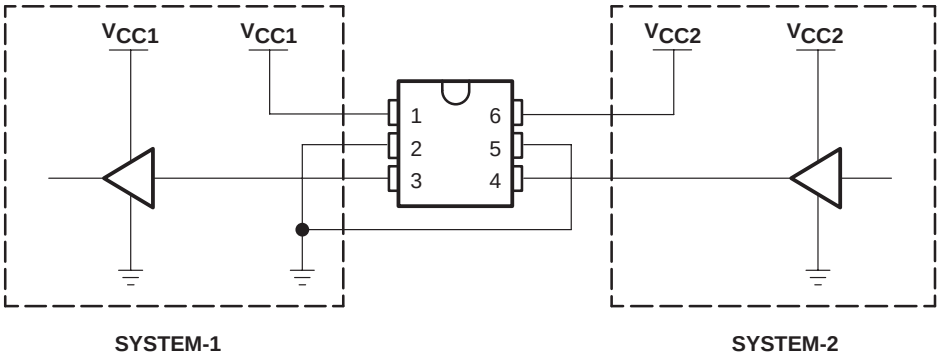

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, dv/dt ≥ 1 V/ns, dv/dt ≥1 V/ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
H. $V_{CCI}$ is the $V_{CC}$ associated with the input port.
I. $V_{CCO}$ is the $V_{CC}$ associated with the output port.
J. All parameters and waveforms are not applicable to all devices.

**Figure 2. Load Circuit and Voltage Waveforms**

## APPLICATION INFORMATION

The following circuit is an example of the SN74LVC1T45 being used in a unidirectional logic level-shifting application.

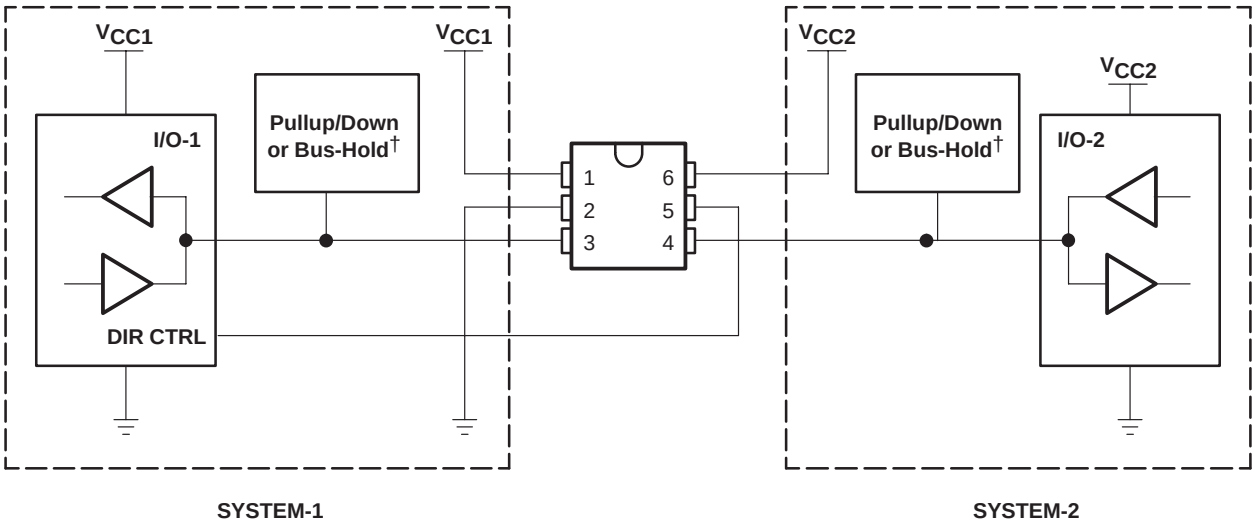



| PIN | NAME | FUNCTION | DESCRIPTION |
|---|---|---|---|
| 1 | $V_{CCA}$ | $V_{CC1}$ | SYSTEM-1 supply voltage (1.65 V to 5.5 V) |
| 2 | GND | GND | Device GND |
| 3 | A | OUT | Output level depends on $V_{CC1}$ voltage |
| 4 | B | IN | Input threshold value depends on $V_{CC2}$ voltage |
| 5 | DIR | DIR | The GND (low level) determines B-port to A-port direction |
| 6 | $V_{CCB}$ | $V_{CC2}$ | SYSTEM-2 supply voltage (1.65 V to 5.5 V) |

**Figure 3. Unidirectional Logic Level-Shifting Application**

## APPLICATION INFORMATION

Figure 4 shows the SN74LVC1T45 being used in a bidirectional logic level-shifting application. Since the SN74LVC1T45 does not have an output enable (OE) pin, the system designer should take precautions to avoid bus contention between SYSTEM-1 and SYSTEM-2 when changing directions.




Following is a sequence that illustrates data transmission from SYSTEM-1 to SYSTEM-2 and then from SYSTEM-2 to SYSTEM-1.

| STATE | DIR CTRL | I/O 1 | I/O 2 | DESCRIPTION |
|---|---|---|---|---|
| 1 | H | OUT | IN | SYSTEM-1 data to SYSTEM-2 |
| 2 | H | HI-Z | HI-Z | SYSTEM-2 is getting ready to send data to SYSTEM-1. I/O-1 and I/O-2 are disabled. The bus-line state depends on pullup or pulldown† |
| 3 | L | HI-Z | HI-Z | DIR bit is flipped. I/O-1 and I/O-2 are still disabled. The bus-line state depends on pullup or pulldown† |
| 4 | L | OUT | IN | SYSTEM-2 data to SYSTEM-1 |

† SYSTEM-1 and SYSTEM-2 must use the same conditions, i.e., both pullup or both pulldown.

**Figure 4. Bidirectional Logic Level-Shifting Application**

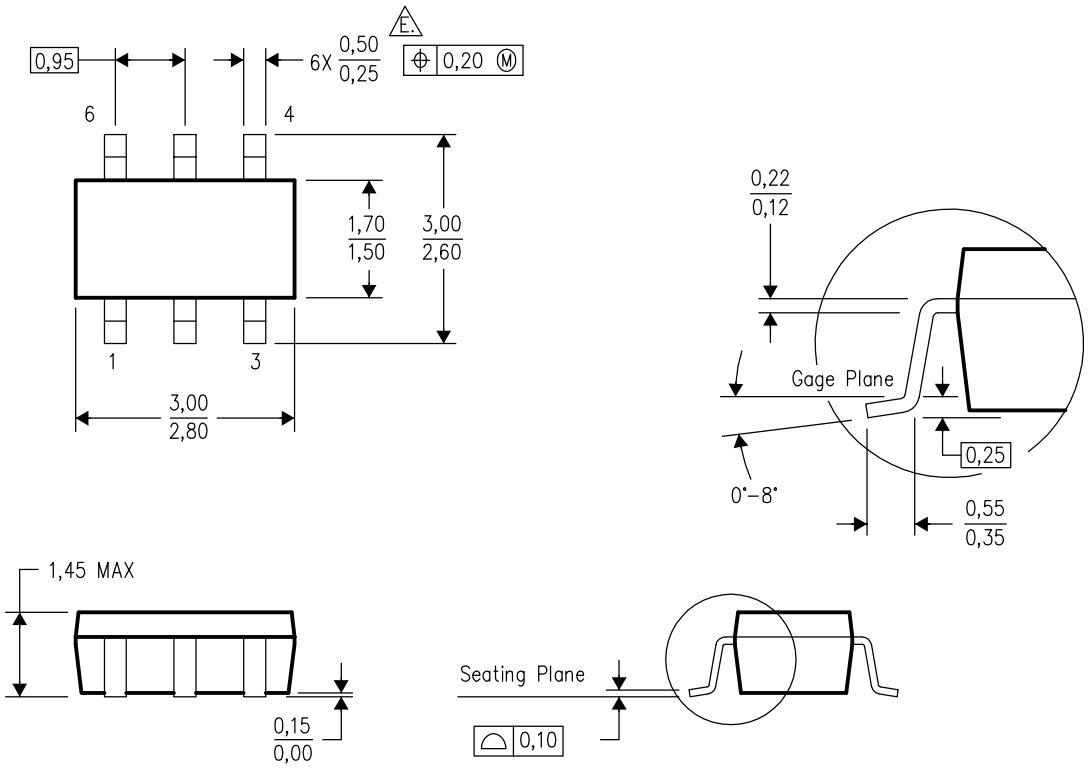
### enable times

Calculate the enable times for the SN74LVC1T45 using the following formulas:

1. $t_{PZH}$ (DIR to A) = $t_{PLZ}$ (DIR to B) + $t_{PLH}$ (B to A)
2. $t_{PZL}$ (DIR to A) = $t_{PHZ}$ (DIR to B) + $t_{PHL}$ (B to A)
3. $t_{PZH}$ (DIR to B) = $t_{PLZ}$ (DIR to A) + $t_{PLH}$ (A to B)
4. $t_{PZL}$ (DIR to B) = $t_{PHZ}$ (DIR to A) + $t_{PHL}$ (A to B)

In a bidirectional application, these enable times provide the maximum delay from the time DIR bit is switched until an output is expected. For example, if the SN74LVC1T45 initially is transmitting from A to B, then the DIR bit is switched, the B port of the device must be disabled before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay.

## DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE




4073253–5/H 10/2003

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

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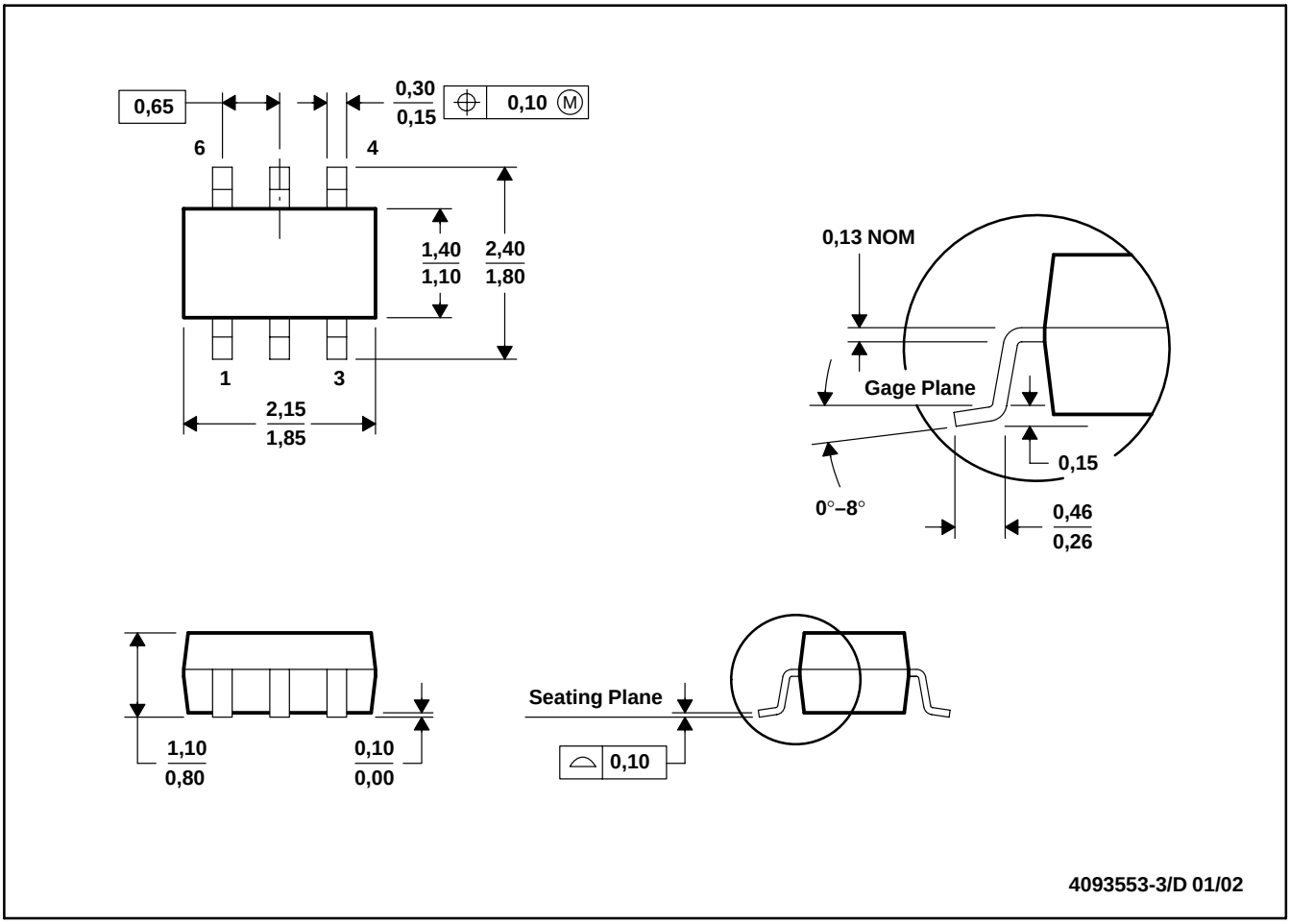
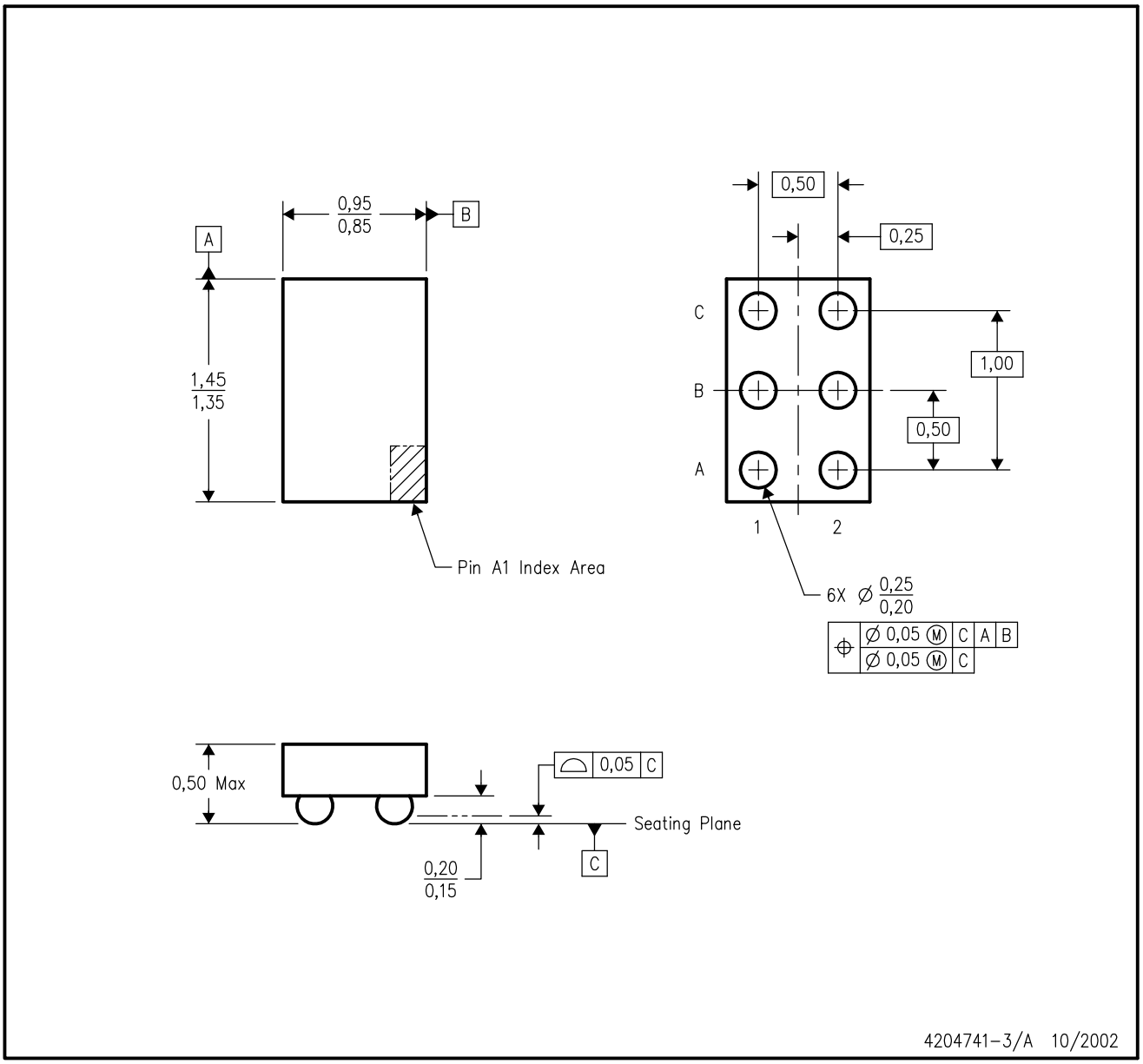
**DCK (R-PDSO-G6)** **PLASTIC SMALL-OUTLINE PACKAGE**




NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-203

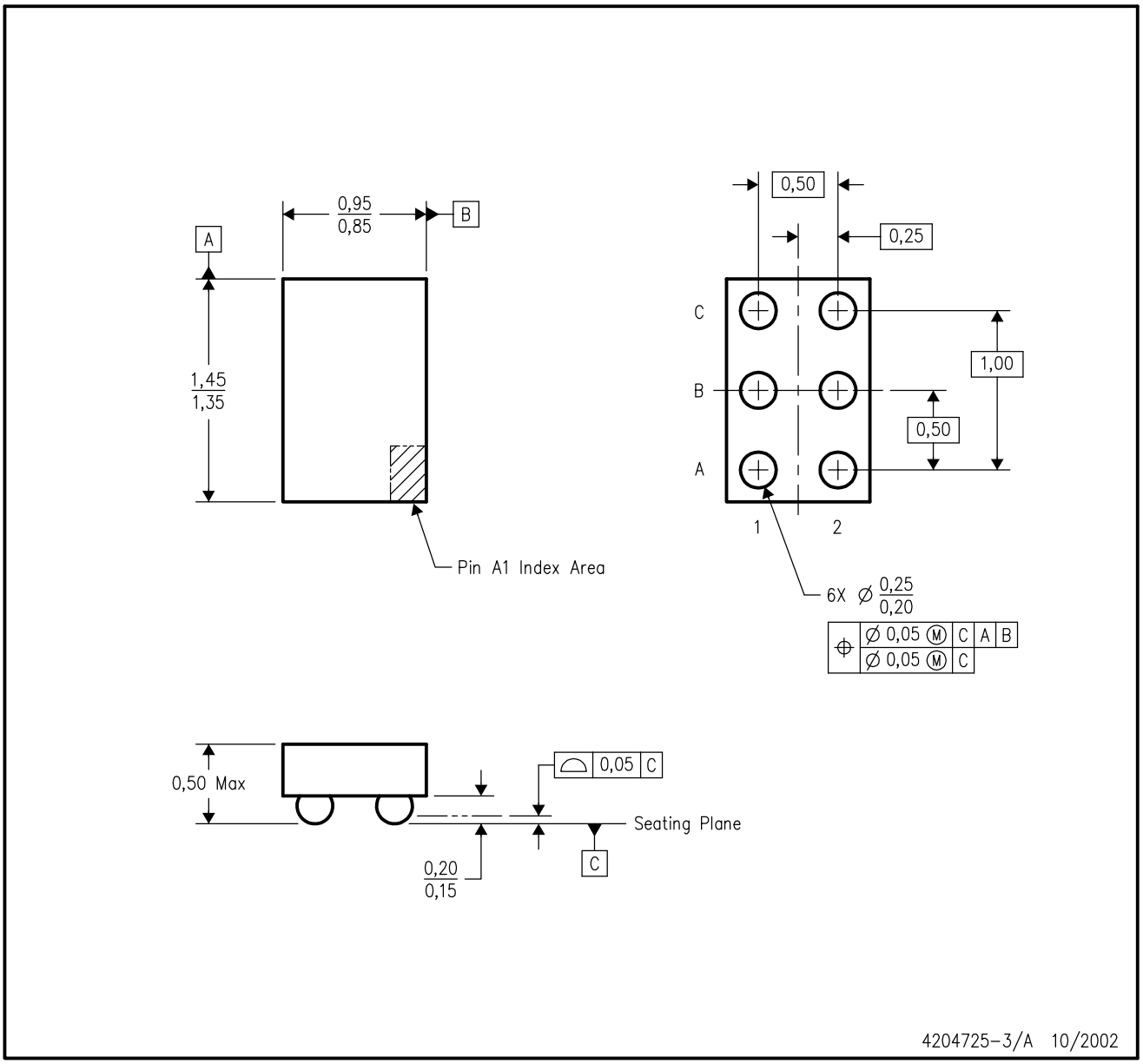
## YZP (R–XBGA–N6) DIE–SIZE BALL GRID ARRAY




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. This package is lead–free. Refer to the 6 YEP package (drawing 4204725) for tin–lead (SnPb).

**NanoFree is a trademark of Texas Instruments.**

YEP (R–XBGA–N6) DIE–SIZE BALL GRID ARRAY




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoStar™ package configuration.
D. This package is tin–lead (SnPb). Refer to the 6 YZP package (drawing 4204741) for lead–free.

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